2.7V to 5.5V, 3A 1ch Synchronous Buck Converter integrated FET

BD8963EFJ

●General Description

ROHM's high efficiency step-down switching regulator BD8963EFJ is a power supply designed to produce a low voltage including 1 volts from 5.5/3.3 volts power supply line. Offers high efficiency with synchronous rectifier. Employs a current mode control system to provide faster transient response to sudden change in load.

●Features

- Offers fast transient response with current mode PWM control system.
- Offers highly efficiency for all load range with synchronous rectifier (Nch/Pch FET)
- Incorporates soft-start function.
- Incorporates thermal protection and ULVO functions.
- Incorporates short-current protection circuit with time delay function.
- Incorporates shutdown function

●Applications

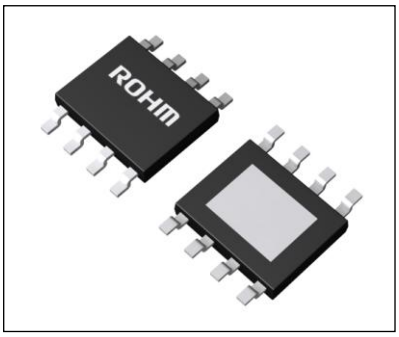
Power supply for LSI including DSP, Micro computer and ASIC

●Key Specification

- Input voltage range: 2.7V to 5.5V
- Output voltage range: 1.0V to 2.5V
- Average output Current: 3A(Max.)
- Switching frequency: 1MHz(Typ.)
- Pch FET ON resistance: 145mΩ(Typ.)
- Nch FET ON resistance: 80mΩ(Typ.)
- Standby current: 5μA (Typ.)
- Operating temperature range: -25℃ to +85℃

●Package

	(Typ.)	(Typ.)	(Max.)
HTSOP-J8	4.90mm x 6.00mm x 1.00mm		



HTSOP-J8

●Typical Application Circuit

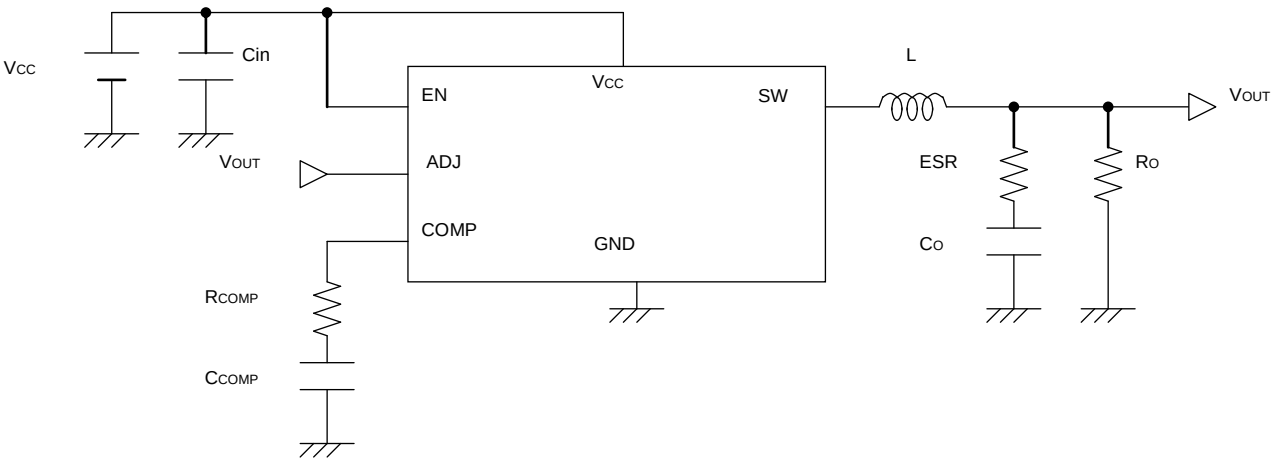


Fig.1 Typical Application Circuit

●**Pin configuration(TOP VIEW)**

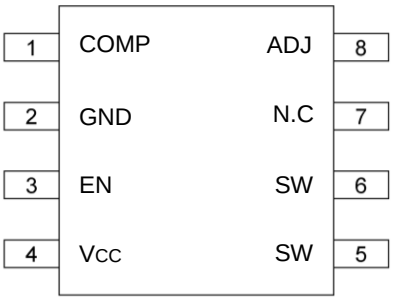


Fig.2 Pin configuration

●**Pin Description**

Pin No.	Pin name	PIN function
1	COMP	GmAmp output pin/Connected phase compensation capacitor
2	GND	Ground
3	EN	Enable pin(Active High, Open Active)
4	Vcc	VCC power supply input pin
5	SW	Pch/Nch FET drain output pin
6	SW	Pch/Nch FET drain output pin
7	N.C	Non Connect
8	ADJ	Output voltage detect pin

●**Block Diagram**

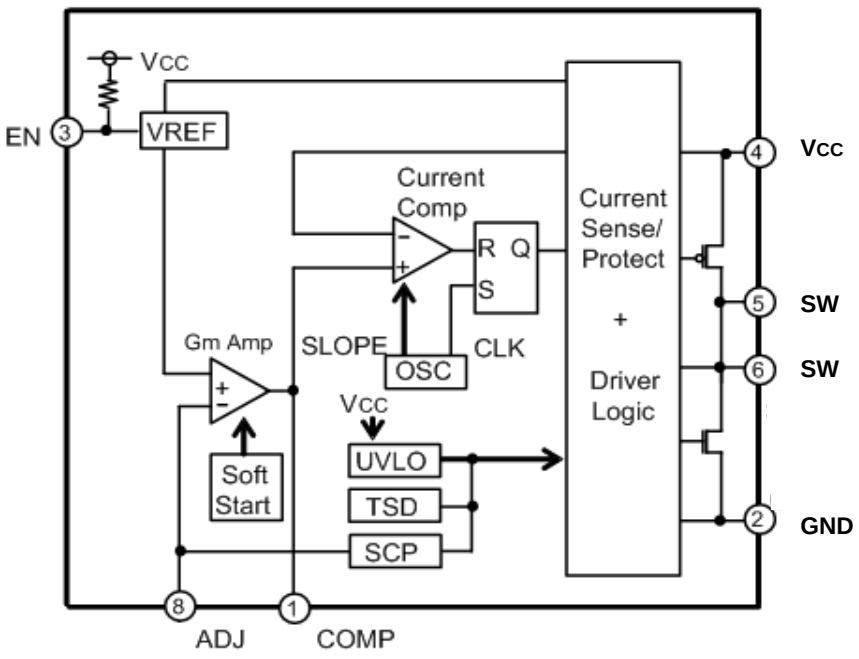


Fig.3 Block Diagram

●**Absolute Maximum Ratings**

Parameter	Symbol	Ratings	Unit
Vcc Voltage	Vcc	-0.3 to +7 *1	V
EN Voltage	VEN	-0.3 to +7	V
SW,COMP Voltage	VSW,VCOMP	-0.3 to +7	V
Power Dissipation 1	Pd1	0.5*2	W
Power Dissipation 2	Pd2	3.76*3	W
Operating temperature range	Topr	-25 to +85	℃
Storage temperature range	Tstg	-55 to +150	℃
Maximum junction temperature	Tjmax	+150	℃

*1 Pd should not be exceeded.
*2 Reduced by 4.0mW for increase in Ta of 1℃ above 25℃.
*3 Reduced by 30.0mW for increase in Ta of 1℃ above 25℃.
(when mounted on a board 70.0mm × 70.0mm × 1.6mm Glass-epoxy PCB)

●**Recommended Operating Ratings** (Ta=-25 to +85℃)

Parameter	Symbol	Ratings			Unit
		Min.	Typ.	Max.	
Power Supply Voltage	Vcc	2.7 *5	5.0	5.5	V
EN Voltage	VEN	0	-	Vcc	V
Output voltage range	VOUT	1.0	-	2.5*4	V
SW average output current	Isw	-	-	3.0*5	A

*4 In case set output voltage 1.6V or more, VccMin. = Vout +2.25V
*5 Pd should not be exceeded.

●**Electrical Characteristics** (Unless otherwise specified , Ta=25℃ Vcc=5V, EN=Vcc, R_1=20kΩ, R_2=7.5kΩ)

Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
Standby Current	ISTB	-	5	20	μA	EN=GND
Bias Current	Icc	-	350	600	μA	
EN Low Voltage	VENL	-	GND	0.3	V	Stand-by Mode
EN High Voltage	VENH	2.0	Vcc	-	V	Active Mode
EN Current	IEN	-	1.25	10	μA	VEN=5V
Oscillation Frequency	Fosc	0.8	1	1.2	MHz	
Pch FET ON Resistance	RONP	-	145	290	mΩ	Vcc=5V
Nch FET ON Resistance	RONN	-	80	160	mΩ	Vcc=5V
ADJ Reference Voltage	VADJ	0.788	0.800	0.812	V	
COMP Sink Current	ICOSI	10	25	-	μA	VADJ=1.0V
COMP Source Current	ICOSO	10	25	-	μA	VADJ=0.6V
UVLO Threshold Voltage	VUVLO1	2.400	2.500	2.600	V	Vcc=5V→0V
UVLO Hysteresis Voltage	VUVLO2	2.425	2.550	2.700	V	Vcc=0V→5V
Soft Start Time	TSS	0.5	1	2	ms	
Timer Latch Time	TLATCH	1	2	4	ms	
Output Short circuit Threshold Voltage	VSCP	-	VOUT × 0.5	VOUT × 0.7	V	VOUT=1.0V→0V

●Typical Performance Curves

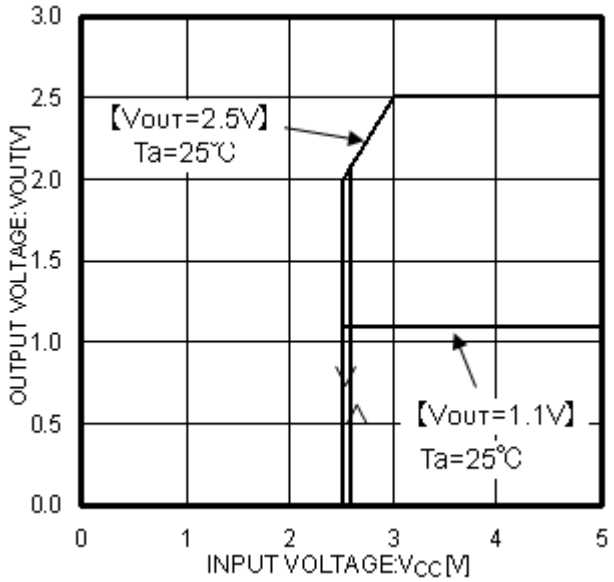


Fig.4 Vcc-Vout

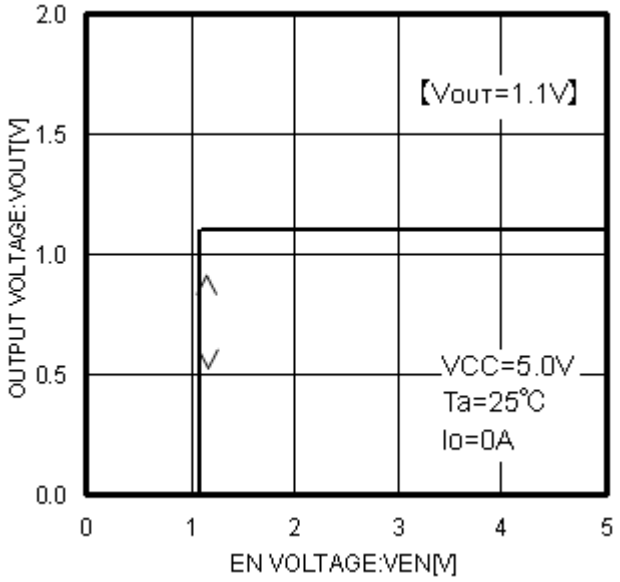


Fig.5 V_{EN}-Vout

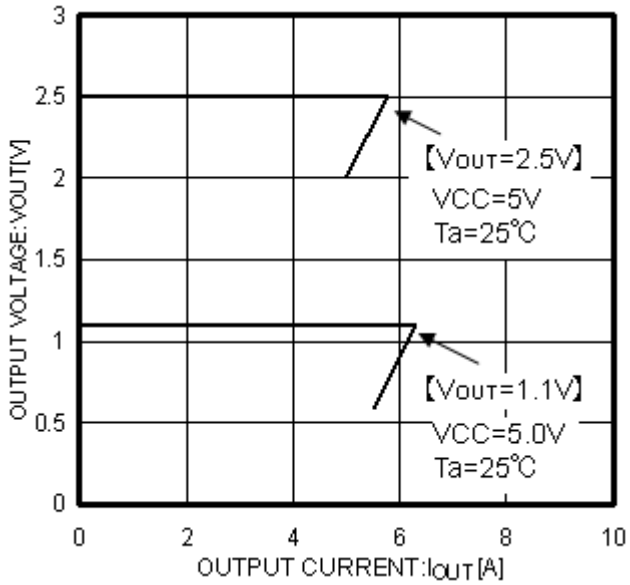


Fig.6 I_{OUT}-V_{OUT}

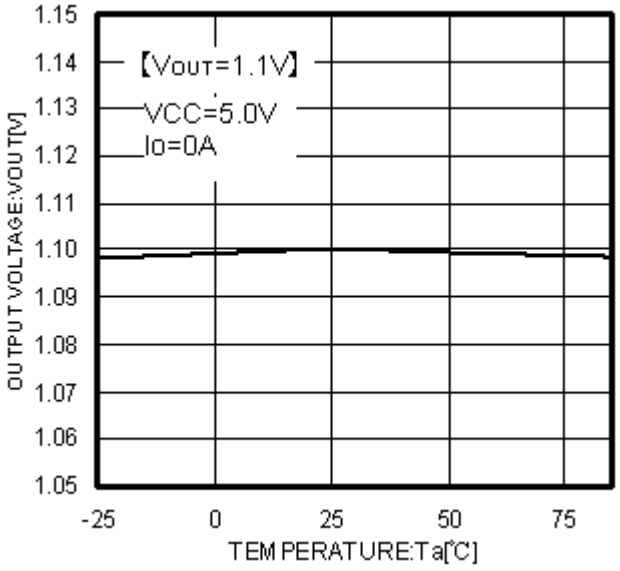


Fig. 7 Ta-V_{OUT}

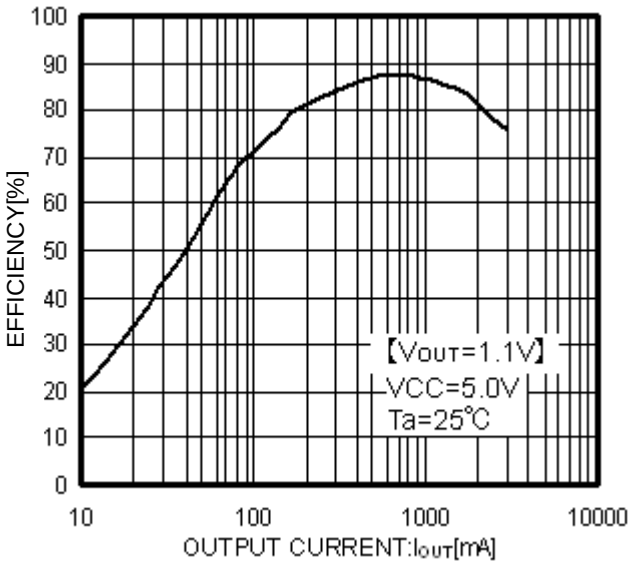


Fig.8 Efficiency

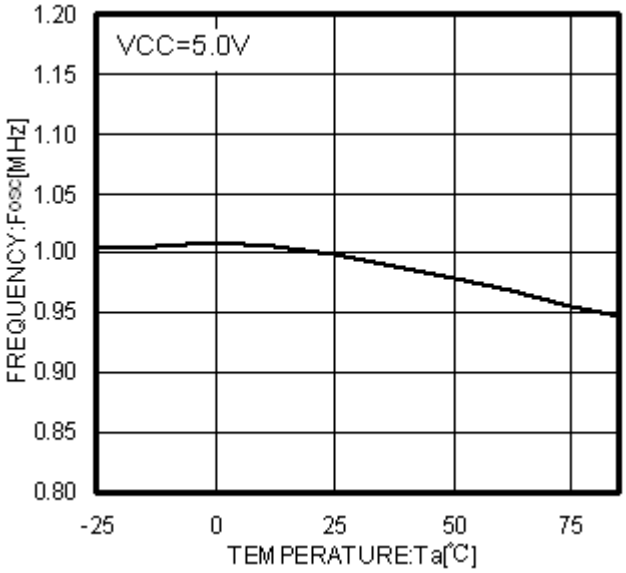


Fig.9 Ta-F_{OSC}

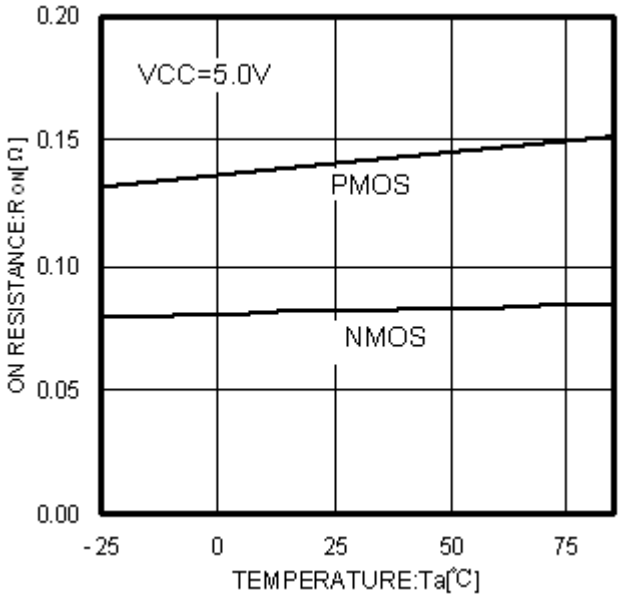


Fig.10 Ta-R_{ONN}, R_{ONP}

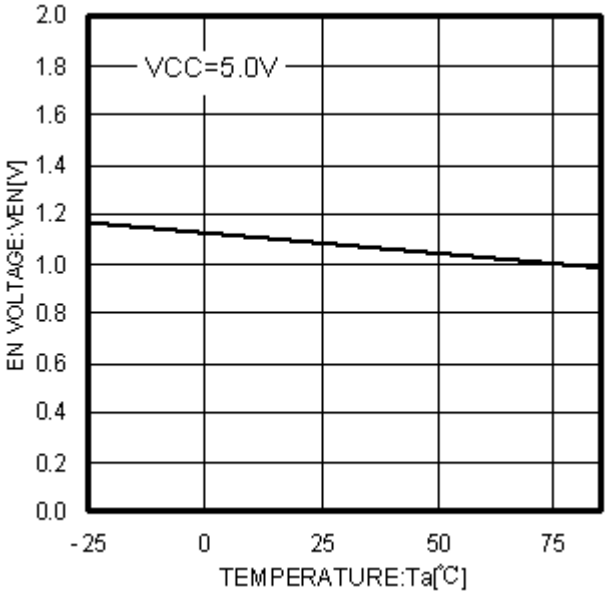


Fig.11 Ta-V_{EN}

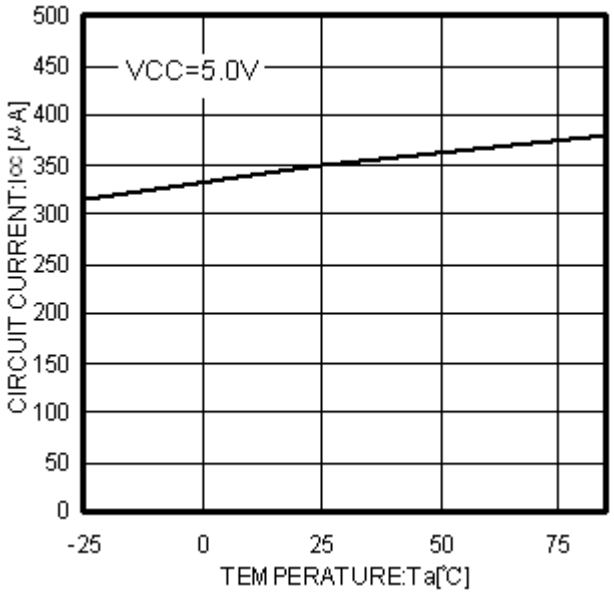


Fig.12 Ta-I_{CC}

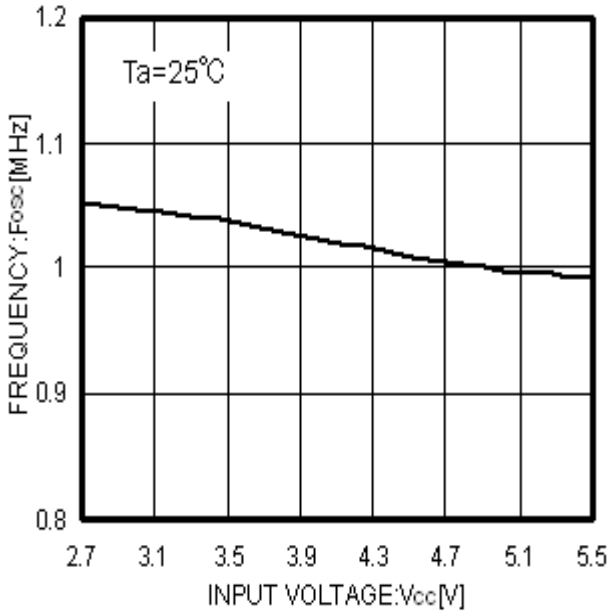


Fig.13 Vcc-F_{OSC}

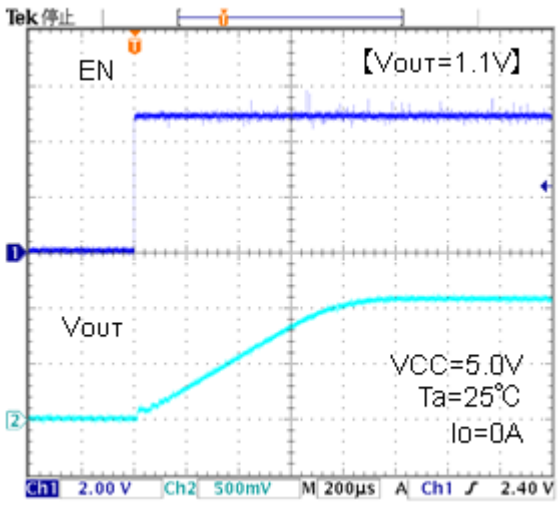


Fig.14 Soft start waveform

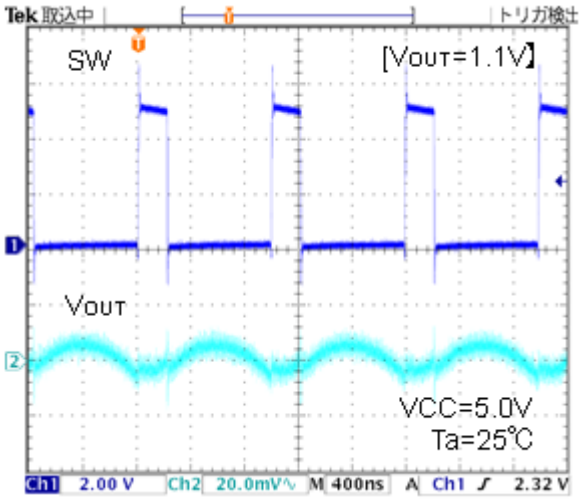


Fig.15 SW waveform Io=10mA

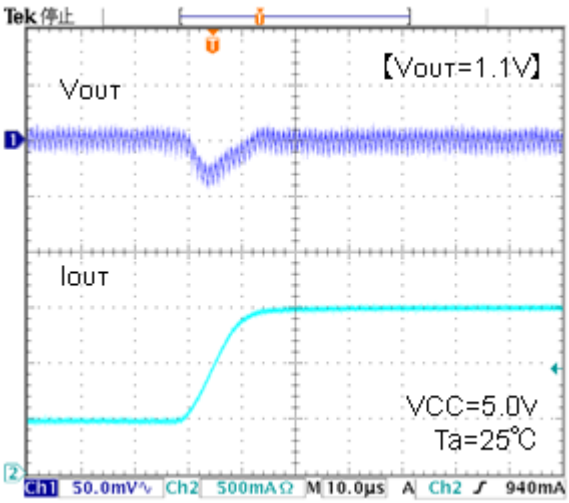


Fig. 16 Transient response
Io=0.5A→1.5A(10µs)

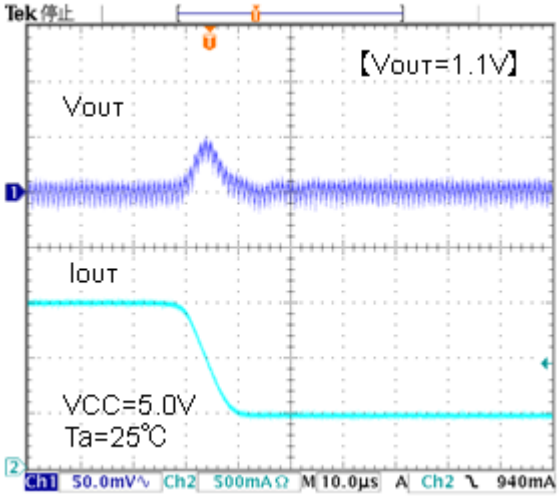


Fig. 17 Transient response
Io=1.5A→0.5A(10µs)

Application Information

●Operation

○Synchronous rectifier

It does not require the power to be dissipated by a rectifier externally connected to a conventional DC/DC converter IC, and its P.N junction shoot-through protection circuit limits the shoot-through current during operation, by which the power dissipation of the set is reduced.

○Current mode PWM control

Synthesizes a PWM control signal with a inductor current feedback loop added to the voltage feedback.

・PWM (Pulse Width Modulation) control

The oscillation frequency for PWM is 1 MHz. SET signal form OSC turns ON a P-channel MOS FET (while a N-channel MOS FET is turned OFF), and an inductor current I_L increases. The current comparator (Current Comp) receives two signals, a current feedback control signal (SENSE: Voltage converted from I_L) and a voltage feedback control signal (FB), and issues a RESET signal if both input signals are identical to each other, and turns OFF the P-channel MOS FET (while a N-channel MOS FET is turned ON) for the rest of the fixed period. The PWM control repeat this operation.

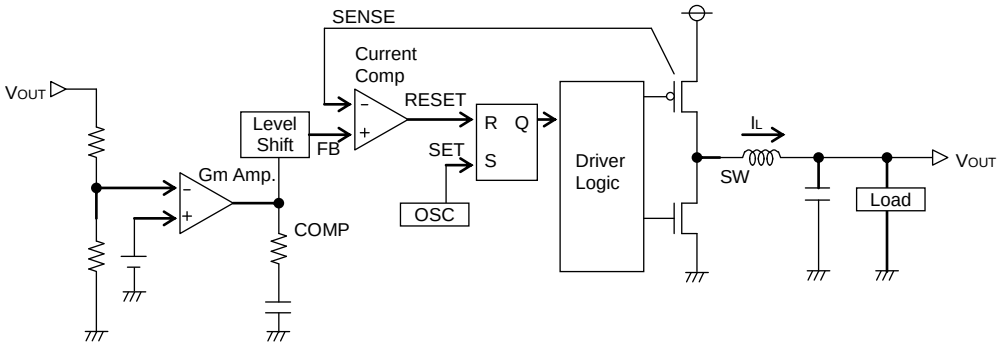


Fig.18 Diagram of current mode PWM control

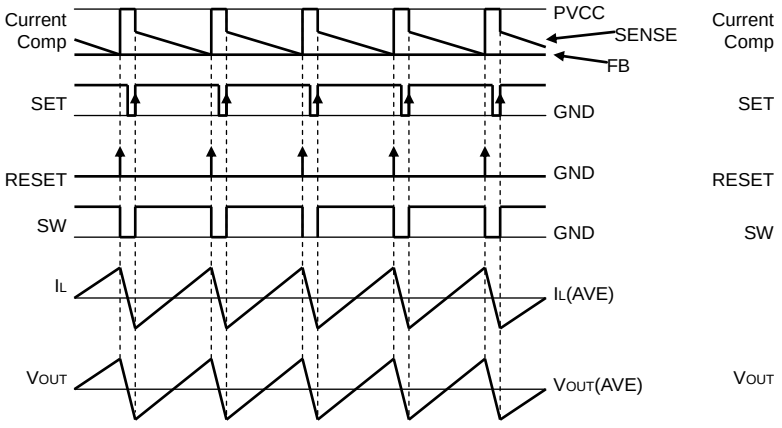


Fig.19 PWM switching timing chart

●Description of operations

・Soft-start function

EN terminal shifted to “High” activates a soft-starter to gradually establish the output voltage with the current limited during startup, by which it is possible to prevent an overshoot of output voltage and an inrush current.

・Shutdown function

With EN terminal shifted to “Low”, the device turns to Standby Mode, and all the function blocks including reference voltage circuit, internal oscillator and drivers are turned to OFF. Circuit current during standby is 5μA (Typ.).

・UVLO function

Detects whether the input voltage sufficient to secure the output voltage of this IC is supplied. And the hysteresis width of 50mV (Typ.) is provided to prevent output chattering.

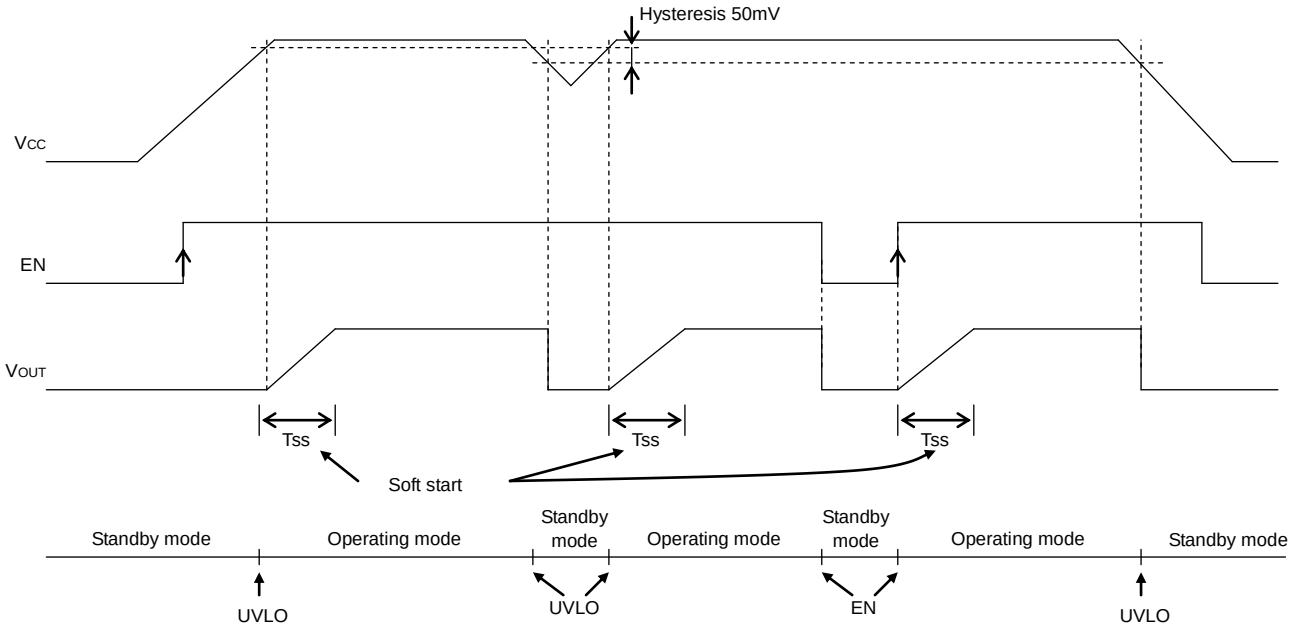


Fig.20 Soft start, Shutdown, UVLO timing chart

・Short-current protection circuit with time delay function

Turns OFF the output to protect the IC from breakdown when the incorporated current limiter is activated continuously for the fixed time(T_{LATCH}) or more. The output thus held tuned OFF may be recovered by restarting EN or by re-unlocking UVLO.

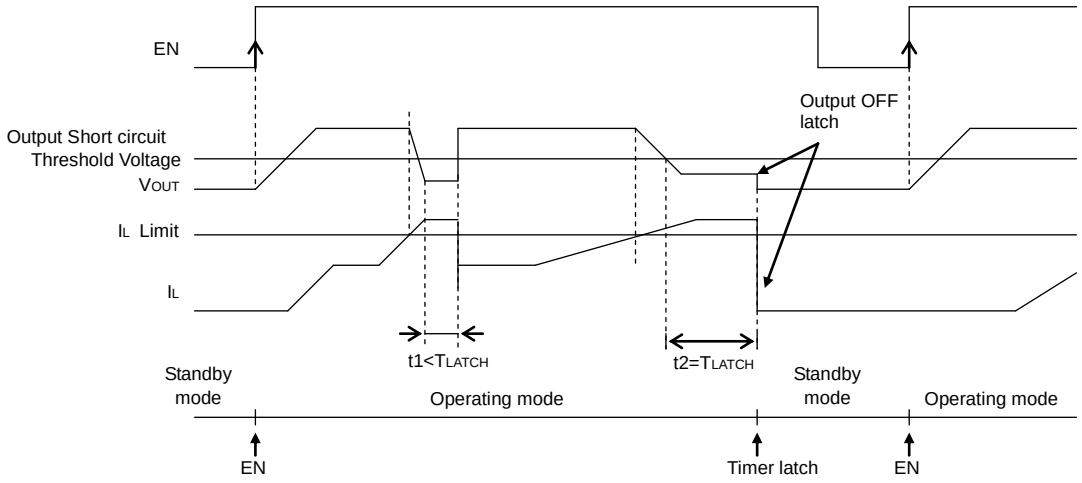
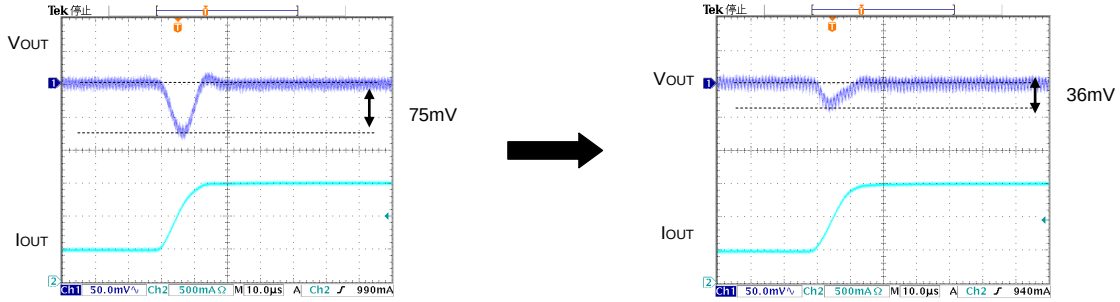


Fig.21 Short-current protection circuit with time delay timing chart

●Information on advantages

Advantage 1 : Offers fast transient response with current mode control system.

Conventional product (Load response Io= 0.5A→1.5A) BD8963EFJ (Load response Io= 0.5A→1.5A)



Voltage drop due to sudden change in load was reduced by about 50%.

Fig.22 Comparison of transient response

Advantage 2 : Offers high efficiency with synchronous rectifier

Utilizes the synchronous rectifying mode and the low on-resistance MOS FETs incorporated as power transistor.

- ON resistance of P-channel MOS FET : 145mΩ(Typ.)
- ON resistance of N-channel MOS FET : 80mΩ(Typ.)

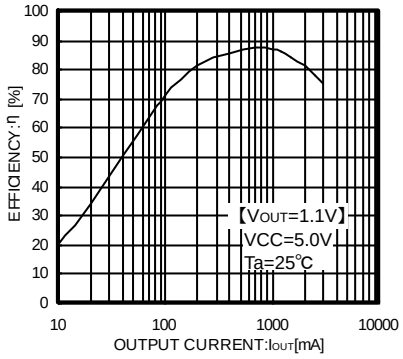


Fig.23 Efficiency

Advantage 3 : ・Supplied in smaller package due to small-sized power MOS FET incorporated.

・Output capacitor Co required for current mode control: 10µF ceramic capacitor
・Inductance L required for the operating frequency of 1 MHz: 1.5µH inductor

Reduces a mounting area required.

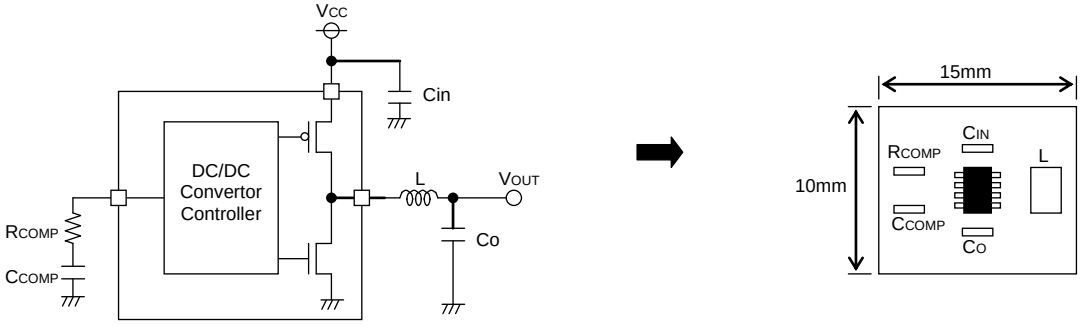


Fig.24 Example application

●Switching regulator efficiency

Efficiency η may be expressed by the equation shown below:

$$\eta = \frac{V_{OUT} \times I_{OUT}}{Vin \times Iin} \times 100[\%] = \frac{P_{OUT}}{Pin} \times 100[\%] = \frac{P_{OUT}}{P_{OUT}+P_{D}\alpha} \times 100[\%]$$

Efficiency may be improved by reducing the switching regulator power dissipation factors $P_D\alpha$ as follows:

Dissipation factors:
1) ON resistance dissipation of inductor and FET : PD(I^2R)
2) Gate charge/discharge dissipation : PD(Gate)
3) Switching dissipation : PD(SW)
4) ESR dissipation of capacitor : PD(ESR)
5) Operating current dissipation of IC : PD(IC)

1)PD(I^2R)=$I_{OUT}^2 \times (R_{COIL}+R_{ON})$ (R_{COIL}[Ω] : DC resistance of inductor, R_{ON}[Ω] : ON resistance of FET, I_{OUT}[A] : Output current.)

2)PD(Gate)=$Cgs \times f \times V^2$ (Cgs[F] : Gate capacitance of FET, f[Hz] : Switching frequency, V[V] : Gate driving voltage of FET)

3)PD(SW)= $\frac{Vin^2 \times C_{RSS} \times I_{OUT} \times f}{I_{DRIVE}}$ (C_{RSS}[F] : Reverse transfer capacitance of FET, I_{DRIVE}[A] : Peak current of gate.)

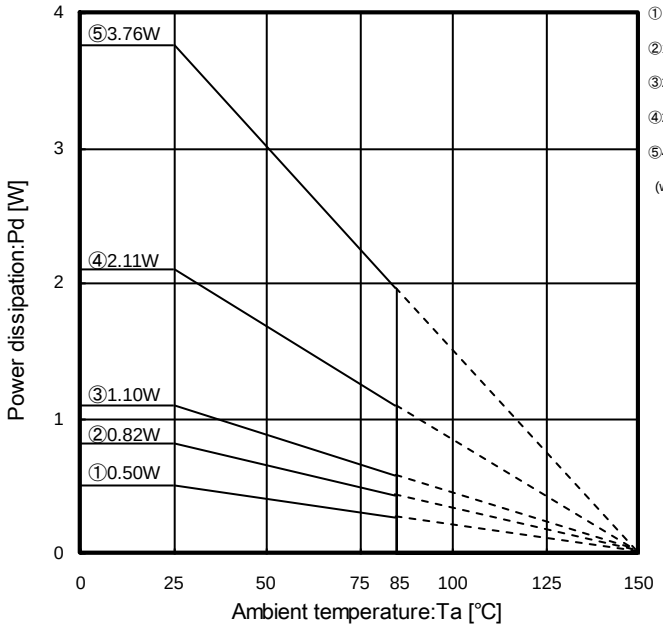
4)PD(ESR)=$I_{RMS}^2 \times ESR$ (I_{RMS}[A] : Ripple current of capacitor, ESR[Ω] : Equivalent series resistance.)

5)PD(IC)=$Vin \times I_{CC}$ (I_{CC}[A] : Circuit current.)

●Consideration on permissible dissipation and heat generation

As this IC functions with high efficiency without significant heat generation in most applications, no special consideration is needed on permissible dissipation or heat generation. In case of extreme conditions, however, including lower input voltage, higher output voltage, heavier load, and/or higher temperature, the permissible dissipation and/or heat generation must be carefully considered.

For dissipation, only conduction losses due to DC resistance of inductor and ON resistance of FET are considered. Because the conduction losses are considered to play the leading role among other dissipation mentioned above including gate charge/discharge dissipation and switching dissipation.



① IC only
θj-a=249.5℃/W
②1 layers（copper foil area:0mm×0mm）
θj-a=153.2℃/W
③2 layers（copper foil area:15mm×15mm）
θj-a=113.6℃/W
④2 layers（copper foil area:70mm×70mm）
θj-a=59.2℃/W
⑤4 layers（copper foil area:70mm×70mm）
θj-a=33.3℃/W
(when mounted on a board 70mm×70mm×1.6mm Glass-epoxy PCB with termal Via)

$P=IOUT^2 \times RON$
$RON=D \times RONP+(1-D)RONN$

D：ON duty (=VOUT/VCC)
RCOIL：DC resistance of coil
RONP：ON resistance of P-channel MOS FET
RONN：ON resistance of N-channel MOS FET
IOUT：Output current

Fig.25 Thermal derating curve
(HTSOP-J8)

Ex.)V_{CC}=5V, V_{OUT}=1.1V, R_{ONP}=0.145Ω, R_{ONN}=0.08Ω
I_{OUT}=3A, for example,
$D=V_{OUT}/V_{CC}=1.1/5=0.22$
$R_{ON}=0.22 \times 0.145+(1-0.22) \times 0.08$
$=0.0319+0.0624$
$=0.0943[\Omega]$

$P=3^2 \times 0.0943=0.8487[W]$

As R_{ONP} is greater than R_{ONN} in this IC, the dissipation increases as the ON duty becomes greater.
With the consideration on the dissipation as above, thermal design must be carried out with sufficient margin allowed.

●Selection of components externally connected

1. Selection of inductor (L)

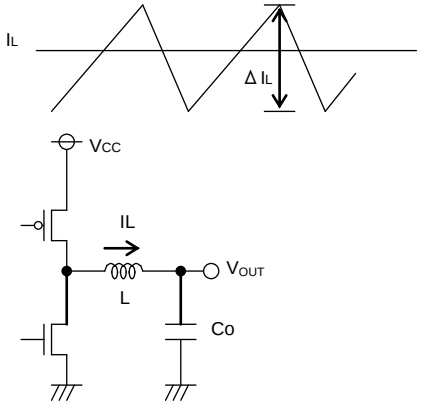


Fig.26 Output ripple current

The inductance significantly depends on output ripple current. As seen in the equation (1), the ripple current decreases as the inductor and/or switching frequency increases.

$$\Delta I_L = \frac{(V_{CC}-V_{OUT}) \times V_{OUT}}{L \times V_{CC} \times f} \text{ [A]} \cdots (1)$$

Appropriate ripple current at output should be 20% more or less of the maximum output current.

$$\Delta I_L = 0.2 \times I_{OUT}\text{max. [A]} \cdots (2)$$

$$L = \frac{(V_{CC}-V_{OUT}) \times V_{OUT}}{\Delta I_L \times V_{CC} \times f} \text{ [H]} \cdots (3)$$

(ΔI_L: Output ripple current, and f: Switching frequency)

*Current exceeding the current rating of the inductor results in magnetic saturation of the inductor, which decreases efficiency. The inductor must be selected allowing sufficient margin with which the peak current may not exceed its current rating.

If V_{CC}=5V, V_{OUT}=1.1V, f=1MHz, $\Delta I_L = 0.2 \times 3A = 0.6A$, for example,(BD8963EFJ)

$$L = \frac{(5-1.1) \times 1.1}{0.6 \times 5 \times 1M} = 1.43\mu \rightarrow 1.5[\mu H]$$

*Select the inductor of low resistance component (such as DCR and ACR) to minimize dissipation in the inductor for better efficiency.

2. Selection of output capacitor (Co)

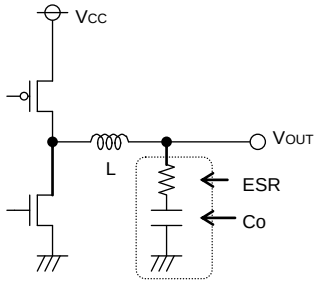


Fig.27 Output capacitor

Output capacitor should be selected with the consideration on the stability region and the equivalent series resistance required to smooth ripple voltage.

Output ripple voltage is determined by the equation (4) :

$$\Delta V_{OUT} = \Delta I_L \times ESR \text{ [V]} \cdots (4)$$

(ΔI_L: Output ripple current, ESR: Equivalent series resistance of output capacitor)

*Rating of the capacitor should be determined allowing sufficient margin against output voltage. A 10µF to 100µF ceramic capacitor is recommended.
Less ESR allows reduction in output ripple voltage.

3. Selection of input capacitor (Cin)

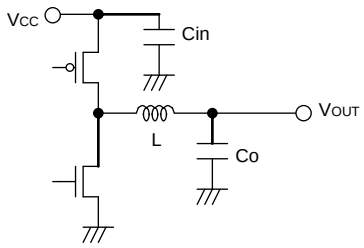


Fig.28 Input capacitor

Input capacitor to select must be a low ESR capacitor of the capacitance sufficient to cope with high ripple current to prevent high transient voltage. The ripple current IRMS is given by the equation (5):

$$I_{RMS} = I_{OUT} \times \frac{\sqrt{V_{OUT}(V_{CC}-V_{OUT})}}{V_{CC}} \text{ [A]} \cdots (5)$$

< Worst case > $I_{RMS(max.)}$

When Vcc is twice the V_{OUT}, $I_{RMS} = \frac{I_{OUT}}{2}$

If V_{CC}=5V, V_{OUT}=1.1V, and I_{OUT}max.= 3A, (BD8963EFJ)

$$I_{RMS} = 3 \times \frac{\sqrt{1.1 \times (5-1.1)}}{5} = 1.24[A_{RMS}]$$

A low ESR 22µF/10V ceramic capacitor is recommended to reduce ESR dissipation of input capacitor for better efficiency.

4. Determination of RCOMP, CCOMP that works as a phase compensator

As the Current Mode Control is designed to limit a inductor current, a pole (phase lag) appears in the low frequency area due to a CR filter consisting of a output capacitor and a load resistance, while a zero (phase lead) appears in the high frequency area due to the output capacitor and its ESR. So, the phases are easily compensated by adding a zero to the power amplifier output with C and R as described below to cancel a pole at the power amplifier.

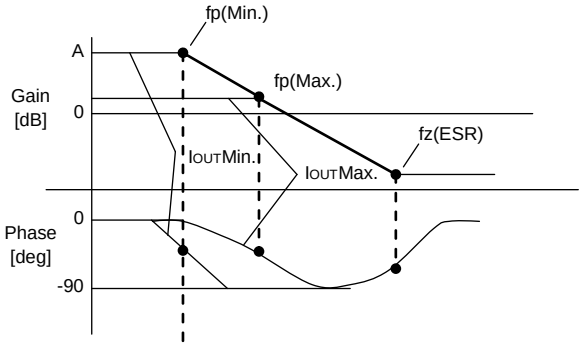


Fig.29 Open loop gain characteristics

$$fp = \frac{1}{2\pi \times R_O \times C_O}$$

$$fz_{(ESR)} = \frac{1}{2\pi \times E_{SR} \times C_O}$$

Pole at power amplifier

When the output current decreases, the load resistance Ro increases and the pole frequency lowers.

$$fp_{(Min.)} = \frac{1}{2\pi \times R_{OMax.} \times C_O}\ [Hz] \leftarrow \text{with lighter load}$$

$$fp_{(Max.)} = \frac{1}{2\pi \times R_{OMin.} \times C_O}\ [Hz] \leftarrow \text{with heavier load}$$

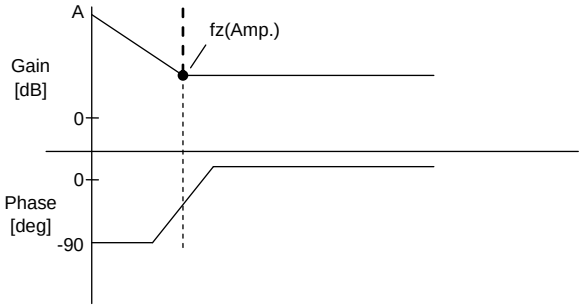


Fig.30 Error amp phase compensation characteristics

Zero at power amplifier

Increasing capacitance of the output capacitor lowers the pole frequency while the zero frequency does not change. (This is because when the capacitance is doubled, the capacitor ESR reduces to half.)

$$fz_{(Amp.)} = \frac{1}{2\pi \times R_{ITH} \times C_{ITH}}$$

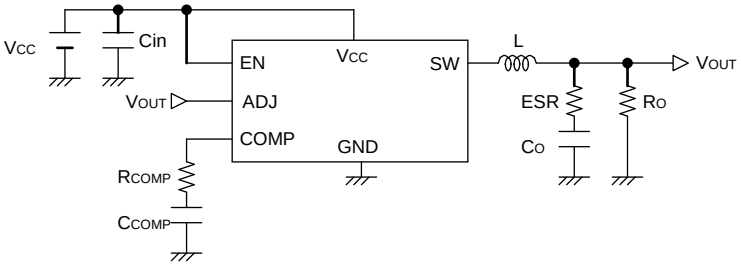


Fig.31 Typical application

Stable feedback loop may be achieved by canceling the pole fp (Min.) produced by the output capacitor and the load resistance with CR zero correction by the error amplifier.

$$fz_{(Amp.)} = fp_{(Min.)}$$

$$\longrightarrow \frac{1}{2\pi \times R_{COMP} \times C_{COMP}} = \frac{1}{2\pi \times R_{OMax.} \times C_O}$$

5. Determination of output voltage

The output voltage V_{OUT} is determined by the equation (6):
$V_{OUT}=(R2/R1+1)\times V_{ADJ}$ ・・・(6) V_{ADJ}: Voltage at ADJ terminal (0.8V Typ.)
With R1 and R2 adjusted, the output voltage may be determined as required.

〔Adjustable output voltage range : 1.0V to 2.5V〕

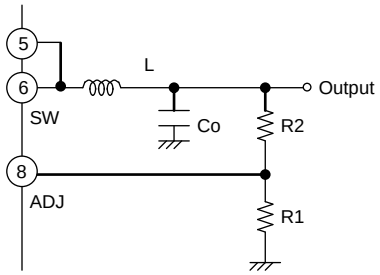


Fig.32 Determination of output voltage

Use 1 kΩ to 100 kΩ resistor for R1. If a resistor of the resistance higher than 100 kΩ is used, check the assembled set carefully for ripple voltage etc.

The lower limit of input voltage depends on the output voltage.
Basically, it is recommended to use in the condition :
$V_{CCmin} = V_{OUT}+2.25V$.
Fig.33. shows the necessary output current value at the lower limit of input voltage. (DCR of inductor : 0.05Ω)
This data is the characteristic value, so it' doesn't guarantee the operation range,

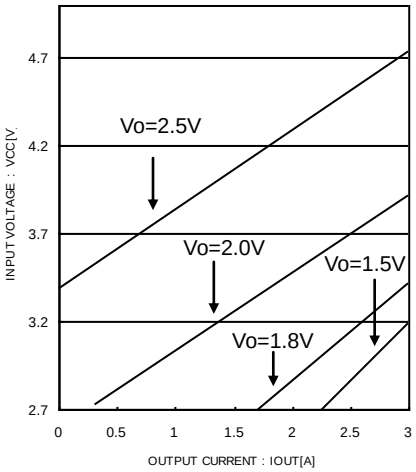


Fig.33 minimum input voltage in each output voltage

●**Cautions on PC Board layout**

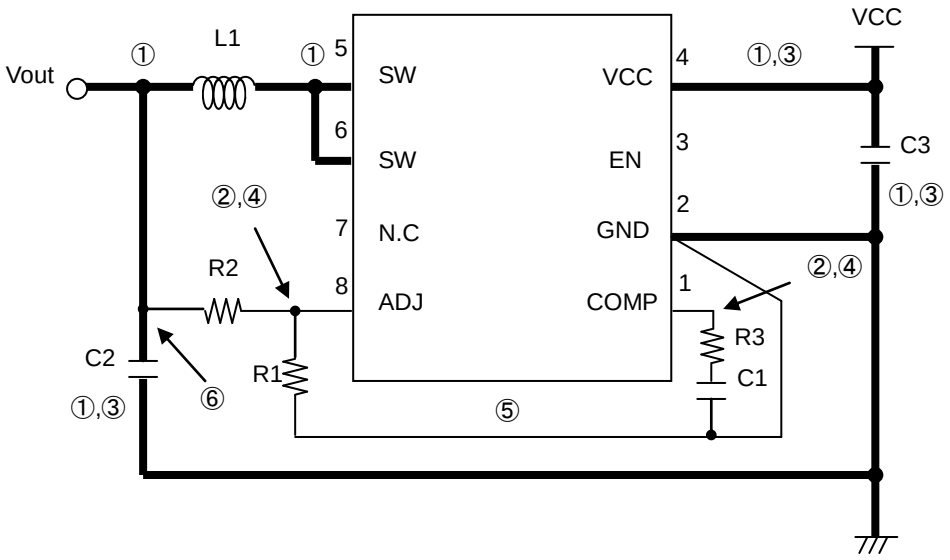
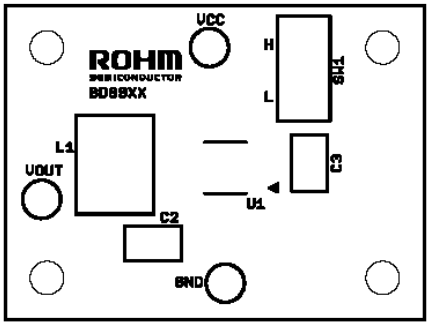


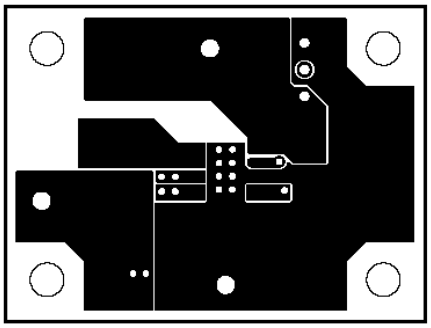
Fig.34 Layout diagram

①To avoid conduction loss, please keep Black thick line as short and thick as possible.
②Don't close to switching current loop.
③Close to IC pin as possible.
④Keep PCB trace as short as possible.
⑤Use single point ground structure to connect with Pin2.
⑥Close to C2 as possible.

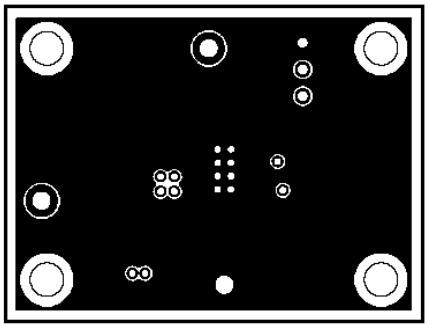
※ HTSOP-J8 (BD8963EFJ) has thermal PAD on the reverse of the package.
The package thermal performance may be enhanced by bonding the PAD to GND plane which take a large area of PCB.



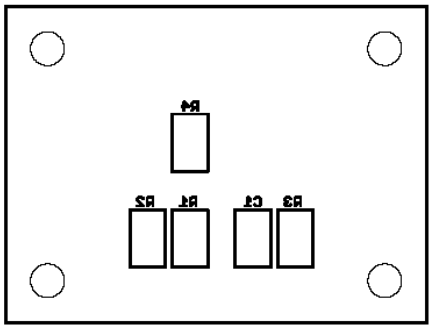
Top Silkscreen Overlay



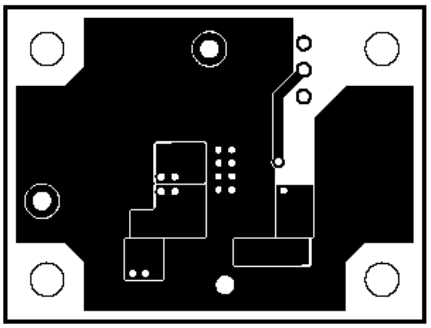
Top Layer



Middle Layer



Bottom Silkscreen Overlay



Bottom Layer

Fig.35 Reference PCB Layout Pattern

●Recommended components Lists on above application

Symbol	Part	Value		Manufacturer	Series
L	Coil	1.5µH		TDK	VLC6045T-1R5N
CIN	Ceramic capacitor	Vcc-VOUT>3V	10µF	Kyocera	CM316X5R106M10A
		Vcc-VOUT<3V	22µF	Kyocera	CM32X5R226M10A
CO	Ceramic capacitor	10µF		Kyocera	CM316X5R106M10A
CCOMP	Ceramic capacitor	VOUT=1.0V	330pF	Murata	GRM18 Series
		VOUT=1.1V	330pF	Murata	GRM18 Series
		VOUT=1.2V	330pF	Murata	GRM18 Series
		VOUT=1.5V	390pF	Murata	GRM18 Series
		VOUT=1.8V	390pF	Murata	GRM18 Series
		VOUT=2.5V	390pF	Murata	GRM18 Series
RCOMP	Resistance	VOUT=1.0V	2kΩ	Rohm	MCR03 Series
		VOUT=1.1V	2kΩ	Rohm	MCR03 Series
		VOUT=1.2V	2.4kΩ	Rohm	MCR03 Series
		VOUT=1.5V	2.4kΩ	Rohm	MCR03 Series
		VOUT=1.8V	3.6kΩ	Rohm	MCR03 Series
		VOUT=2.5V	5.6kΩ	Rohm	MCR03 Series

* The parts list presented above is an example of recommended parts. Although the parts are sound, actual circuit characteristics should be checked on your application carefully before use. Be sure to allow sufficient margins to accommodate variations between external devices and this IC when employing the depicted circuit with other circuit constants modified. Both static and transient characteristics should be considered in establishing these margins.

●I/O equivalence circuit

【BD8963EFJ】

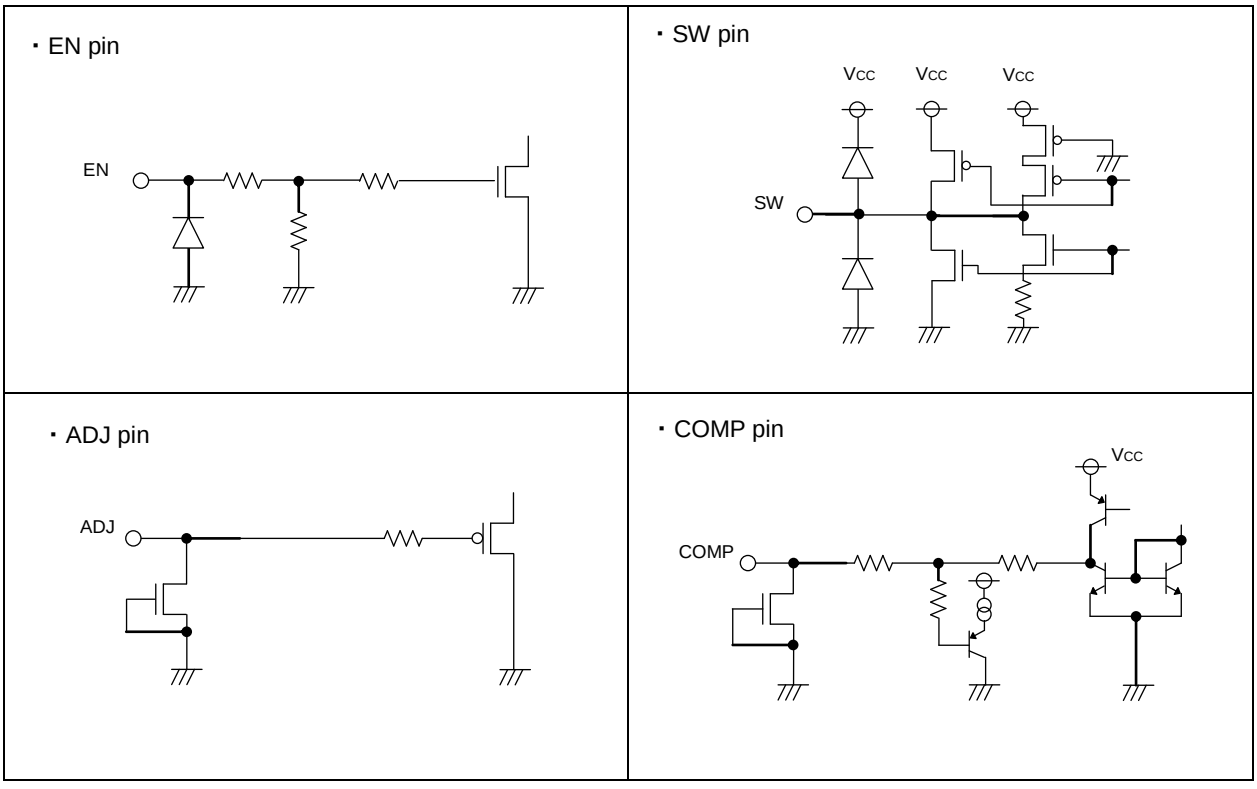


Fig.36 I/O equivalence circuit

●Operational Notes

1. Absolute Maximum Ratings
   While utmost care is taken to quality control of this product, any application that may exceed some of the absolute maximum ratings including the voltage applied and the operating temperature range may result in breakage. If broken, short-mode or open-mode may not be identified. So if it is expected to encounter with special mode that may exceed the absolute maximum ratings, it is requested to take necessary safety measures physically including insertion of fuses.

2. Electrical potential at GND
   GND must be designed to have the lowest electrical potential In any operating conditions.

3. Short-circuiting between terminals, and mismounting
   When mounting to pc board, care must be taken to avoid mistake in its orientation and alignment. Failure to do so may result in IC breakdown. Short-circuiting due to foreign matters entered between output terminals, or between output and power supply or GND may also cause breakdown.

4. Operation in Strong electromagnetic field
   Be noted that using the IC in the strong electromagnetic radiation can cause operation failures.

5. Thermal shutdown protection circuit
   Thermal shutdown protection circuit is the circuit designed to isolate the IC from thermal runaway, and not intended to protect and guarantee the IC. So, the IC the thermal shutdown protection circuit of which is once activated should not be used thereafter for any operation originally intended.

6. Inspection with the IC set to a pc board
   If a capacitor must be connected to the pin of lower impedance during inspection with the IC set to a pc board, the capacitor must be discharged after each process to avoid stress to the IC. For electrostatic protection, provide proper grounding to assembling processes with special care taken in handling and storage. When connecting to jigs in the inspection process, be sure to turn OFF the power supply before it is connected and removed.

7. Input to IC terminals
   This is a monolithic IC with P^+ isolation between P-substrate and each element as illustrated below. This P-layer and the N-layer of each element form a P-N junction, and various parasitic element are formed.
   If a resistor is joined to a transistor terminal as shown in Fig 37.
   ○P-N junction works as a parasitic diode if the following relationship is satisfied;
   GND>Terminal A (at resistor side), or GND>Terminal B (at transistor side); and
   ○if GND>Terminal B (at NPN transistor side),
   a parasitic NPN transistor is activated by N-layer of other element adjacent to the above-mentioned parasitic diode.
   The structure of the IC inevitably forms parasitic elements, the activation of which may cause interference among circuits, and/or malfunctions contributing to breakdown. It is therefore requested to take care not to use the device in such manner that the voltage lower than GND (at P-substrate) may be applied to the input terminal, which may result in activation of parasitic elements.

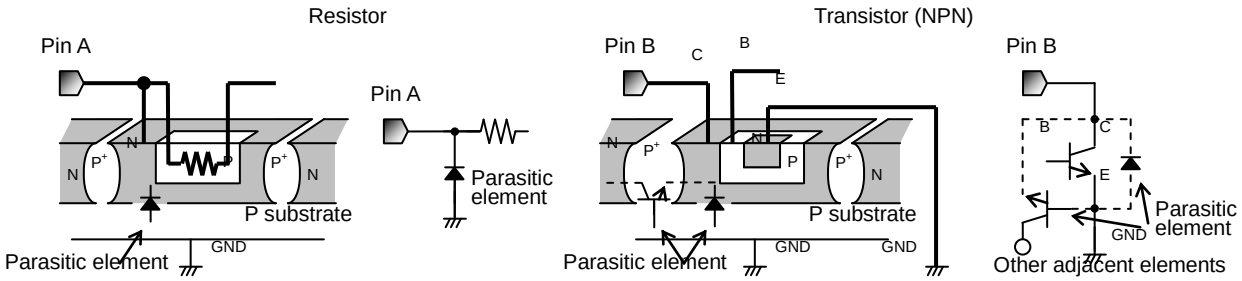


Fig.37 Simplified structure of monorisic IC

8. Ground wiring pattern
   If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

9. Selection of inductor
   It is recommended to use an inductor with a series resistance element (DCR) 0.1Ω or less. Especially, in case output voltage is set 1.6V or more, note that use of a high DCR inductor will cause an inductor loss, resulting in decreased output voltage. Should this condition continue for a specified period (soft start time + timer latch time), output short circuit protection will be activated and output will be latched OFF. When using an inductor over 0.1Ω, be careful to ensure adequate margins for variation between external devices and this IC, including transient as well as static characteristics. Furthermore, in any case, it is recommended to start up the output with EN after supply voltage is within operation range.

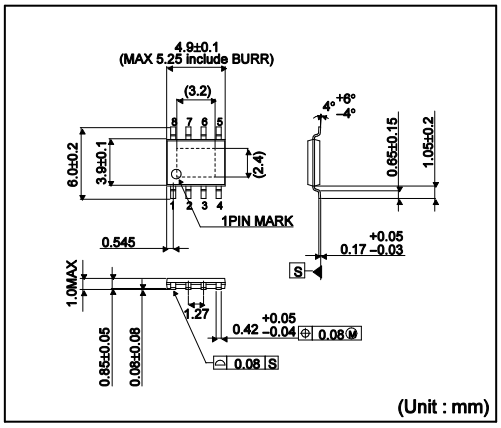
Status of this document
The Japanese version of this document is formal specification. A customer may use this translation version only for a reference to help reading the formal version.
If there are any differences in translation version of this document formal version takes priority

●Ordering Information

B D 8 9 6 3 E F J	E 2
Part Number	Package EFJ: HTSOP-J8
	Packaging and forming specification E2: Embossed tape and reel

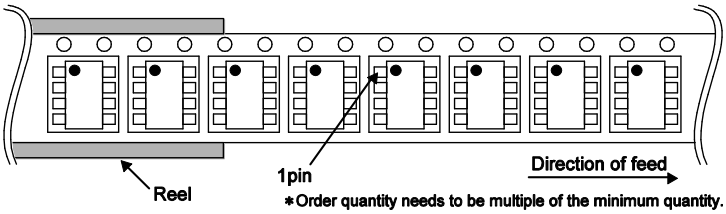
●Physical Dimension Tape and Reel Information

HTSOP-J8



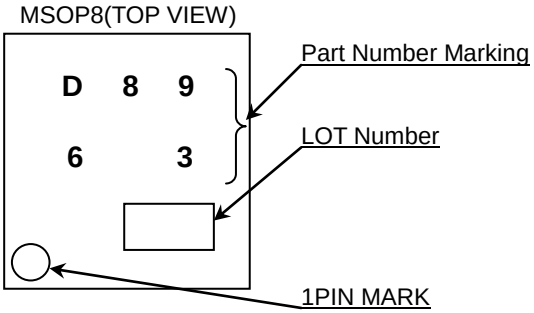
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

●Marking Diagram



●**Revision History**

Date	Revision	Changes
17.Jan.2012	001	New Release

Notice

●Precaution for circuit design

1) The products are designed and produced for application in ordinary electronic equipment (AV equipment, OA equipment, telecommunication equipment, home appliances, amusement equipment, etc.). If the products are to be used in devices requiring extremely high reliability (medical equipment, transport equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or operational error may endanger human life and sufficient fail-safe measures, please consult with the ROHM sales staff in advance. If product malfunctions may result in serious damage, including that to human life, sufficient fail-safe measures must be taken, including the following:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits in the case of single-circuit failure

2) The products are designed for use in a standard environment and not in any special environments. Application of the products in a special environment can deteriorate product performance. Accordingly, verification and confirmation of product performance, prior to use, is recommended if used under the following conditions:
   [a] Use in various types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use outdoors where the products are exposed to direct sunlight, or in dusty places
   [c] Use in places where the products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use in places where the products are exposed to static electricity or electromagnetic waves
   [e] Use in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Use involving sealing or coating the products with resin or other coating materials
   [g] Use involving unclean solder or use of water or water-soluble cleaning agents for cleaning after soldering
   [h] Use of the products in places subject to dew condensation

3) The products are not radiation resistant.

4) Verification and confirmation of performance characteristics of products, after on-board mounting, is advised.

5) In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse) is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

6) De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta).
   When used in sealed area, confirm the actual ambient temperature.

7) Confirm that operation temperature is within the specified range described in product specification.

8) Failure induced under deviant condition from what defined in the product specification cannot be guaranteed.

●Precaution for Mounting / Circuit board design

1) When a highly active halogenous (chlorine, bromine, etc.) flux is used, the remainder of flux may negatively affect product performance and reliability.

2) In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the Company in advance.

Regarding Precaution for Mounting / Circuit board design, please specially refer to ROHM Mounting specification

●Precautions Regarding Application Examples and External Circuits

1) If change is made to the constant of an external circuit, allow a sufficient margin due to variations of the characteristics of the products and external components, including transient characteristics, as well as static characteristics.

2) The application examples, their constants, and other types of information contained herein are applicable only when the products are used in accordance with standard methods. Therefore, if mass production is intended, sufficient consideration to external conditions must be made.

●Precaution for Electrostatic

This product is Electrostatic sensitive product, which may be damaged due to Electrostatic discharge. Please take proper caution during manufacturing and storing so that voltage exceeding Product maximum rating won't be applied to products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

●Precaution for Storage / Transportation

1) Product performance and soldered connections may deteriorate if the products are stored in the following places:
   [a] Where the products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] Where the temperature or humidity exceeds those recommended by the Company
   [c] Storage in direct sunshine or condensation
   [d] Storage in high Electrostatic

2) Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using products of which storage time is exceeding recommended storage time period .

3) Store / transport cartons in the correct direction, which is indicated on a carton as a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4) Use products within the specified time after opening a dry bag.

●Precaution for product label

QR code printed on ROHM product label is only for internal use, and please do not use at customer site. It might contain a internal part number that is inconsistent with an product part number.

●Precaution for disposition

When disposing products please dispose them properly with a industry waste company.

●Precaution for Foreign exchange and Foreign trade act

Since concerned goods might be fallen under controlled goods prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

●Prohibitions Regarding Industrial Property

1) Information and data on products, including application examples, contained in these specifications are simply for reference; the Company does not guarantee any industrial property rights, intellectual property rights, or any other rights of a third party regarding this information or data. Accordingly, the Company does not bear any responsibility for:
   [a] infringement of the intellectual property rights of a third party
   [b] any problems incurred by the use of the products listed herein.

2) The Company prohibits the purchaser of its products to exercise or use the intellectual property rights, industrial property rights, or any other rights that either belong to or are controlled by the Company, other than the right to use, sell, or dispose of the products.