

# 8-bit shift register and latch driver

## BU2114 / BU2114F

The BU2114 and BU2114F are CMOS ICs with low power consumption, and are equipped with an 8-bit shift register latch. Data in the shift register can be latched asynchronously. The outputs (O1 to O8) are open drain outputs (because there is no protection diode, a maximum voltage above  $V_{DD}$ , of up to 7V, can be applied), and one output can drive 36 mA. A total output of up to 150 mA can be driven (when using static operation).

### ●Applications

These are designed for a wide range of applications in microcomputer peripheral circuits, such as in industrial equipment, office telephones, audio visual equipment, and expansion input and output boards.

### ●Features

- 1) The CMOS configuration enables low power consumption.
- 2) Open drain output.
- 3) Latch to 8-bit shift register provided, enabling drive of up to 150mA. ( $I_{SINK} = 36mA$ )
- 4) Cascade connections possible.

### ●Absolute maximum ratings (unless otherwise noted, $T_a = 25^{\circ}C$ )

| Parameter                      |         | Symbol    | Limits                | Unit        |
|--------------------------------|---------|-----------|-----------------------|-------------|
| Applied voltage                |         | $V_{DD}$  | $-0.3 \sim +7.0$      | V           |
| Input voltage                  |         | $V_{IN}$  | $-0.3 \sim V_{DD}0.3$ | V           |
| Operating temperature          |         | $T_{opr}$ | $-25 \sim +75$        | $^{\circ}C$ |
| Storage temperature            |         | $T_{stg}$ | $-55 \sim +150$       | $^{\circ}C$ |
| Input protection diode current |         | $I_D$     | $\pm 20$              | mA          |
| Power dissipation              | BU2114  | $P_d$     | 1100*1                | mW          |
|                                | BU2114F |           | 400*2                 |             |

\*1 Power dissipation is reduced by 8.8mW for each increase in  $T_a$  of  $1^{\circ}C$  over  $25^{\circ}C$ .

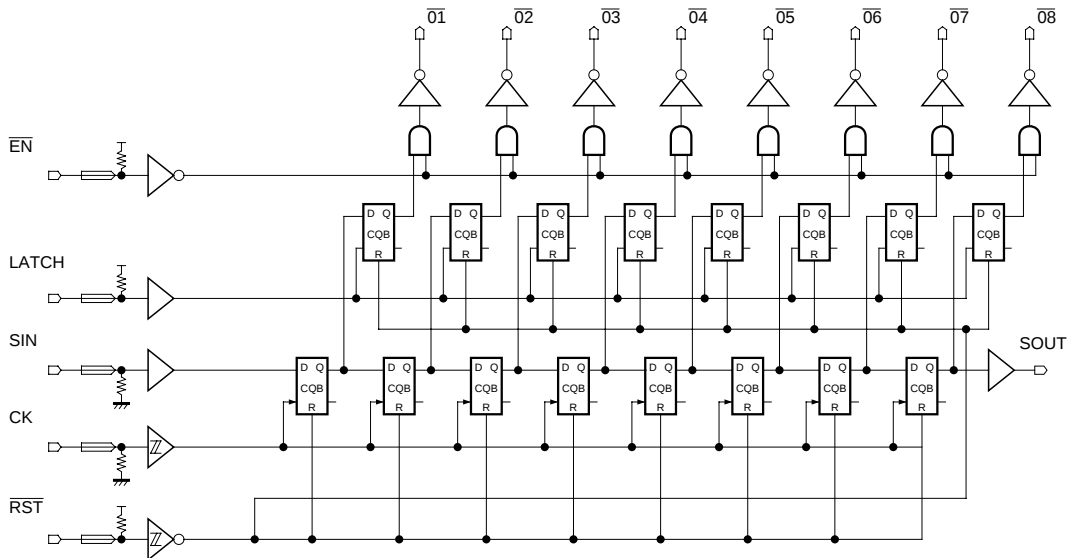
\*2 Power dissipation is reduced by 3.2mW for each increase in  $T_a$  of  $1^{\circ}C$  over  $25^{\circ}C$ .

### ●Recommended operating conditions (unless otherwise noted, $T_a = 25^{\circ}C$ )

| Parameter         | Symbol    | Min. | Typ. | Max.     | Unit | Conditions              |
|-------------------|-----------|------|------|----------|------|-------------------------|
| Recommend voltage | $V_{DD}$  | 4.5  | 5.0  | 5.5      | V    |                         |
| Input voltage     | $V_{IN}$  | 0    | —    | $V_{DD}$ | V    | SIN, CK, LATCH, EN, RST |
| Output voltage    | $V_{OUT}$ | 0    | —    | $V_{DD}$ | V    | SOUT                    |

○Not designed for radiation resistance.

## ● Logic circuit diagram



## ● Pin assignments

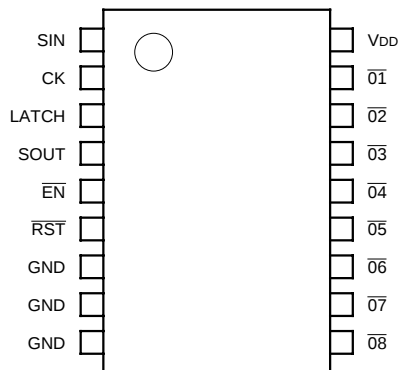


Fig.1

## ●Pin descriptions

| Pin No. | Symbol          | I / O | Function                                                                                                                                                                                             |
|---------|-----------------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1       | SIN             | I     | Serial data input pin                                                                                                                                                                                |
| 2       | CK              | I     | Shift clock for shift register                                                                                                                                                                       |
| 3       | LATCH           | I     | Setting this pin to "L" holds the latch output. While it is "H", latch output changes simultaneously when the shift register output changes.                                                         |
| 4       | SOUT            | O     | This is the output for the final-stage shift register.                                                                                                                                               |
| 5       | EN              | I     | This is the Enable pin for O1 to O8. When this pin is "L", the latch output appears as is.<br>When the output is "H", however, output QN is "L", and when the latch output is "L", Qn becomes High-Z |
| 6       | RST             | I     | Resets the shift register and latch.                                                                                                                                                                 |
| 7       | GND             | —     | 0V power supply                                                                                                                                                                                      |
| 8       | GND             | —     | 0V power supply                                                                                                                                                                                      |
| 9       | GND             | —     | 0V power supply                                                                                                                                                                                      |
| 10      | O8              | O     | Latch output for 8th stage of shift register                                                                                                                                                         |
| 11      | O7              | O     | Latch output for 7th stage of shift register                                                                                                                                                         |
| 12      | O6              | O     | Latch output for 6th stage of shift register                                                                                                                                                         |
| 13      | O5              | O     | Latch output for 5th stage of shift register                                                                                                                                                         |
| 14      | O4              | O     | Latch output for 4th stage of shift register                                                                                                                                                         |
| 15      | O3              | O     | Latch output for 3rd stage of shift register                                                                                                                                                         |
| 16      | O2              | O     | Latch output for 2nd stage of shift register                                                                                                                                                         |
| 17      | O1              | O     | Latch output for 1st stage of shift register                                                                                                                                                         |
| 18      | V <sub>DD</sub> | —     | + V <sub>DD</sub> power supply                                                                                                                                                                       |

Note 1) O1 to O8 are open drain output, and when the shift register output is "H", the output level goes "L".

●Electrical characteristics (unless otherwise noted, Ta = 25°C, V<sub>DD</sub> = 5.0V)

| Parameter                           | Symbol          | Min. | Typ. | Max. | Unit | Conditions                        |
|-------------------------------------|-----------------|------|------|------|------|-----------------------------------|
| Input low level voltage             | V <sub>IL</sub> | 0    | —    | 1.5  | V    | SIN, LATCH, EN                    |
| Input high level voltage            | V <sub>IH</sub> | 3.5  | —    | 5.0  | V    | SIN, LATCH, EN                    |
| Output low level current            | I <sub>SL</sub> | —    | —    | 6    | mA   | SOUT (VL = 0.4)                   |
| Output high level current           | I <sub>SH</sub> | —    | —    | − 6  | mA   | SOUT (VL = V <sub>DD</sub> − 0.4) |
| Schmitt trigger "H" threshold value | V <sub>P</sub>  | 2.31 | —    | 3.28 | V    | CK, RST                           |
| Schmitt trigger "L" threshold value | V <sub>N</sub>  | 1.5  | —    | 2.58 | V    | CK, RST                           |
| Schmitt trigger hysteresis width    | V <sub>H</sub>  | 0.35 | 0.75 | —    | V    | CK, RST                           |
| Output low level voltage            | V <sub>OL</sub> | —    | —    | 0.15 | V    | O1 ~ O8I <sub>D</sub> = 12mA      |
|                                     | V <sub>OL</sub> | —    | —    | 0.4  | V    | O1 ~ O8I <sub>D</sub> = 36mA      |
| Output leakage current              | I <sub>L</sub>  | —    | —    | ± 10 | μA   | —                                 |
| Current dissipation                 | I <sub>DD</sub> | —    | 1    | 100  | μA   | V <sub>DD</sub> or GND            |
| Pull-up resistance                  | R <sub>UP</sub> | 35   | 50   | 68   | kΩ   | —                                 |
| Pull-down resistance                | R <sub>DN</sub> | 35   | 50   | 68   | kΩ   | —                                 |

● Timing characteristics (unless otherwise noted,  $T_a = 25^\circ\text{C}$ ,  $V_{DD} = 5.0\text{V}$ )

| Parameter         | Symbol    | Conditions     | Min. | Typ. | Max. | Unit |
|-------------------|-----------|----------------|------|------|------|------|
| Clock frequency   | f         | Input duty 50% |      |      | 5    | MHz  |
| Clock pulse width | $t_{cw}$  | —              | 100  | —    | —    | ns   |
| Latch pulse width | $t_{rw}$  | —              | 100  | —    | —    | ns   |
| Data setup time   | $t_{su}$  | CK→SIN         | 100  | —    | —    | ns   |
| Data hold time    | $t_h$     | CK→SIN         | 100  | —    | —    | ns   |
| Clock latch time  | $t_{dtl}$ | —              | 100  | —    | —    | ns   |

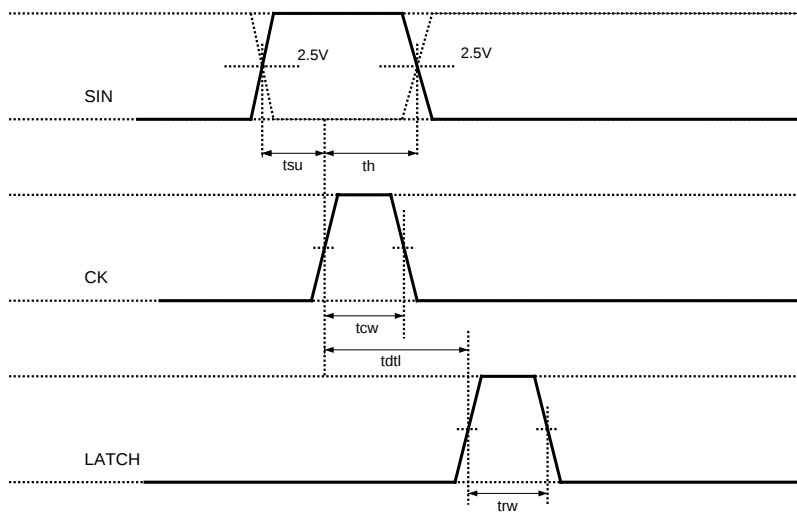
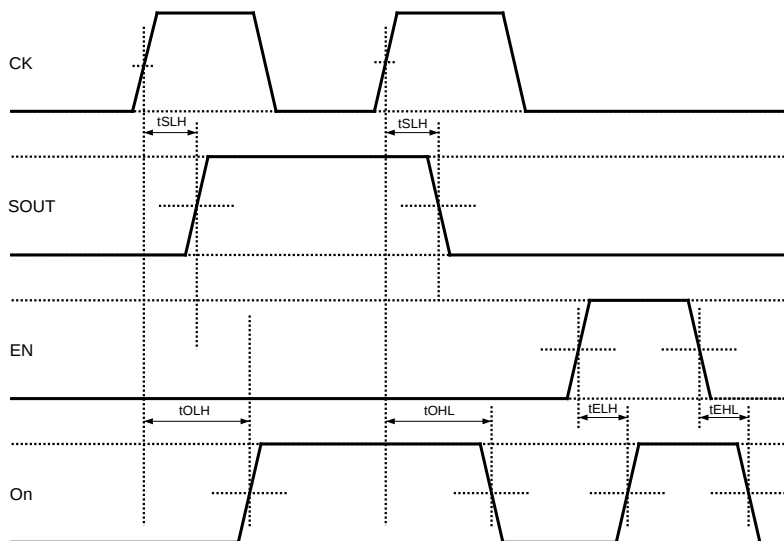


Fig.2 Timing conditions

● Switching characteristics (unless otherwise noted,  $T_a = 25^\circ\text{C}$ ,  $V_{DD} = 5.0\text{V}$ )

| Parameter                                                  | Symbol     | Conditions                                   | Min. | Typ. | Max. | Unit |
|------------------------------------------------------------|------------|----------------------------------------------|------|------|------|------|
| Output "L - H" propagation time<br>Input CK to output SOUT | $t_{SLH}$  | $V_{IH} = 5\text{V}$<br>$V_{IL} = 0\text{V}$ | —    | —    | 100  | ns   |
| Output "H - L" propagation time<br>Input CK to output SOUT | $t_{SPLH}$ |                                              | —    | —    | 100  | ns   |
| Output "L - H" propagation time<br>Input CK to output ON   | $t_{OLH}$  |                                              | —    | —    | 200  | ns   |
| Output "H - L" propagation time<br>Input CK to output ON   | $t_{OHL}$  |                                              | —    | —    | 200  | ns   |
| Output "L - H" propagation time<br>Input EN to output ON   | $t_{ELH}$  |                                              | —    | —    | 100  | ns   |
| Output "H - L" propagation time<br>Input EN to output ON   | $t_{EHL}$  |                                              | —    | —    | 100  | ns   |



Note) Measured with pull-up resistance of  $1.0\text{k}\Omega$  and load of  $20\text{pF}$  applied to terminals O1 to O8.

Fig.3 Switching characteristic

## ●Timing chart

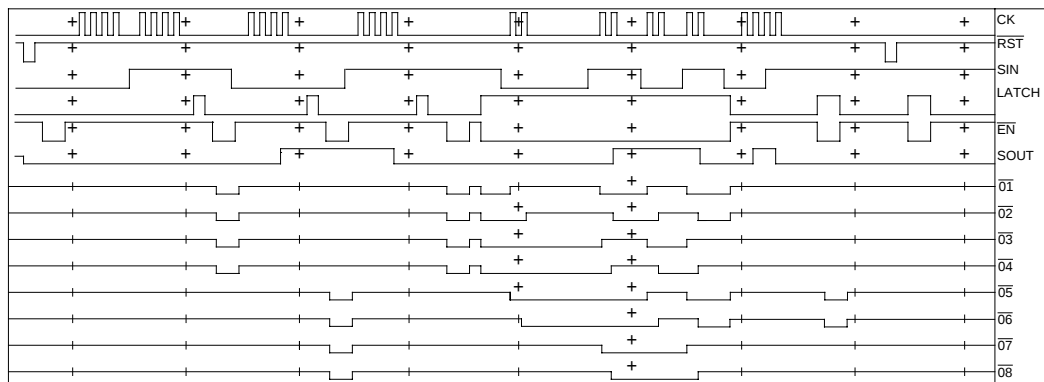


Fig.4

## ●Input / output circuits

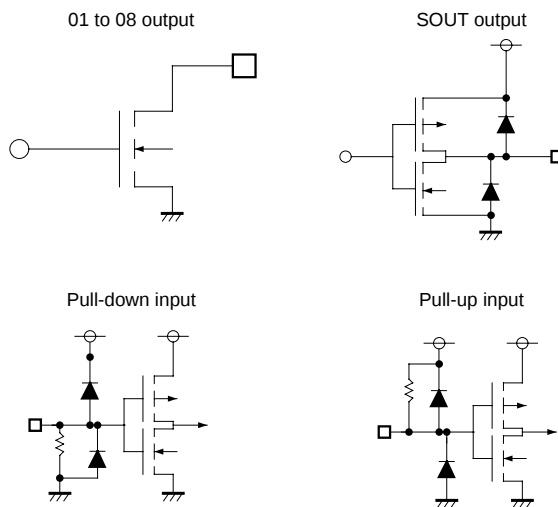


Fig.5

## ●Application example

Expansion port

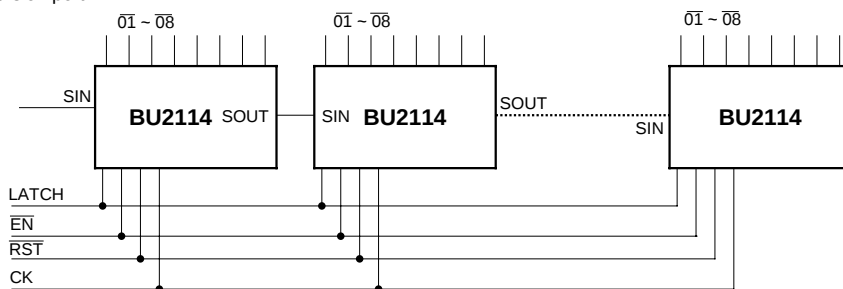
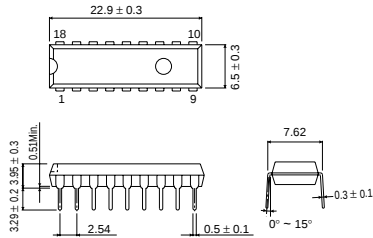


Fig.6

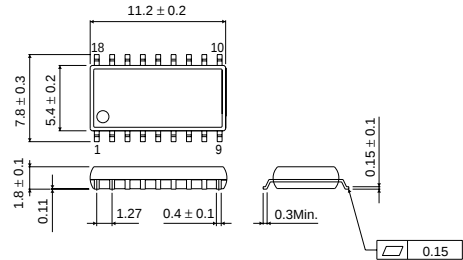
## ● External dimensions (Units: mm)

BU2114



DIP18

BU2114F



SOP18