

STRUCTURE Silicon Monolithic Integrated Circuit

TYPE 8bit Shift Register

PRODUCT SERIES **BU4094BC**
BU4094BCF
BU4094BCFV

FEATURES

- Wide operating power supply range (3[V]~18[V])
- High impedance input

○ ABSOLUTE MAXIMUM RATINGS (Ta=25[°C])

Parameter	Symbol	Limit	Unit
Power Supply Voltage 1	VDD	(VSS-0.5)~(VSS+20.0)	V
Power Supply Voltage 2	VDD	(VSS-0.5)~(VSS+20.0)	V
Power Dissipation	Pd	BU4094BC	1180(*1)(*4)
		BU4094BCF	620(*2)(*4)
		BU4094BCFV	380(*3)(*4)
Supply current	Iin	±10	mA
Operating temperature	Topr	-40~+85	°C
Storage temperature	Tstg	-55~+150	°C
Input Voltage	Vin	(VSS-0.5)~(VDD+0.5)	V
Maximum junction temperature	Tjmax	150	°C

• This product is designed for protection against radioactive rays.

(*1) When used at Ta=25[°C] on above, value of above is reduced 9.0[mW] per 1[°C].

(*2) When used at Ta=25[°C] on above, value of above is reduced 5.0[mW] per 1[°C].

(*3) When used at Ta=25[°C] on above, value of above is reduced 3.1[mW] per 1[°C].

(*4) Power dissipation is the value for mounting 70[mm]×[70mm]×1.6[mm] FR4 glass epoxy circuit board (copper foil area is 3% or less).

○ OPERATING CONDITION (Ta=-40~+85[°C])

Parameter	Symbol	Limit	Unit
Power Supply Voltage	VDD	+3.0~+18.0	V
Input voltage	VIN	0~VDD	V

Status of this document

The Japanese version of this document is the official specification.

This translated version is intended only as a reference, to aid in understanding the official version.

If there are any differences between the original and translated versions of this document, the official Japanese language version takes priority.

○ ELECTRICAL CHARACTERISTICS (unless otherwise noted, VSS=VEE=0[V], Ta=25[°C])

Parameter	Symbol	Standard Value			Unit	VDD[V]	Condition
		MIN	TYP	MAX			
Input "H" voltage	VIH	3.5	—	—	V	5	—
		7.0	—	—	V	10	
		11.0	—	—	V	15	
Input "L" voltage	VIL	—	—	1.5	V	5	—
		—	—	3.0	V	10	
		—	—	4.0	V	15	
Input "H" current	IIH	—	—	0.3	μA	15	VIH=15[V]
Input "L" current	IIL	—	—	-0.3	μA	15	VIL=0[V]
Output "H" voltage	VOH	4.95	—	—	V	5	IO=0[mA]
		9.95	—	—	V	10	
		14.95	—	—	V	15	
Output "L" voltage	VOL	—	—	0.05	V	5	IO=0[mA]
		—	—	0.05	V	10	
		—	—	0.05	V	15	
Output "H" current	IOH	-0.44	—	—	mA	5	VOH=4.6[V]
		-1.1	—	—	mA	10	VOH=9.5[V]
		-3.0	—	—	mA	15	VOH=13.5[V]
Output "L" current	IOL	0.44	—	—	mA	5	VOL=0.4[V]
		1.1	—	—	mA	10	VOL=0.5[V]
		3.0	—	—	mA	15	VOL=1.5[V]
"H" output current (disable)	IDH	—	—	1.0	μA	15	VOUT=15[V]
"L" output current (disable)	IDL	—	—	-1.0	μA	15	VOUT=0[V]
Supply current	IDD	—	—	5	μA	5	VIN=GND or VDD
		—	—	10	μA	10	
		—	5	20	μA	15	
Input capacitance	CIN	—	5	—	pF	—	—

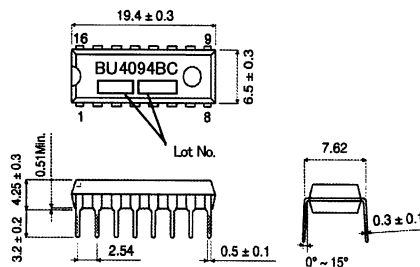
○ Switching Characteristics 1 (unless otherwise noted, Ta=25[°C], VSS=VEE=0[V], RL=10[kΩ], CL=50[pF])

Parameter	Symbol	Standard Value			Unit	VDD[V]	Condition
		MIN	TYP	MAX			
Output rising time	t _{TLH}	—	100	200	ns	5	—
		—	50	100	ns	10	
		—	40	80	ns	15	
Output falling time	t _{THL}	—	100	200	ns	5	—
		—	50	100	ns	10	
		—	40	80	ns	15	
Propagation delay time (CLOCK → Qs)	t _{PLH} t _{PHL}	—	350	600	ns	5	—
		—	125	250	ns	10	
		—	95	190	ns	15	
Propagation delay time (CLOCK → Q's)	t _{PLH} t _{PHL}	—	230	460	ns	5	—
		—	110	220	ns	10	
		—	75	150	ns	15	
Propagation delay time (CLOCK → Qn)	t _{PLH} t _{PHL}	—	420	840	ns	5	—
		—	195	390	ns	10	
		—	135	270	ns	15	
Propagation delay time (STROBE → Qn)	t _{PLH} t _{PHL}	—	290	580	ns	5	—
		—	145	290	ns	10	
		—	100	200	ns	15	
3 state Propagation delay time (OUTPUT ENABLE → Qn)	t _{PHZ} t _{PZH}	—	140	280	ns	5	RL=1[kΩ]
		—	75	150	ns	10	
		—	55	110	ns	15	
3 state Propagation delay time (OUTPUT ENABLE → Qn)	t _{PLZ} t _{PZL}	—	140	280	ns	5	RL=1[kΩ]
		—	75	150	ns	10	
		—	55	110	ns	15	

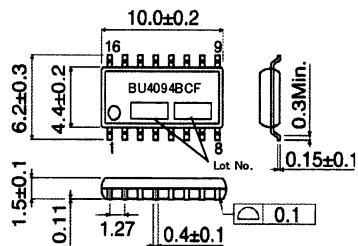
○ Switching Characteristics 2 (unless otherwise noted, Ta=25[°C], VSS=VEE=0[V], RL=10[kΩ], CL=50[pF])

Parameter	Symbol	Standard Value			Unit	VDD[V]	Condition
		MIN	TYP	MAX			
Minimum set up time (DATA → CLOCK)	tSU	—	20	125	ns	5	—
		—	8	55	ns	10	
		—	6	35	ns	15	
Output rising time	tH	—	10	40	ns	5	—
		—	10	20	ns	10	
		—	5	15	ns	15	
Minimum clock pulse width	tW	—	100	200	ns	5	—
		—	50	100	ns	10	
		—	40	80	ns	15	
Minimum clock rising/falling time	tr(CL) tf(CL)	No Limit			μs	5	—
					μs	10	
					μs	15	
Maximum clock frequency	fCL	1.25	5	—	MHz	5	—
		2.5	10	—	MHz	10	
		3.0	12.5	—	MHz	15	
Minimum strobe pulse width	tWH	—	100	200	ns	5	—
		—	40	80	ns	10	
		—	35	70	ns	15	

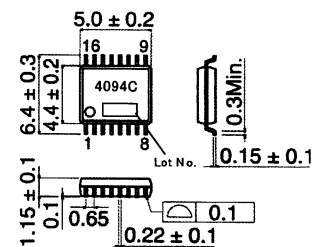
○ PHYSICAL DIMENSIONS



BU4094BC(DIP16)(UNIT:[mm])

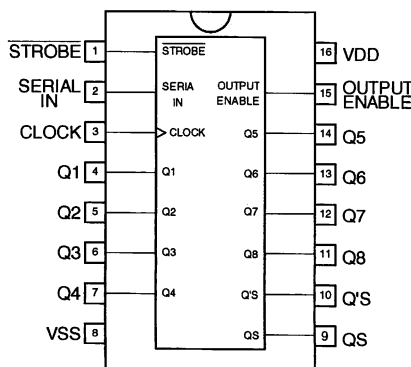


BU4094BCF(SOP16)(UNIT:[mm])

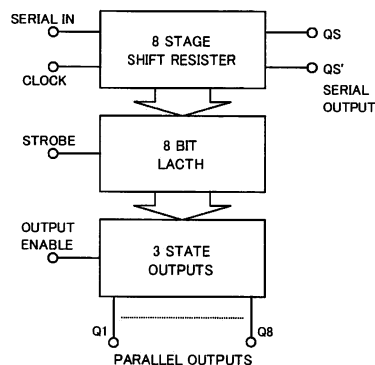


BU4094BCFV(SSOP-B16)(UNIT:[mm])

○ BLOCK DIAGRAM



○ PIN DESCRIPTION



Pin	Pin name
1	A1
2	B1
3	O1
4	O2
5	B2
6	A2
7	VSS
8	A3
9	B3
10	O3
11	O4
12	B4
13	A4
14	VDD

○ NOTES FOR USE

(1) Absolute maximum ratings

Exceeding the absolute maximum ratings, including applied voltage and operating temperature range, may damage or destroy the IC. Since the cause of the damage cannot be conclusively identified (as, for example, a short or open mode), be sure to take appropriate physical safety measures, such as incorporating fuses, whenever a special mode anticipated to exceed absolute maximum ratings is employed.

(2) External voltage at input terminal

VDD+0.3[V], VSS-0.3[V] can be input led without characteristics deterioration and destruction. However the circuit operation is not guaranteed. Please use within recommended operating conditions.

(3) Treatment about input of unused circuit

Redundancy current and oscillation may occur, so untreated input should be connected to VDD or VSS. At connection, it is better to connect resistance (about 100k Ω).

(4) Power Dissipation

If the IC is used out of this power dissipation area, the faulty operation or reduction of current characteristics may occur due to the rise of IC temperature. Also, be sure to Use this IC within a power dissipation range while also allowing enough margins.

(5) Mounting errors

Mounting errors, such as incorrect positioning or orientation, may destroy the device.

(6) Electromagnetic fields

Use in strong electromagnetic fields may cause malfunctions. Be careful operating in electromagnetic fields.

(7) Treatment of IC

Stress (camber, bend etc) may cause characteristic change due to piezo electric effect. Pay attention to stress.

(8) Latch up

Please pay attention to the deterioration and destruction by parasitic element action and latch up that occurs when excessive noise, surge on negatic voltage is loaded at the normal operation.

(9) Test with set PCB

When you connect capacitor to low impedance terminal. You should discharge to avoid stress under IC.

Also at attachment and detachment to jig in testing line, its power supply should be "OFF" .

Moreover for static electricity, please set ground to assembly line, and pong enough attention at conveyance on storage.

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