1.5V Drive Pch MOSFET

RZR040P01

●Structure
Silicon P-channel MOSFET

●Features
1) Low on-resistance.
2) High power package.
3) Low voltage drive. (1.5V)

●Applications
Switching

●Packaging specifications

Type	Package	Taping
	Code	TL
	Basic ordering unit (pieces)	3000
RZR040P01		◯

●Absolute maximum ratings (Ta=25°C)

Parameter		Symbol	Limits	Unit
Drain-source voltage		V_{DSS}	−12	V
Gate-source voltage		V_{GSS}	±10	V
Drain current	Continuous	I_D	±4	A
	Pulsed	I_{DP} ∗1	±16	A
Source current (Body diode)	Continuous	I_S	−0.8	A
	Pulsed	I_{SP} ∗1	−16	A
Total power dissipation		P_D ∗2	1.0	W
Channel temperature		Tch	150	°C
Range of Storage temperature		Tstg	−55 to +150	°C

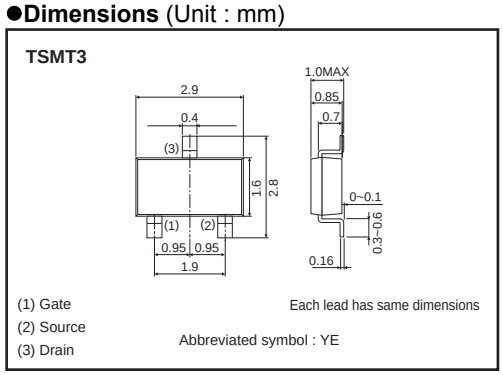
∗1 Pw≤10μs, Duty cycle≤1%
∗2 When mounted on a ceramic board

●Thermal resistance

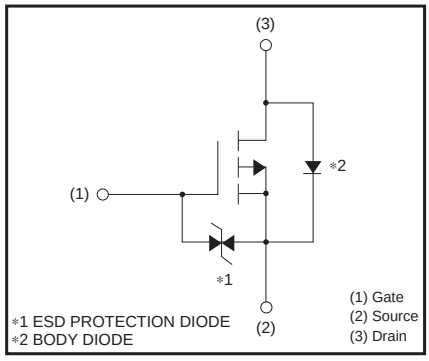
Parameter	Symbol	Limits	Unit
Channel to ambient	Rth(ch-a) ∗	125	°C / W

∗ When mounted on a ceramic board.

●Dimensions (Unit : mm)



●Inner circuit



●Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	–	–	±10	μA	V_{GS}=±10V, V_{DS}=0V
Drain-source breakdown voltage	$V_{(BR)\ DSS}$	–12	–	–	V	I_D= –1mA, V_{GS}=0V
Zero gate voltage drain current	I_{DSS}	–	–	–1	μA	V_{DS}= –12V, V_{GS}=0V
Gate threshold voltage	$V_{GS\ (th)}$	–0.3	–	–1.0	V	V_{DS}= –6V, I_D= –1mA
Static drain-source on-state resistance	$R_{DS\ (on)}$ *	–	22	30	mΩ	I_D= –4A, V_{GS}= –4.5V
		–	30	42	mΩ	I_D= –2A, V_{GS}= –2.5V
		–	40	60	mΩ	I_D= –2A, V_{GS}= –1.8V
		–	55	110	mΩ	I_D= –0.8A, V_{GS}= –1.5V
Forward transfer admittance	$\|Y_{fs}\|$ *	6.5	–	–	S	V_{DS}= –6V, I_D= –4A
Input capacitance	C_{iss}	–	2350	–	pF	V_{DS}= –6V
Output capacitance	C_{oss}	–	310	–	pF	V_{GS}=0V
Reverse transfer capacitance	C_{rss}	–	280	–	pF	f=1MHz
Turn-on delay time	$t_{d\ (on)}$ *	–	11	–	ns	V_{DD}≒ –6V I_D= –2A V_{GS}= –4.5V R_L≒ 3Ω R_G=10Ω
Rise time	t_r *	–	70	–	ns	
Turn-off delay time	$t_{d\ (off)}$ *	–	380	–	ns	
Fall time	t_f *	–	210	–	ns	
Total gate charge	Q_g *	–	30	–	nC	V_{DD}≒ –6V R_L≒1.5Ω I_D= –4A R_G=10Ω V_{GS}= –4.5V
Gate-source charge	Q_{gs} *	–	4.0	–	nC	
Gate-drain charge	Q_{gd} *	–	3.5	–	nC	

*Pulsed

●Body diode characteristics (Source-drain) (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V_{SD} *	–	–	–1.2	V	I_S= –4A, V_{GS}=0V

*Pulsed

●Electrical characteristics curves

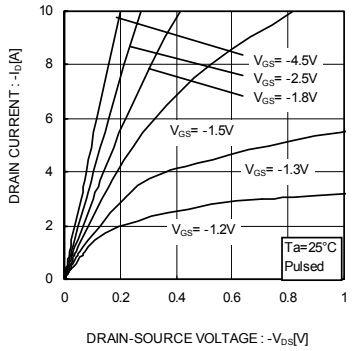


Fig.1 Typical output characteristics(Ⅰ)

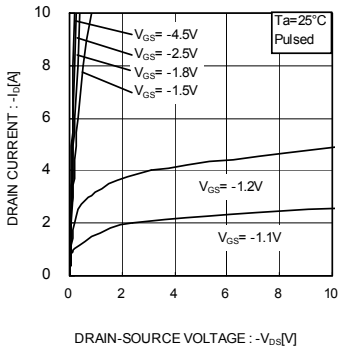


Fig.2 Typical output characteristics(Ⅱ)

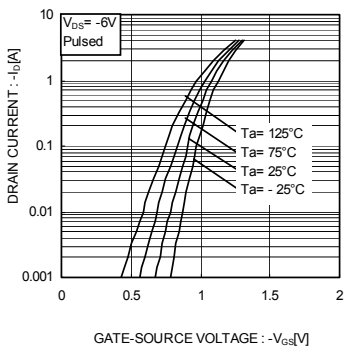


Fig.3 Typical Transfer Characteristics

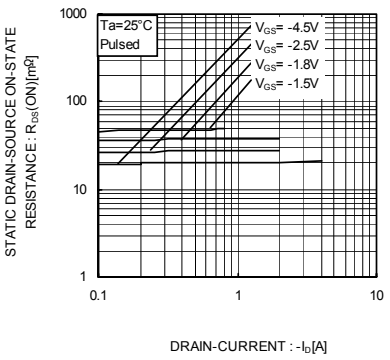


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current(Ⅰ)

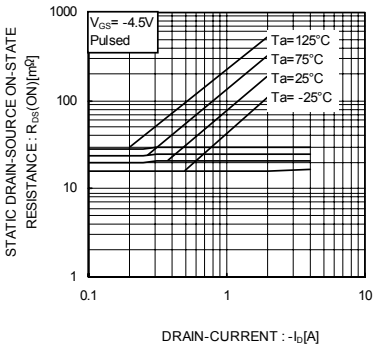


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current(Ⅱ)

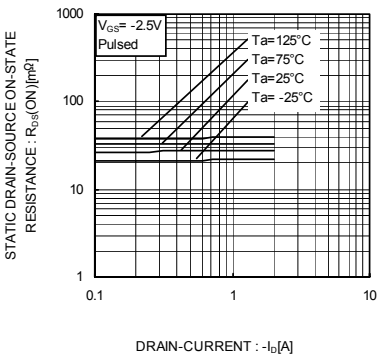


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current(Ⅲ)

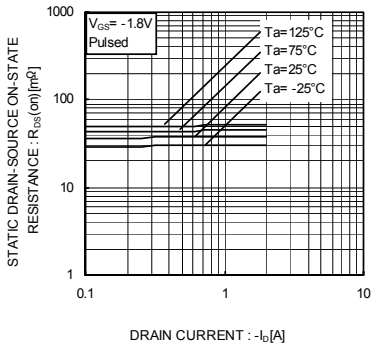


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current(Ⅳ)

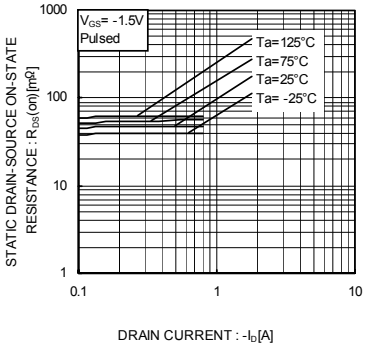


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current(Ⅴ)

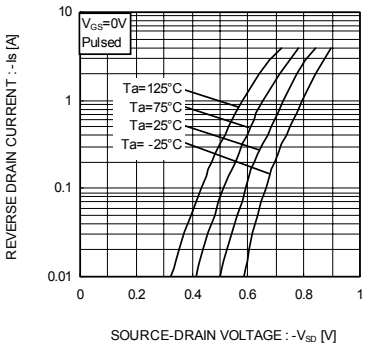


Fig.9 Reverse Drain Current vs. Sourse-Drain Voltage

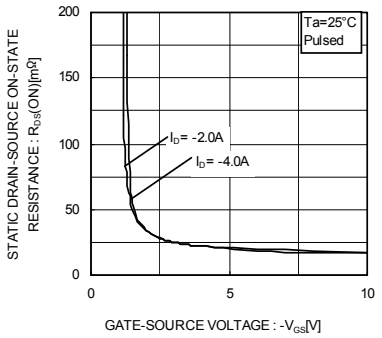


Fig.10 Static Drain-Source On-State Resistance vs. Gate Source Voltage

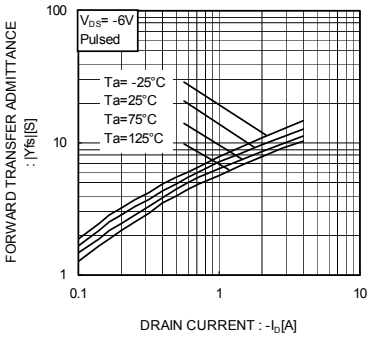


Fig.11 Forward Transfer Admittance vs. Drain Current

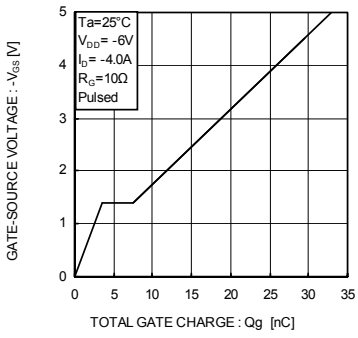


Fig.12 Dynamic Input Characteristics

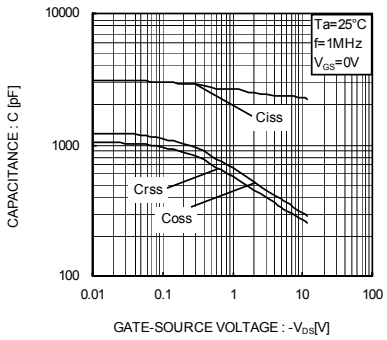


Fig.13 Typical Capacitance vs. Drain-Source Voltage

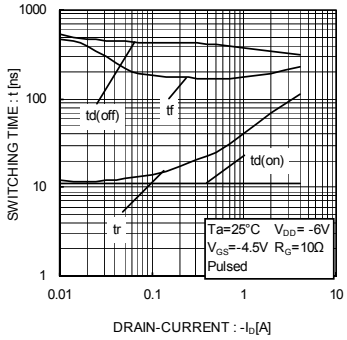


Fig.14 Switching Characteristics

●Measurement circuits

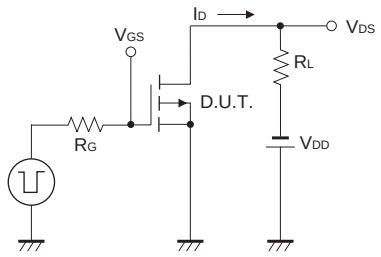


Fig.1-1 Switching Time Measurement Circuit

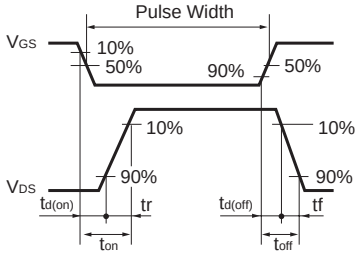


Fig.1-2 Switching Waveforms

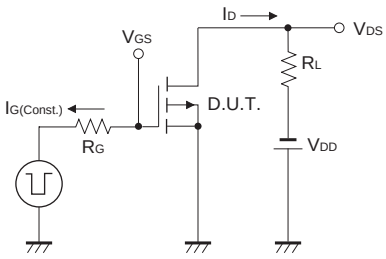


Fig.2-1 Gate Charge Measurement Circuit

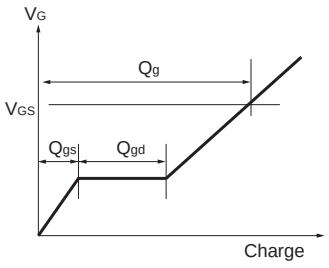


Fig.2-2 Gate Charge Waveform

●Notice

This product might cause chip aging and breakdown under the large electrified environment.
Please consider to design ESD protection circuit.

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