

# 4V Drive Nch+Pch MOS FET

## SP8M8

●Structure

Silicon N-channel / P-channel MOS FET

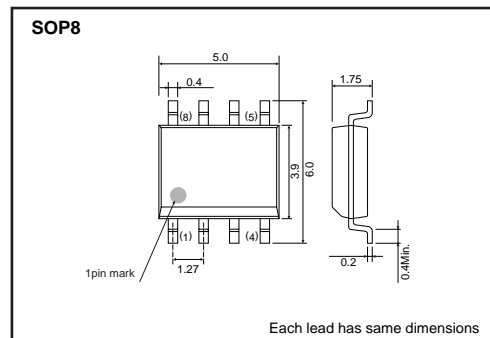
●Features

- 1) Low on-resistance.
- 2) Built-in G-S Protection Diode.
- 3) Small Surface Mount Package (SOP8).

●Application

Power switching, DC / DC converter.

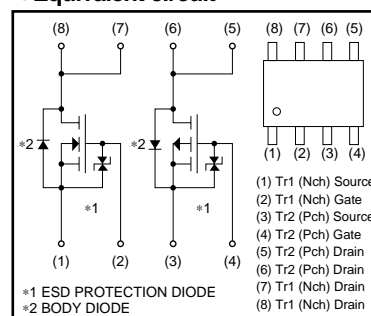
●External dimensions (Unit : mm)



●Packaging specifications

Type	Package	Taping
	Code	TB
	Basic ordering unit (pieces)	2500
SP8M8		○

●Equivalent circuit



\*1 A protection diode is included between the gate and the source terminals to protect the diode against static electricity when the product is in use. Use the protection circuit when the fixed voltages are exceeded.

●Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits		Unit	
		Nchannel	Pchannel		
Drain-source voltage	$V_{DSS}$	30	-30	V	
Gate-source voltage	$V_{GSS}$	20	-20	V	
Drain current	Continuous	$I_D$	$\pm 6.0$	$\pm 4.5$	A
	Pulsed	$I_{DP}^{*1}$	$\pm 24$	$\pm 18$	A
Source current (Body diode)	Continuous	$I_S$	1.6	-1.6	A
	Pulsed	$I_{SP}^{*1}$	20	-18	A
Total power dissipation	$P_D^{*2}$	2		W	
Channel temperature	$T_{ch}$	150		°C	
Storage temperature	$T_{stg}$	-55 to +150		°C	

\*1  $P_w \leq 10\mu s$ , Duty cycle  $\leq 1\%$

\*2 MOUNTED ON A CERAMIC BOARD.

●Thermal resistance

Parameter	Symbol	Limits	Unit
Channel to ambient	$R_{th}(ch-a)^*$	62.5	°C / W

\*MOUNTED ON A CERAMIC BOARD.

## Transistors

## N-ch

## ●Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I <sub>GSS</sub>	–	–	10	μA	V <sub>GS</sub> =20V, V <sub>DS</sub> =0V
Drain-source breakdown voltage	V <sub>(BR) DSS</sub>	30	–	–	V	I <sub>D</sub> =1mA, V <sub>GS</sub> =0V
Zero gate voltage drain current	I <sub>DSS</sub>	–	–	1	μA	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V
Gate threshold voltage	V <sub>GS(th)</sub>	1.0	–	2.5	V	V <sub>DS</sub> =10V, I <sub>D</sub> =1mA
Static drain-source on-state resistance	R <sub>DS(on)</sub> *	–	21	30	mΩ	I <sub>D</sub> =6.0A, V <sub>GS</sub> =10V
		–	30	42		I <sub>D</sub> =6.0A, V <sub>GS</sub> =4.5V
		–	33	47		I <sub>D</sub> =6.0A, V <sub>GS</sub> =4V
Forward transfer admittance	Y <sub>fs</sub>  *	4.0	–	–	S	I <sub>D</sub> =6.0A, V <sub>DS</sub> =10V
Input capacitance	C <sub>iss</sub>	–	520	–	pF	V <sub>DS</sub> =10V
Output capacitance	C <sub>oss</sub>	–	150	–	pF	V <sub>GS</sub> =0V
Reverse transfer capacitance	C <sub>rss</sub>	–	95	–	pF	f=1MHz
Turn-on delay time	t <sub>d(on)</sub> *	–	9	–	ns	I <sub>D</sub> =3A, V <sub>DD</sub> ≐15V
Rise time	t <sub>r</sub> *	–	21	–	ns	V <sub>GS</sub> =10V
Turn-off delay time	t <sub>d(off)</sub> *	–	36	–	ns	R <sub>L</sub> =5.0Ω
Fall time	t <sub>f</sub> *	–	13	–	ns	R <sub>G</sub> =10Ω
Total gate charge	Q <sub>g</sub> *	–	7.2	–	nC	V <sub>DD</sub> ≐15V
Gate-source charge	Q <sub>gs</sub> *	–	1.8	–	nC	V <sub>GS</sub> =5V
Gate-drain charge	Q <sub>gd</sub> *	–	2.8	–	nC	I <sub>D</sub> =6.0A

\*Pulsed

## ●Body diode characteristics (Source-Drain) (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V <sub>SD</sub> *	–	–	1.2	V	I <sub>S</sub> =6.4A, V <sub>GS</sub> =0V

\*Pulsed

## Transistors

## P-ch

## ●Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I <sub>GSS</sub>	–	–	–10	μA	V <sub>GS</sub> = –20V, V <sub>DS</sub> =0V
Drain-source breakdown voltage	V <sub>(BR) DSS</sub>	–30	–	–	V	I <sub>D</sub> = –1mA, V <sub>GS</sub> =0V
Zero gate voltage drain current	I <sub>DSS</sub>	–	–	–1	μA	V <sub>DS</sub> = –30V, V <sub>GS</sub> =0V
Gate threshold voltage	V <sub>GS(th)</sub>	–1.0	–	–2.5	V	V <sub>DS</sub> = –10V, I <sub>D</sub> = –1mA
Static drain-source on-state resistance	R <sub>DS(on)</sub> *	–	40	56	mΩ	I <sub>D</sub> = –4.5A, V <sub>GS</sub> = –10V
		–	57	80		I <sub>D</sub> = –2.5A, V <sub>GS</sub> = –4.5V
		–	65	90		I <sub>D</sub> = –2.5A, V <sub>GS</sub> = –4.0V
Forward transfer admittance	Y <sub>fs</sub>   *	3.5	–	–	S	I <sub>D</sub> = –2.5A, V <sub>DS</sub> = –10V
Input capacitance	C <sub>iss</sub>	–	850	–	pF	V <sub>DS</sub> = –10V
Output capacitance	C <sub>oss</sub>	–	190	–	pF	V <sub>GS</sub> =0V
Reverse transfer capacitance	C <sub>rss</sub>	–	120	–	pF	f=1MHz
Turn-on delay time	t <sub>d(on)</sub> *	–	10	–	ns	I <sub>D</sub> = –2.5A, V <sub>DD</sub> ≐ –15V
Rise time	t <sub>r</sub> *	–	25	–	ns	V <sub>GS</sub> = –10V
Turn-off delay time	t <sub>d(off)</sub> *	–	60	–	ns	R <sub>L</sub> =6.0Ω
Fall time	t <sub>f</sub> *	–	25	–	ns	R <sub>G</sub> =10Ω
Total gate charge	Q <sub>g</sub> *	–	8.5	–	nC	V <sub>DD</sub> ≐ –15V
Gate-source charge	Q <sub>gs</sub> *	–	2.5	–	nC	V <sub>GS</sub> = –5V
Gate-drain charge	Q <sub>gd</sub> *	–	3.0	–	nC	I <sub>D</sub> = –4.5A

\*Pulsed

## ●Body diode characteristics (Source-Drain) (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V <sub>SD</sub>	–	–	–1.2	V	I <sub>S</sub> = –1.6A, V <sub>GS</sub> =0V

Transistors

N-ch

●Electrical characteristic curves

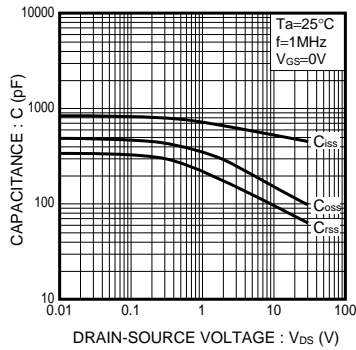


Fig.1 Typical Capacitance vs. Drain-Source Voltage

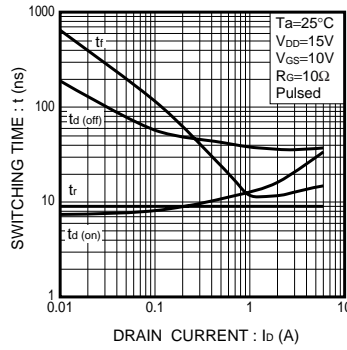


Fig.2 Switching Characteristics

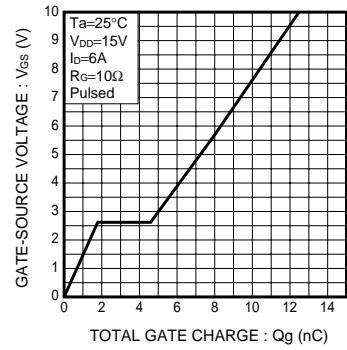


Fig.3 Dynamic Input Characteristics

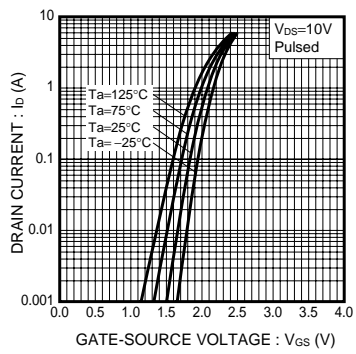


Fig.4 Typical Transfer Characteristics

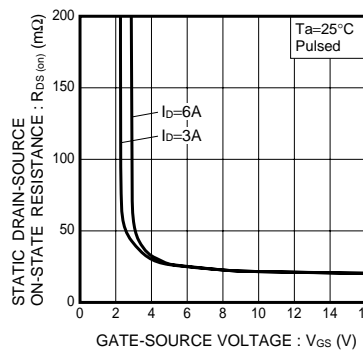


Fig.5 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

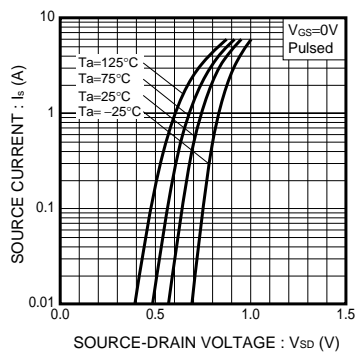


Fig.6 Source Current vs. Source-Drain Voltage

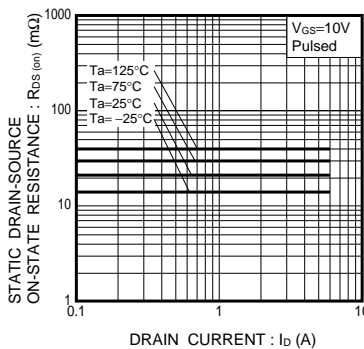


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current (I)

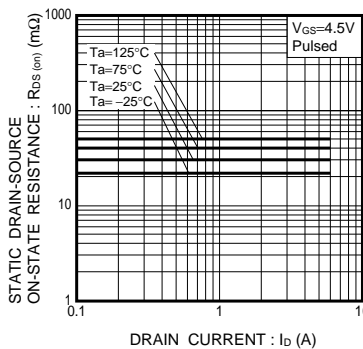


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current (II)

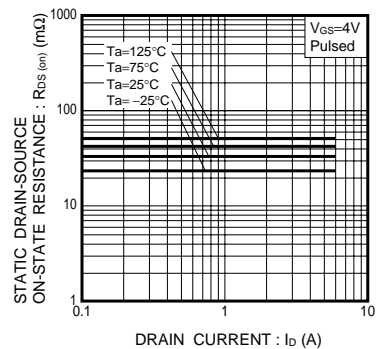


Fig.9 Static Drain-Source On-State Resistance vs. Drain Current (III)

Transistors

P-ch

●Electrical characteristic curves

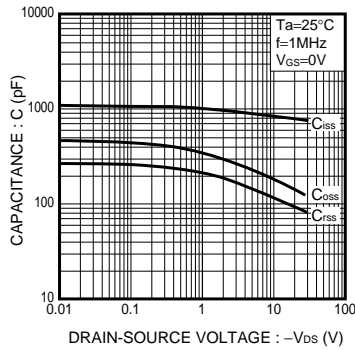


Fig.1 Typical Capacitance vs. Drain-Source Voltage

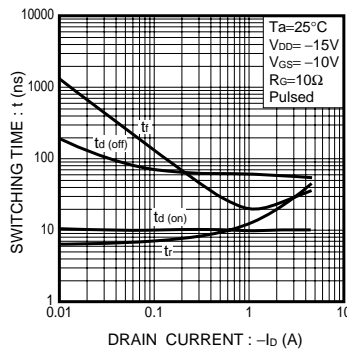


Fig.2 Switching Characteristics

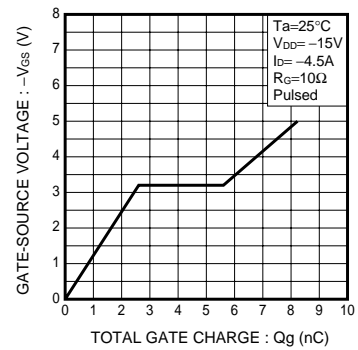


Fig.3 Dynamic Input Characteristics

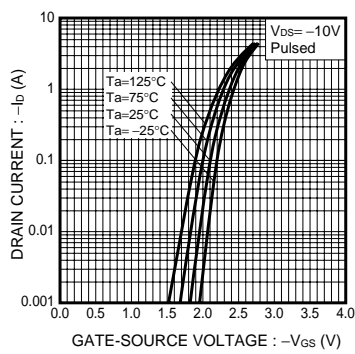


Fig.4 Typical Transfer Characteristics

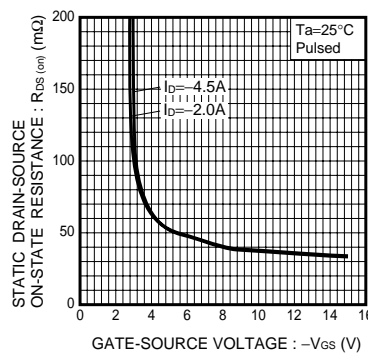


Fig.5 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

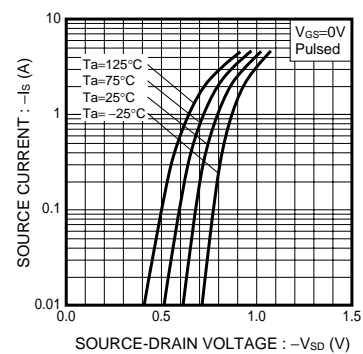


Fig.6 Source Current vs. Source-Drain Voltage

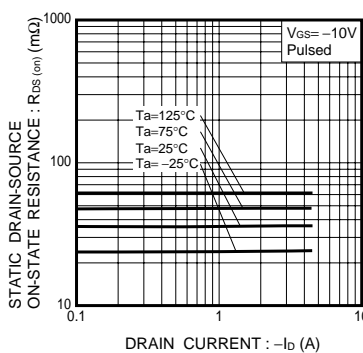


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current (I)

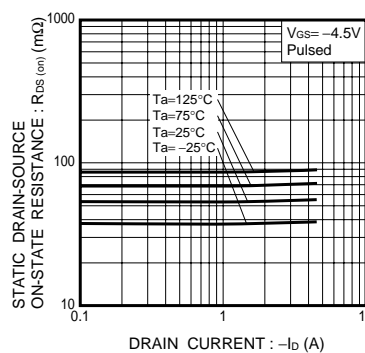


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current (II)

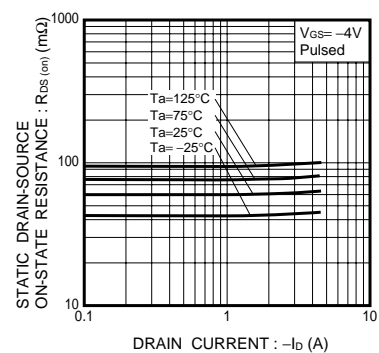


Fig.9 Static Drain-Source On-State Resistance vs. Drain Current (III)

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