

600 V High Voltage High and Low Side Gate Driver

BS2114F

Contents

1. Product summary	2
1.1 Applications.....	2
1.2 Series line-up	2
1.3 Functions and features	2
1.4 Block diagram	2
2. Specifications	3
2.1 Details of absolute maximum rating	3
2.2 Protection function and operation sequence	4
2.2.1 Under voltage lock out (UVLO) circuit for control supply voltage	4
2.3 Package	5
2.3.1 Outer dimensions drawing	5
2.3.2 Terminal configuration	6
3. Applications	7
3.1 Example of practical application circuit (IGBT output stage)	7
3.2 Selection method of application components (refer to Figure 3.1.1)	8
3.2.1 Bootstrap circuit (VB terminal).....	8
3.2.2 Design method for output gate resistance	12
3.2.3 VCC terminal (V _{CC})	17
3.2.4 Power supply for external power element.....	17
3.2.5 Control input terminal (HIN, LIN).....	18
3.2.6 COM terminal	18
3.2.7 Shunt resistor	19
3.3 Notes for PCB pattern designing including the power elements.....	20
3.4 Snubber capacitor connection.....	21

1. Product summary

1.1 Applications

- Application for driving N-channel MOSFET and IGBT

1.2 Series line-up

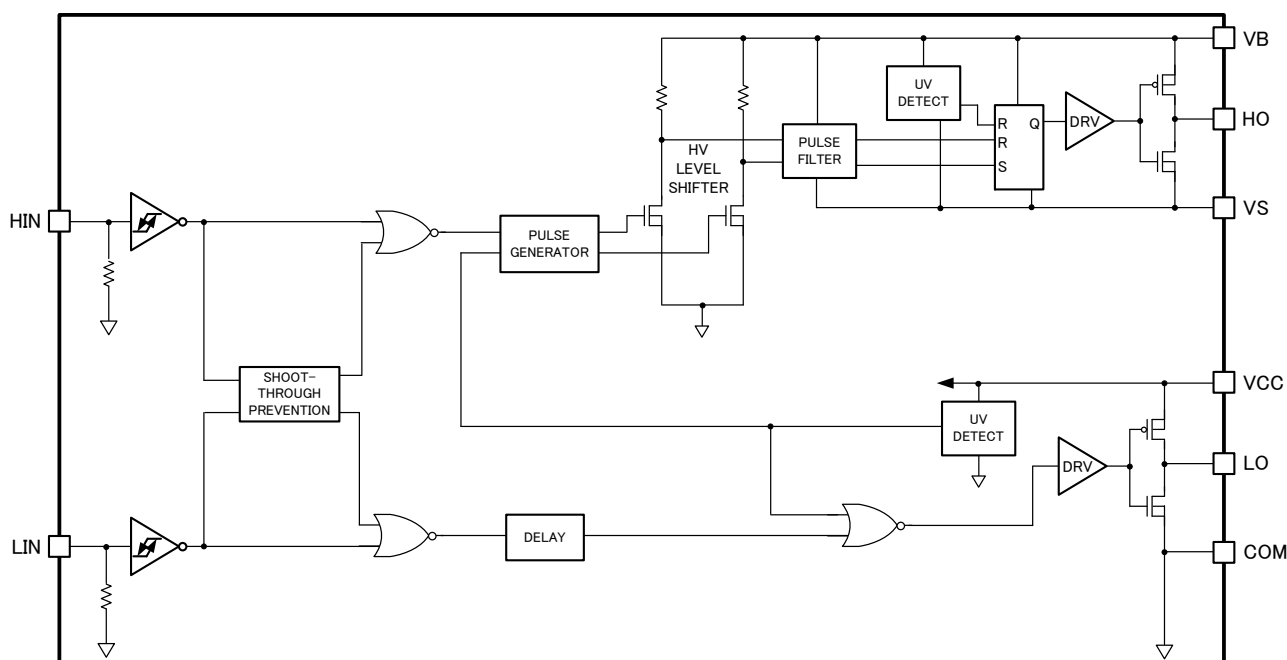
Table 1.2.1 Line-up

Series	Model	Absolute maximum rating	VCC recommended operating range	Output stage capacity (min) (source/sink)	Protection function	Dead time (typ)	Package
6 ch (3 arms)	BS2130F-G	625V/25V	11.5 – 20V	120mA/250mA	UVLO, OCP	300ns	SOP-28
2 ch (1 arm)	BS2101F	620V/20V	10 – 18V	60mA/130mA	UVLO	–	SOP-8
	BS2103F	620V/20V	10 – 18V	60mA/130mA	UVLO	160ns	SOP-8
	BS2114F	625V/25V	10–20V	500mA/500mA	UVLO	160ns	SOP-8

1.3 Functions and features

- Floating terminal withstanding voltage: Up to 600 V
- Gate driver voltage range: 10 V to 20 V
- SOI (silicon on insulator) process is employed
- Under voltage lock out (UVLO) circuit is installed for the supply voltage on the upper drive (voltage between the VB and VS terminals) and the supply voltage on the lower drive (voltage between the VCC and COM terminals)
- Logic voltage of 3.3 V or 5.0 V can be input
- Output common-mode for input signal

1.4 Block diagram



2. Specifications

2.1 Details of absolute maximum rating

Table 2.1.1 provides details of the absolute maximum ratings.

Table 2.1.1 Absolute maximum rating (Unless specified otherwise, Ta = 25°C and COM is set to the reference at 0 V.)

Item	Symbol	Rating (Min)	Rating (Max)	Unit	Description
High side offset voltage	V _S	V _B -25	V _B +0.3	V	Maximum voltage between the VB and VS terminals
High side floating supply voltage	V _B	-0.3	+625V	V	Maximum voltage between the VB and COM terminals
High side floating output voltage HO	V _{HO}	V _S -0.3	V _B +0.3	V	Maximum voltage for the HO terminal
Low side and logic fixed supply voltage(VCC vs. COM)	V _{CC}	-0.3	+25	V	Maximum voltage that can be applied between the VCC and COM terminals
Low side output voltage LO (LO vs COM)	V _{LO}	-0.3	V _{CC} +0.3	V	Maximum voltage between the COM and LO terminals
Logic input voltage(HIN, LIN)	V _{IN}	-0.3	V _{CC} +0.3	V	Input voltage of the logic signal
Logic ground	Com	V _{CC} -25	V _{CC} +0.3	V	Maximum voltage for the COM terminal
Allowable offset voltage SLEW RATE	dV _S /dt	—	50	V/ns	Maximum slew rate for the VS terminal
Junction temperature	T _{jmax}	—	150	°C	Maximum allowable junction temperature of the chip
Storage temperature	T _{stg}	-55	+150	°C	LSI storage temperature

2.2 Protection function and operation sequence

2.2.1 Under voltage lock out (UVLO) circuit for control supply voltage

Reduction in the control supply voltage (voltage between the VB and VS terminals or between the VCC and COM terminals) decreases the “High” voltage of the HO and LO terminals that is the gate driving voltage for external power elements. As a result, the gate voltage of the external power elements is reduced, causing problems such as insufficient capacity. Therefore, keep the supply voltage within the recommended range. When the control supply voltage is reduced below a specified voltage, the under voltage lock out (UVLO) circuit for the control supply voltage is activated.

The UVLO circuits are installed for both the upper driving supply voltage on the VB terminal (voltage between the VB and VS terminals) and for the lower control supply voltage V_{CC} (voltage between the VCC and COM terminals).

■ Operation sequence of under voltage lock out (UVLO) circuit for the control supply voltage input V_{CC}

- The protection is activated when V_{CC} is reduced to V_{CCUV-} .
- The LO terminal on the lower phase changes to “Low” (power elements are turned OFF), and the HO terminal on the upper phase changes to “Low”.
- When V_{CC} returns to V_{CCUV+} , the protection is released.
- When the protection is released, an output logic is output according to the input signal.

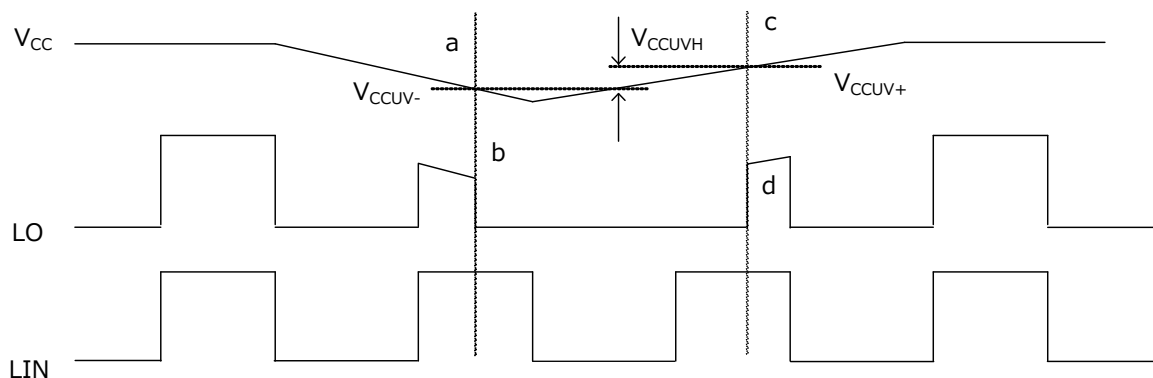


Figure 2.2.1 Timing chart of V_{CC} UVLO

■ Operation sequence of under voltage lock out (UVLO) circuit for the VB control supply voltage

- The protection is activated when V_{BS} (voltage between the VB and VS terminals) is reduced to V_{BSUV-} .
- The HO terminal on the upper phase changes to “Low” (power elements are turned OFF).
- When V_{BS} returns to V_{BSUV+} , the protection is released.
- Even when the protection is released, a “High” output logic is not output until a rising edge of the input signal arrives.
- After the protection is released, a “High” output logic is output when a rising edge of the input signal arrives.

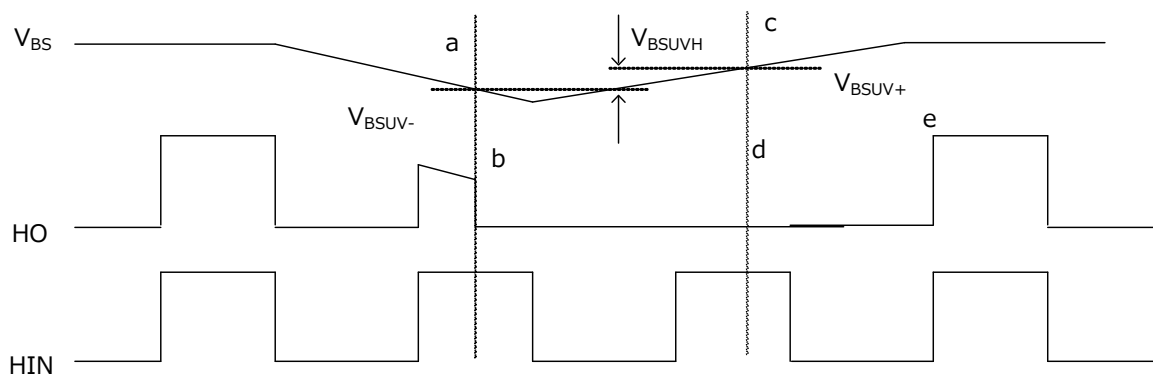


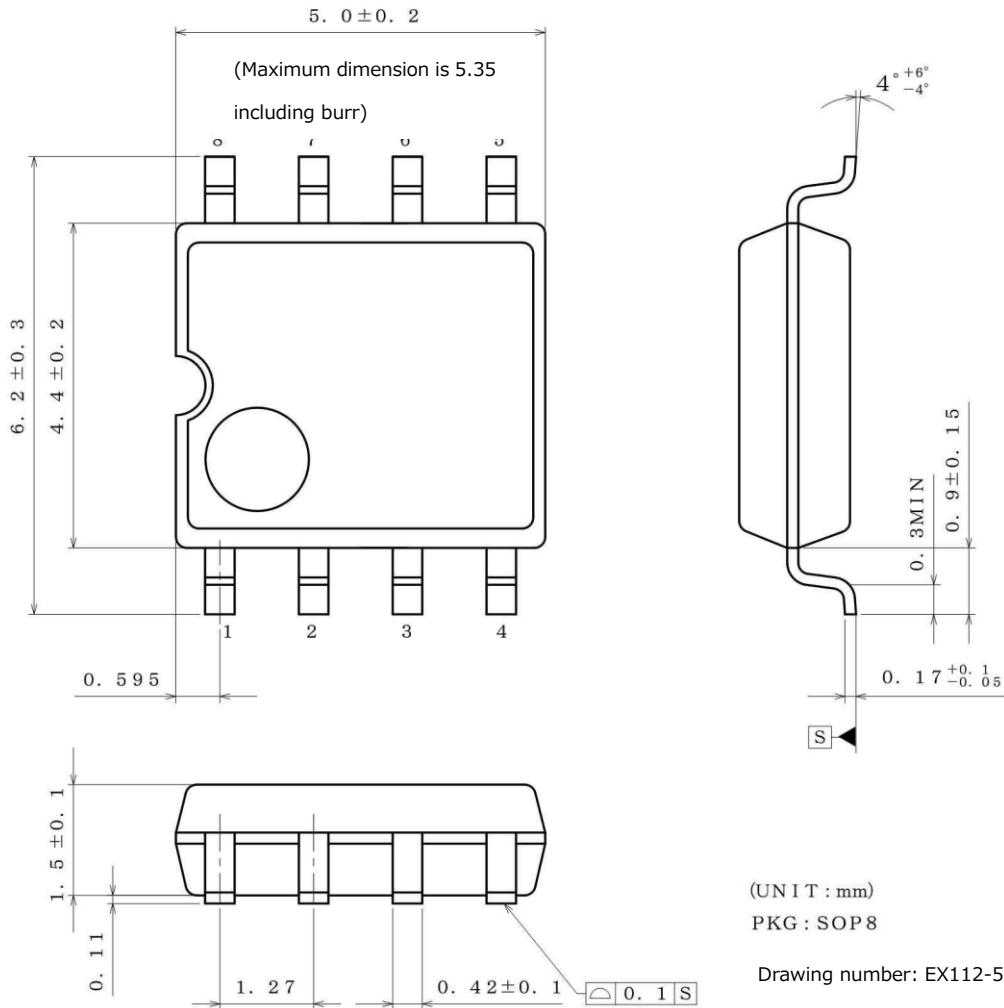
Figure 2.2.2 Timing chart of V_{BS} UVLO

2.3 Package

The SOP8 package is employed.

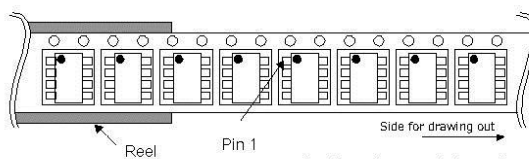
2.3.1 Outer dimensions drawing

Package Name	SOP8
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Package specifications

Packaging type	Embossed taping
Number of packages	2500pcs
Packaging direction	E2 (direction in which pin 1 of the product is located on the upper left when you hold the reel in your left hand and draw out the tape with your right hand)



Note: Please place your order in quantities that are multiples of the number of packages.

2.3.2 Terminal configuration

Table 2.3.1 Terminal descriptions

Pin No.	Symbol	Function
1	LIN	Logic input for low side gate driver output
2	HIN	Logic input for high side gate driver output
3	VCC	Low side supply voltage
4	COM	Low side return
5	LO	Low side gate drive output
6	VS	High side floating supply return
7	HO	High side gate drive output
8	VB	High side floating supply

3. Applications

3.1 Example of practical application circuit (IGBT output stage)

In this example of an application circuit, a three-phase inverter is configured.

The circuit design also considers external components for handling phenomena (or problems) that occur in the actual equipment.

Since some of the components included may be unnecessary in the actual equipment, an evaluation should be performed using a finalized actual set to optimize the circuit design.

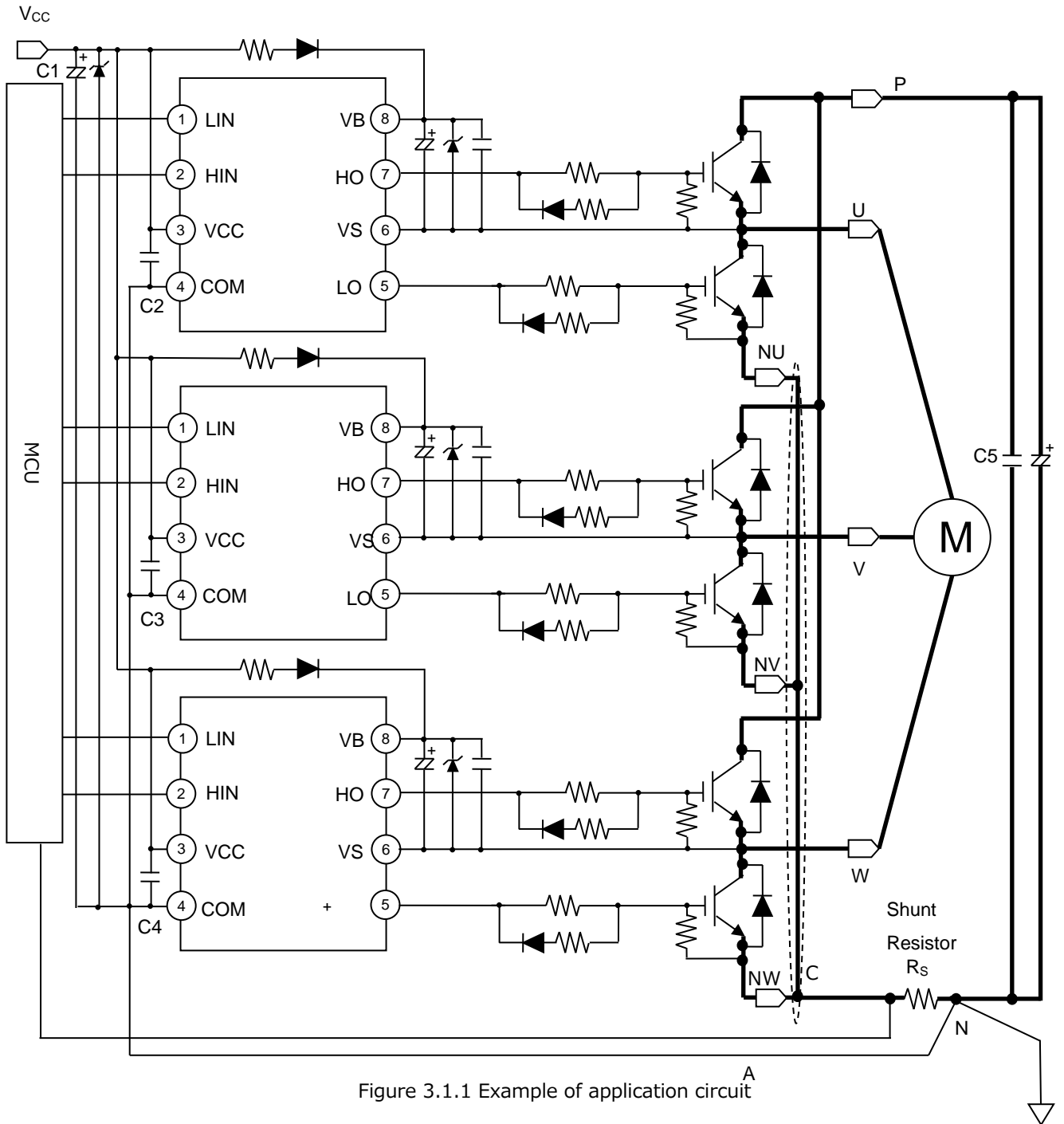


Figure 3.1.1 Example of application circuit

- When the wiring of C is too long, the output may be short-circuited.

3.2 Selection method of application components (refer to Figure 3.1.1)

3.2.1 Bootstrap circuit (VB terminal)

By creating a floating power supply with a bootstrap circuit, you can obtain the four independent power supplies that are normally necessary for driving an inverter (power supplies for driving the upper power elements in three phases and for driving the lower power elements) from a single V_{CC} power supply.

Installing an external bootstrap capacitor (C_{BS}) allows you to configure a bootstrap circuit (Figure 3.2.1). C_{BS} functions as a power supply, providing the upper power element driving current and the upper gate drive supply current. Electric charges consumed for driving the circuit are charged into C_{BS} from the V_{CC} power supply through the BSD, when the potential of the VS terminal (external output terminal for each phase) is reduced to near the ground level. Depending on the driving methods, the capacitance value of C_{BS} , or other factors, the electric charge may not be charged adequately, reducing the C_{BS} potential. This can lead to deterioration of losses in the power elements, heating, or activation of the UVLO. Therefore, the circuit constants such as the capacitance value of C_{BS} should be determined based on a detailed evaluation on the actual equipment.

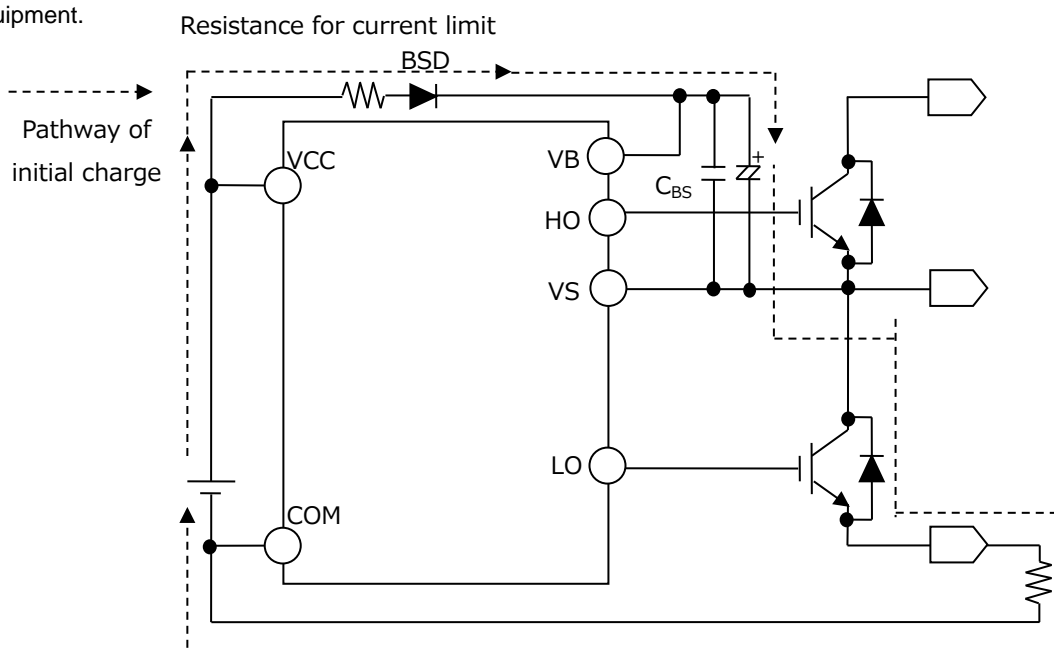


Figure 3.2.1 Bootstrap circuit (with IGBT power element, simplified single phase)

■ Initial charge

When you use a bootstrap circuit, it is necessary to charge C_{BS} in advance before starting the circuit. Normally, C_{BS} is charged by turning ON all phases of the lower power element. When a motor load is connected, the charging may be performed via the motor winding by turning on only one phase. However, it should be noted that the charging efficiency is reduced due to the resistance in the motor winding and wiring.

The initial charge can be performed using two methods: single pulse method (Figure 3.2.2) and multiple ON pulses method when there is a limitation such as the supply capacity of the 15 V control power supply (Figure 3.2.3). The time required for the initial charge depends on the capacitance of C_{BS} and the resistance for the current limit. Therefore, you should secure an adequate charge time according to the capacitance value of C_{BS} , based on a detailed evaluation on the actual equipment.

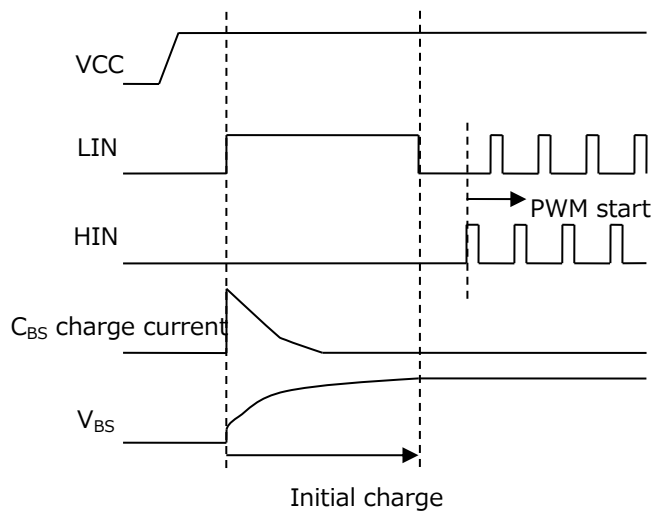


Figure 3.2.2 Initial charge sequence with a single pulse

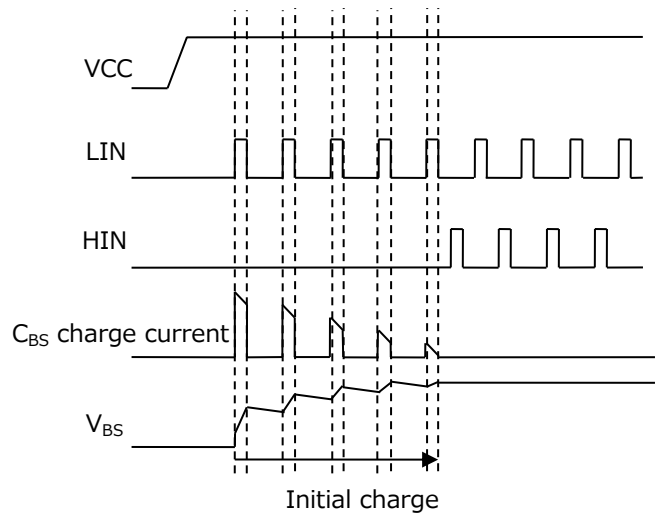


Figure 3.2.3 Initial charge sequence with multiple pulses

■ Design method of bootstrap capacitor C_{BS}

For capacitors to be used in bootstrap circuits, we recommend ceramic capacitors with low ESR in order to reduce a ripple voltage. When the capacitance of a ceramic capacitor is insufficient, connect an electrolytic capacitor in parallel to the ceramic capacitor.

The size of the bootstrap capacitor is determined by the value of the voltage drop and the total amount of supplied charges.

The minimum voltage drop ΔV_{BS} that can turn ON power devices on the high side is determined by the following equation.

$$\Delta V_{BS} = V_{CC} - V_F - V_{GEMIN} - V_{OL} - V_{RS} \quad (3.2.1)$$

V_{CC} : Supply voltage for the gate driver

V_F : Forward voltage drop in the bootstrap diode

V_{GEMIN} : Minimum voltage between the gate and emitter that can keep the upper side power elements ON

V_{OL} : ON voltage for the lower side power elements

V_{RS} : Voltage between the current detection resistances

In addition, total charge amount Q_{Total} is determined by the following equation.

$$Q_{Total} = Q_G + (I_{LKGS} + I_{LK} + I_{LKDIO} + I_{QBS}) \times T_{HON} \quad (3.2.2)$$

Q_G : Gate charge required to turn ON the power element

I_{LKGE} : Leakage current between the gate and emitter of the power element

I_{LK} : Leakage current in the level shift circuit of the gate driver IC

I_{LKDIO} : Leakage current in the bootstrap diode

I_{QBS} : Supply current in the high side of the gate driver IC

T_{HON} : ON time for the high side

Accordingly, set the capacitance value of the bootstrap capacitor so that the following equation is satisfied.

$$C_{BS} \geq \frac{Q_{Total}}{\Delta V_{BS}} \quad (3.2.3)$$

Numerical example

Use an RFN1LAM6S fast recovery diode ($V_R = 600$ V, $I_O = 0.8$ A) as the bootstrap diode and an IGBT RGT50NL65D ($V_{CES} = 650$ V, $I_{C(100^\circ C)} = 25$ A) as the power element. Set shunt resistance R_S to 0.033 Ω .

$$V_{CC} = 15 \text{ V (typ)}$$

$$V_F = 1.15 \text{ V (typ) [when } I_F = 0.8 \text{ A] (from the electrical characteristics in the RFN1LAM6S data sheet)}$$

$$V_{GEMIN} = 9.0 \text{ V (typ) [} V_{GE} \text{ when } I_C = 25.0 \text{ A] (from the electrical characteristics curve in the RGT50NL65D data sheet)}$$

$$V_{OL} = 1.62 \text{ V (typ) [} V_{CE(sat)} \text{ when } I_C = 25.0 \text{ A] (from the electrical characteristics in the RGT50NL65D data sheet)}$$

$$V_{RS} = I_C \cdot R_S = 25 \text{ A} \cdot 0.033\Omega \text{ (typ)} = 0.825 \text{ V (typ)}$$

When these values are substituted in Equation (3.2.1),

$$\Delta V_{BS} = 15 \text{ V (typ)} - 1.15 \text{ V (typ)} - 9.0 \text{ V (typ)} - 1.62 \text{ V (typ)} - 0.825 \text{ V (typ)} = 2.405 \text{ V (typ)}$$

is obtained.

$Q_G = 49 \text{ nC (typ)}$ [when $I_C = 25.0 \text{ A}$] (from the electrical characteristics in the RGT50NL65D data sheet)

$I_{LKGE} = 200 \text{ nA (max)}$ (from the electrical characteristics in the RGT50NL65D data sheet)

$I_{ik} = 50 \text{ }\mu\text{A (max)}$ (from the electrical characteristics in the BS2114F data sheet)

$I_{LKDIO} = 1 \text{ }\mu\text{A (max)}$ (from the electrical characteristics in the RFN1LAM6S data sheet)

$I_{QBS} = 150 \text{ }\mu\text{A (max)}$ (from the electrical characteristics in the BS2114F data sheet)

$T_{HON} = 100 \text{ }\mu\text{s (typ)}$ (when the PWM frequency is 10 kHz and the ON time of the upper side power element is the maximum of the PWM period)

When these values are substituted in Equation (3.2.2),

$$Q_{\text{Total}} = 49 \text{ nC (typ)} + \{200 \text{ nA (max)} + 50 \text{ }\mu\text{A (max)} + 1 \text{ }\mu\text{A (max)} + 150 \text{ }\mu\text{A (max)}\} \cdot 100 \text{ }\mu\text{s (typ)}$$

$$= 49 \text{ nC (typ)} + 20.1 \text{ nC} = 33.6 \text{ nC}$$

is obtained. When the values of ΔV_{BS} and Q_{Total} are substituted in Equation (3.2.3),

$$C_{BS} \geq \frac{69.1 \text{ nC}}{2.405 \text{ V}} = 28.7 \text{ nF}$$

is obtained.

C_{BS} should be determined so that a sufficient margin is provided, considering variation in supply voltage, variation in the electrical characteristics of the elements, the temperature characteristics, and other factors.

Meanwhile, since the UVLO (8.2 V (typ)) is installed between VB and VS, C_{BS} should also be set so that the voltage between VB and VS remains higher than the voltage that will activate the UVLO by ΔV_{BS} .

In addition, if a countermeasure against surge is necessary, place a zener diode (20.5 V to 24.5 V) for surge absorption immediately next to the terminal.

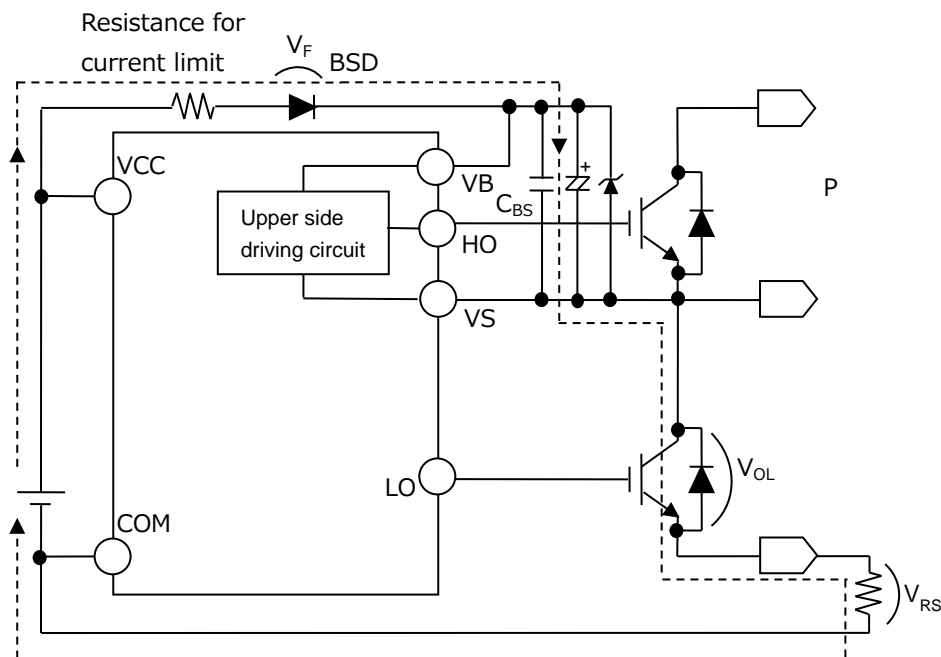


Figure 3.2.4 Bootstrap circuit (with IGBT power element, simplified single phase)

■ Resistance for current limit

Connect a resistance for the current limit in series to each bootstrap diode (BSD). Determine a resistor value so that a current value is obtained that does not exceed the average rectified current of the maximum rating for the BSD to be used. In addition, de-rating should be achieved with the current value.

Note the consumption power with this resistance and select a product that does not exceed the rated power of the resistance.

■ Bootstrap diode (BSD)

The DC reverse voltage (V_R) of the absolute maximum rating for the BSD should be higher than the power supply (P point) voltage of the power element.

To minimize the amount of charges that return to the VCC terminal power supply from the bootstrap capacitor, it is recommended to use a fast recovery diode that has a short reverse recovery time (t_{rr}).

3.2.2 Design method for output gate resistance

With an output gate resistance, you can set the switching time t_{sw} or the variation rate of the output voltage dV_S/dt (the slew rate of the output voltage).

For the gate resistance setting, consider the switching time or the variation rate of the output voltage that is required for the set, and determine the gate resistance that provides such characteristics.

■ Value of the gate resistance at turn-on

(1) Method for calculating the gate resistance from the switching time t_{sw}

The switching time t_{sw} is defined as the time shown in Figure 3.2.5.

• The current that flows through the gate of the power device is described by the following equation.

$$I_g = \frac{Q_{ge} + Q_{gc}}{t_{sw}} \quad (3.2.4)$$

• The gate resistance at turn-on is described by the following equation.

$$R_{TOTAL(on)} = R_{pon} + R_{G(on)} = \frac{V_{BS} - V_{ge(th)}}{I_g} \quad (3.2.5)$$

By substituting Equation (3.2.4) into Equation (3.2.5), the gate resistance is determined as follows.

$$R_{G(on)} = \frac{(V_{BS} - V_{ge(th)}) \times t_{sw}}{Q_{ge} + Q_{gc}} - R_{pon} \quad (3.2.6)$$

t_{sw} : Required switching time

V_{BS} : Gate drive voltage in the high side

$V_{ge(th)}$: ON threshold of the power element

Q_{ge} : Charge between the gate and emitter of the power element

Q_{gc} : Charge between the gate and collector of the power element

R_{pon} : ON-resistance in the high side of the output stage of the gate driver

Numerical example

Use an RFN1LAM6S fast recovery diode ($V_R = 600$ V, $I_O = 0.8$ A) as the bootstrap diode and an IGBT RGT50NL65D ($V_{CES} = 650$ V, $I_{C(100^\circ C)} = 25$ A) as the power element.

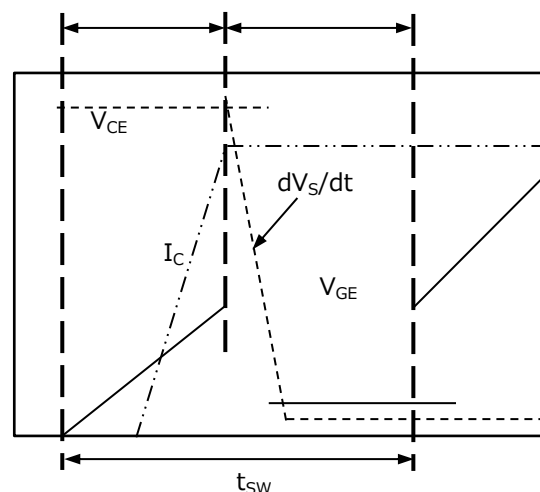


Figure 3.2.5. Gate charge transfer characteristics

$t_{SW} = 1 \mu s$ (with the PWM frequency of 10 kHz, the switching time should be less than 1/100 of the PWM period)

$$V_{BS} = V_{CC} - V_F = 15V(\text{typ}) - 1.15V(\text{typ}) = 13.85V(\text{typ})$$

($V_{CC} = 15 V$ (typ) and the value of V_F is taken from the electrical characteristics in the data sheet for the RFN1LAM6S diode of the bootstrap circuit)

$$V_{ge(th)} = 9.0 V (\text{typ}) [V_{GE} \text{ when } I_C = 25.0 A] \text{ (from the electrical characteristics curve in the RGT50NL65D data sheet)}$$

$$Q_{ge} = 15.0 \text{ nC (typ) (from the electrical characteristics in the RGT50NL65D data sheet)}$$

$$Q_{gc} = 19.0 \text{ nC (typ) (from the electrical characteristics in the RGT50NL65D data sheet)}$$

$$R_{pon} = 10\Omega (\text{typ}) \text{ (from the electrical characteristics curve in the BS2114F data sheet)}$$

When these values are substituted in Equation (3.2.6),

$$R_{G(on)} = \frac{(13.85V(\text{typ}) - 9.0V(\text{typ})) \times 1\mu s(\text{typ})}{15.0\text{nC} + 19.0\text{nC}} - 10\Omega(\text{typ}) = 142\Omega(\text{typ}) - 10\Omega(\text{typ}) = 132\Omega(\text{typ})$$

is obtained.

- (2) Method for calculating the gate resistance from the variation rate of the output voltage (slew rate of the output stage)
- The value of dV_S/dt can be determined from the value of the gate resistance. The slew rate of a power device is determined by the following equation.

$$\frac{dV_S}{dt} = \frac{I_g}{C_{res}} \quad (3.2.7)$$

- The gate resistance at turn-on is described by the following equation.

$$R_{TOTAL(on)} = R_{pon} + R_{G(on)} = \frac{V_{BS} - V_{ge(th)}}{I_g} \quad (3.2.8)$$

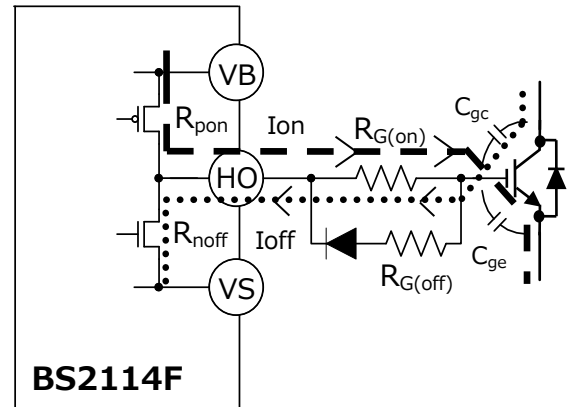


Figure 3.2.6 Gate driver equivalent circuit

By substituting Equation (3.2.7) into Equation (3.2.8), the gate resistance $R_{G(on)}$ is determined as follows.

$$R_{G(on)} = \frac{V_{BS} - V_{ge(th)}}{C_{res} \times \frac{dV_S}{dt}} - R_{pon} \quad (3.2.9)$$

dV_S/dt : Variation rate of the output voltage (slew rate of the output stage)

C_{res} : Feedback capacitance of the power element

V_{BS} : Gate drive voltage in the high side

$V_{ge(th)}$: ON threshold of the power element

R_{pon} : ON-resistance in the high side of the output stage of the gate driver

Numerical example

Use an RFN1LAM6S fast recovery diode ($V_R = 600$ V, $I_O = 0.8$ A) as the bootstrap diode and an IGBT RGT50NL65D ($V_{CES} = 650$ V, $I_{C(100^\circ C)} = 25$ A) as the power element.

$dV_S/dt = 3.0$ V/ns (a value that satisfies the noise and heating requirements based on an empirical rule)

$C_{res} = 22$ pF (from the electrical characteristics in the RGT50NL65D data sheet)

$V_{BS} = V_{CC} - V_F = 15V(\text{typ}) - 1.15V(\text{typ}) = 13.85V(\text{typ})$

($V_{CC} = 15$ V (typ) and the value of V_F is taken from the electrical characteristics in the data sheet for the RFN1LAM6S diode of the bootstrap circuit)

$V_{ge(th)} = 9.0$ V (typ) [V_{GE} when $I_C = 25.0$ A] (from the electrical characteristics curve in the RGT50NL65D data sheet)

$R_{pon} = 10\Omega$ (typ) (from the electrical characteristics curve in the BS2114F data sheet)

When these values are substituted in Equation (3.2.9),

$$R_{G(on)} = \frac{13.85V(\text{typ}) - 9.0V(\text{typ})}{22pF(\text{typ}) \times 3V/ns} - 10\Omega(\text{typ}) = 73.5\Omega(\text{typ}) - 10\Omega(\text{typ}) = 63.5\Omega(\text{typ})$$

is obtained.

■ Value of the gate resistance at turn-off

When the power device in either the upper or lower side is turned OFF, turning ON the power device in the other side causes a current (I_g) flowing via C_{gc} of the power device in the side that is turned OFF. (Figure 3.2.7)

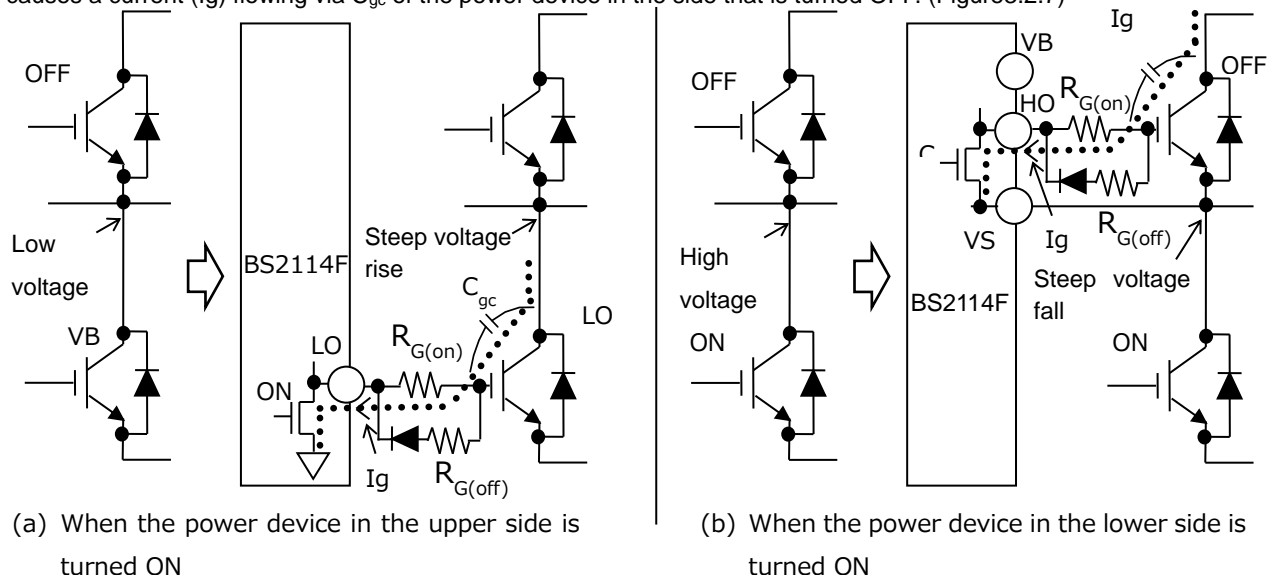


Figure 3.2.7 Rise in the gate voltage of the power device that is turned OFF

At this point, set the value of the gate resistance ($R_{G(off)}$) so that the gate voltage does not exceed the threshold of the power element ($V_{ge(th)}$) and turn ON the element itself.

$$V_{ge(th)} \geq (R_{noff} + R_{g(off)}) \times I_g + V_F = (R_{noff} + R_{g(off)}) \times C_{gc} \frac{dV_S}{dt} + V_F \quad (3.2.10)$$

By transforming the above equation, we obtain the following equation.

$$R_{g(off)} \leq \frac{V_{ge(th)} - V_F}{C_{gc} \frac{dV_S}{dt}} - R_{noff} \quad (3.2.11)$$

dV_S/dt : Variation rate of the output voltage (slew rate of the output stage) of the power element in the side that is turned ON

C_{gc} : Capacitance between the gate and collector ($C_{gc} = C_{res}$)

$V_{ge(th)}$: ON threshold of the power element

V_F : Forward voltage drop in the diode that is connected in series to the gate resistance ($R_{G(off)}$)

R_{noff} : ON-resistance in the low side of the output stage of the gate driver

Numerical example

Use an IGBT RGT50NL65D ($V_{CES} = 650$ V, $I_{C(100^\circ C)} = 25$ A) as a power element and an RB160VAM-40 Schottky barrier diode ($V_R = 40$ V, $I_O = 1.0$ A) as the diode that is connected in series to the gate resistance ($R_{G(off)}$).

$dV_S/dt = 3.0$ V/ns (from a standard setting for the slew rate of the output stage of the power element that is turned ON)

$C_{gc} = C_{res} = 22.0$ pF (typ) (from the electrical characteristics in the RGT50NL65D data sheet)

$V_{ge(th)} = 6.0$ V (typ) [when $I_C = 17.5$ mA] (from the electrical characteristics in the RGT50NL65D data sheet)

$V_F = 0.50$ V (typ) [when $I_F = 0.7$ A] (from the electrical characteristics in the RB160VAM-40 data sheet)

$R_{noff} = 8\Omega$ (typ) (from the electrical characteristics curve in the BS2114F data sheet)

When these values are substituted in Equation (3.2.1),

$$R_{g(\text{off})} \leq \frac{6.0V(\text{typ}) - 0.5V(\text{typ})}{22\text{pF}(\text{typ}) \times \frac{3.0V}{ns}} - 8\Omega(\text{typ}) = 83\Omega(\text{typ}) - 8\Omega(\text{typ}) = 75\Omega$$

is obtained. $R_{g(\text{off})}$ is set to a value that is 1/3 to 1/10 of $R_{g(\text{on})}$ to adjust the slew rate and prevent the power elements in the upper and lower sides from being turned ON simultaneously.

3.2.3 VCC terminal (V_{CC})

- To prevent a malfunction or breakdown due to a switching noise or power supply ripple, install electrolytic capacitor C1, which has excellent temperature and frequency characteristics as a bypass capacitor near the terminal. To reduce the power supply impedance over a broad frequency bandwidth, also install ceramic capacitors C2, C3, and C4 (characteristics B or R recommended) with a capacitance of 0.1 μ F to 0.22 μ F, which have excellent temperature, frequency, and DC bias characteristics in parallel to the electrolytic capacitor immediately next to the VCC terminal of each gate driver.
- If a countermeasure against surge is necessary, place a zener diode (18.5 V to 19.5 V) with a power loss of approximately 1 W for surge absorption immediately next to the terminal.
- Since the V_{CC} capacitor supplies charges to the high and low sides and it also supplies a large amount of charges for the initial charge of bootstrap capacitor C_{BS} , a capacitor that has a capacitance larger than the total capacitance of the bootstrap capacitors in three phases by a factor of 2 (larger than the capacitance of a bootstrap capacitor by a factor of 6) is recommended.
- Design a power supply circuit that satisfies $V_{ripple} \leq 2 V_{p-p}$ with the power supply noise of $dV/dt \leq 1 V/\mu s$. (Reference value)

3.2.4 Power supply for external power element

- To prevent an over voltage breakdown due to a surge voltage, keep the wiring between the smoothing capacitor and points P and N (the terminal parts of the shunt resistor) as thick and short as possible.
- It is recommended to install snubber capacitor C5 with a capacitance of 0.1 μ F to 0.22 μ F between points P and N.

3.2.5 Control input terminal (HIN, LIN)

- To prevent a malfunction, keep the wiring as short as possible.
- The input signal is high-active. A pull-down at approximately 1MΩ (typ) is performed inside the LSI. When inserting an RC filter, adjust the setting to satisfy the input threshold voltage.
- Be sure to observe the rest time (Δt_{IN}) for the upper and lower arms as described below.
- Input signal interval Δt_{IN}
The minimum interval between input signals ($\Delta t_{IN(min)}$) that is required to prevent the power elements in the high and low sides from being turned ON simultaneously can be calculated by the following equation.

$$t_{dead} \approx (t_{on} + \Delta t_{IN}) - (t_{off} + t_f) \quad (3.2.12)$$

$$t_f = -\tau \times (\ln 0.1 - \ln 0.9) \quad (3.2.13)$$

$$\tau = (R_{non} + R_G) \times C_L \quad (3.2.14)$$

t_{on} : Propagation delay in the ON side

t_{off} : Propagation delay in the OFF side

t_f : Fall time

R_{non} : N-channel on-resistance of the final stage of

the gate driver

R_G : Gate resistance

C_L : Load capacitance

To prevent the simultaneous ON, design the timing to satisfy the following conditions.

$$t_{dead} > 0 \quad (3.2.15)$$

$$(t_{on} + \Delta t_{IN}) - (t_{off} + t_f) > 0 \quad (3.2.16)$$

$$\Delta t_{IN} > (t_{off} - t_{on}) + t_f \quad (3.2.17)$$

$$\Delta t_{IN(min)} > (t_{off(max)} - t_{on(min)}) - (R_{non(max)} + R_G) \times C_L \times (\ln 0.1 - \ln 0.9) \quad (3.2.18)$$

3.2.6 COM terminal

- The COM terminal serves as the ground for the control system and the output stage part.

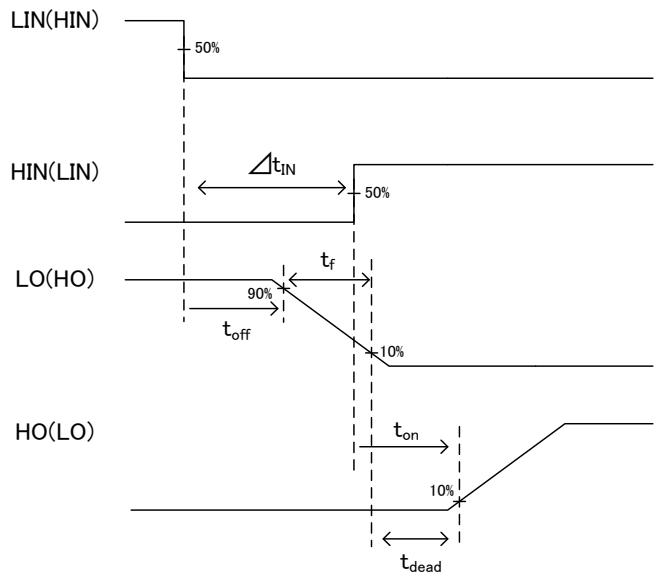


Figure 3.2.8. Shoot-through prevention timing

3.2.7 Shunt resistor

(1) Driving with one shunt resistor

Notes for the wiring around an external shunt resistor when driving with one shunt resistor are shown in the figure below (Figure 3.2.9).

The surface mounted, low inductance type is recommended for the shunt resistor.

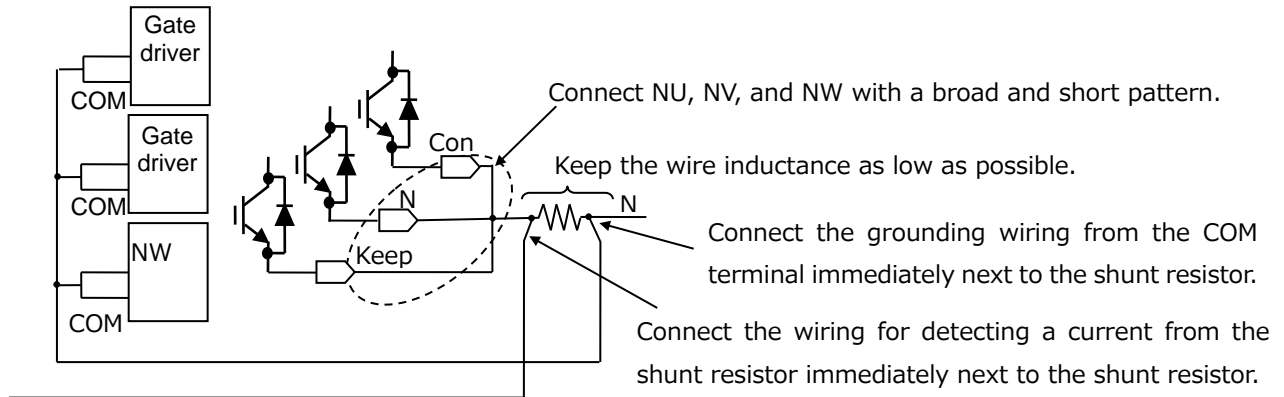


Figure 3.2.9 Wiring around an external shunt resistor when driving with one shunt resistor

(2) Driving with three shunt resistors

Notes for the wiring around external shunt resistors when driving with three shunt resistors are shown in the figure below (Figure 3.2.10).

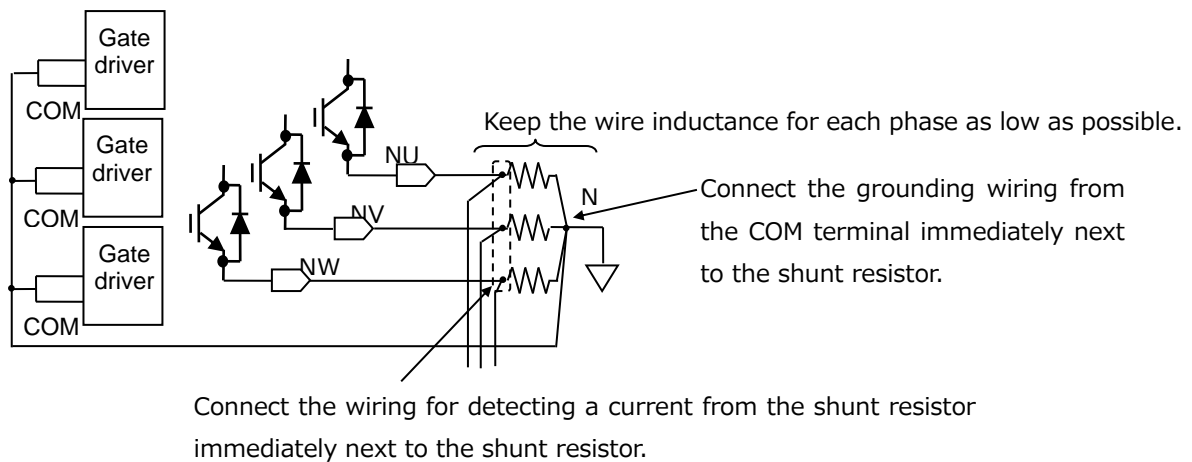
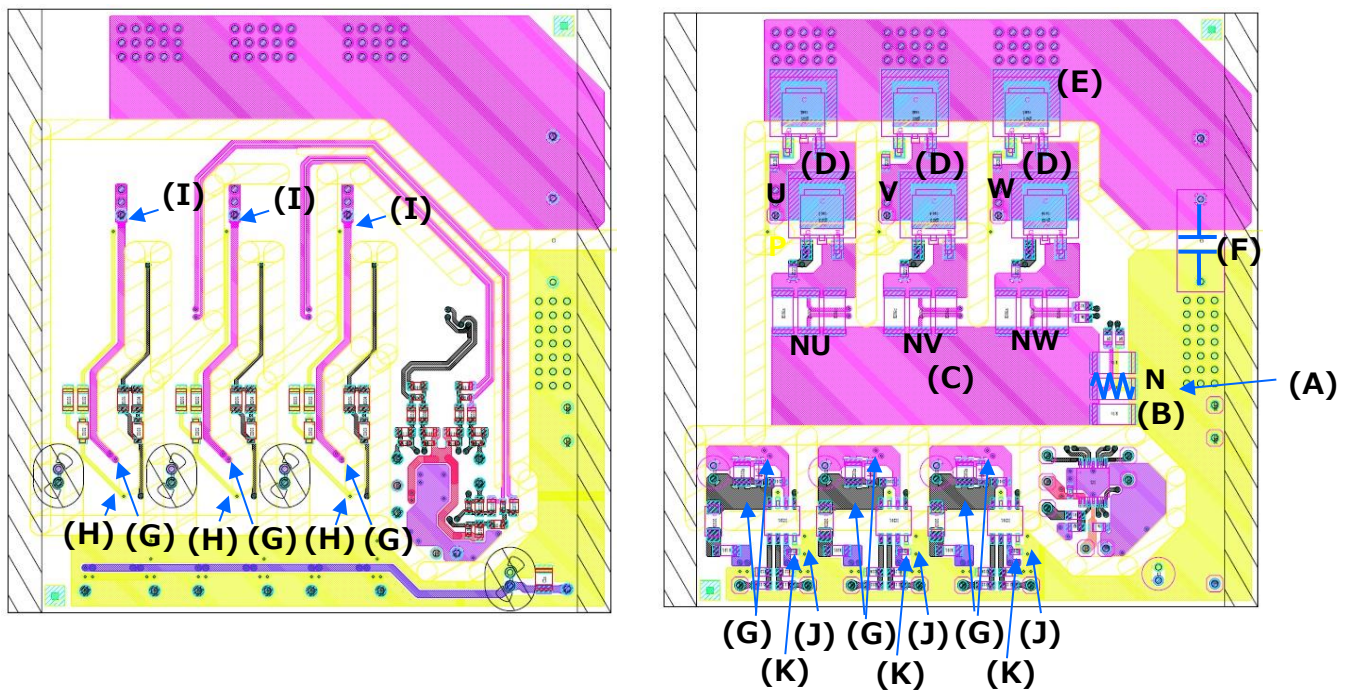


Figure 3.2.10 Wiring around an external shunt resistor when driving with three shunt resistors

3.3 Notes for PCB pattern designing including the power elements



Size: 90mm x 90mm

Figure 3.3.1 Example of PCB pattern

- (A) Connect the power ground and the control system ground at a single point immediately next to the terminal part of the shunt resistor (point N).
- (B) The surface mounted, low inductance type is recommended for the shunt resistor.
- (C) Keep the wiring from points NU, NV, and NW to the shunt resistor as short as possible.
- (D) Keep the wiring for output points U, V, and W itself and the wiring to the motor as short and broad as possible.
- (E) Keep the wiring of the power supply for power elements as broad and short as possible.
- (F) Place the snubber capacitor immediately next to and between points P and N.
- (G) To minimize the parasitic inductance, keep the wiring for the bootstrap diode and capacitor as short as possible. Since the wiring for the VB and VS terminals swings at a high voltage during the switching, any adjacent wiring may result in superimposing noise, causing a malfunction. When using a multilayer board, etc., design the circuit so that these wirings will not be placed adjacent to or cross low voltage wirings, such as the wiring for the control input signal.
- (H) Since the wiring from the HO terminal to the gate of the power element in the upper side also swings at a high voltage during the switching, any adjacent wiring may result in superimposing noise, causing a malfunction. When using a multilayer board, etc., design the circuit so that these wirings will not be placed adjacent to or cross low voltage wirings, such as the wiring for the control input signal.
- (I) Separate the wiring for each VS terminal at the output point (U, V, or W) from the main wiring for the motor, so that they will not have a common impedance.
- (J) Since the charge current for the bootstrap flows to the ground for the control system, keep the wiring as short and low impedance as possible.
- (K) Place the capacitor immediately next to the VCC terminal.

3.4 Snubber capacitor connection

To prevent an over voltage breakdown due to a surge voltage, make the wiring between the smoothing capacitor and points P and N (the terminal parts of the shunt resistor) as thick and short as possible. In addition, install a snubber capacitor with a capacitance of 0.1 μF to 0.22 μF immediately next to the collector (or drain) of the power elements in the upper side and immediately next to the ground side of the shunt resistor.

Figure 3.4.1 shows an example for the positions to insert the snubber capacitors.

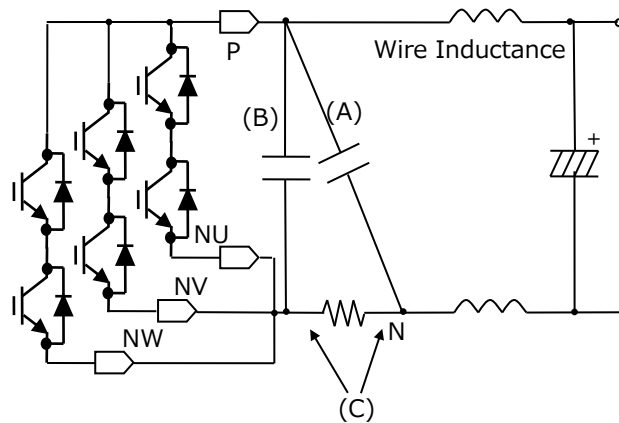


Figure 3.4.1 Connection method of snubber capacitor

To remove a surge voltage as much as possible, the snubber capacitor should be installed on position (B). However, care must be taken because the charge/discharge current (resonance current between the wire inductance and the snubber capacitor) flows in the shunt resistor through the snubber capacitor, activating the protection circuit against the short-circuit current if the wire inductance is large. A recommended connection is as follows: connect the snubber capacitor to the outside of the shunt resistor (A), keep the wiring (C) as short as possible to remove the surge voltage as much as possible, and connect the snubber capacitor immediately next to point P

• Revision history

Date	Revision	Revised content
Jan. 31, 2018	001	Newly created

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