FEDR45V200B-02
Issue Date: Oct. 2, 2018

MR45V200B

2M(262,144-Word × 8-Bit) FeRAM (Ferroelectric Random Access Memory) SPI

GENERAL DESCRIPTION

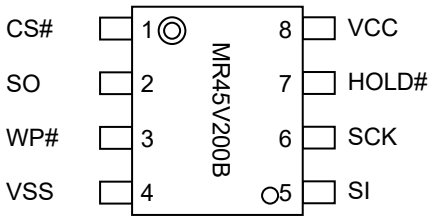
The MR45V200B is a nonvolatile 262,144-word x 8-bit ferroelectric random access memory (FeRAM) developed in the ferroelectric process and silicon-gate CMOS technology. The MR45V200B is accessed using Serial Peripheral Interface. Unlike SRAMs, this device, whose cells are nonvolatile, eliminates battery backup required to hold data. This device has no mechanisms of erasing and programming memory cells and blocks, such as those used for various EEPROMs. Therefore, the write cycle time can be equal to the read cycle time and the power consumption during a write can be reduced significantly.
The MR45V200B can be used in various applications, because the device is guaranteed for the write/read tolerance of 10^{13} cycles per bit and the rewrite count can be extended significantly.

FEATURES

- 262,144-word × 8-bit configuration (Serial Peripheral Interface: SPI)
- A single 2.7V to 3.6V power supply
- Operating frequency: 34MHz
- Read/write tolerance 10^{13} cycles/bit
- Data retention 10 years
- Guaranteed operating temperature range –40 to 85°C
- Package:
  8-pin plastic DIP
- RoHS (Restriction of hazardous substances) compliant

PIN CONFIGURATION (TOP VIEW)

8-pin plastic DIP



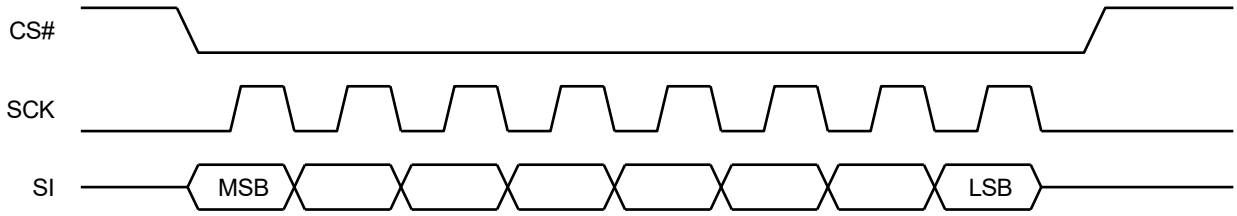
Note:
Signal names that end with # indicate that the signals are negative-true logic.

PIN DESCRIPTIONS

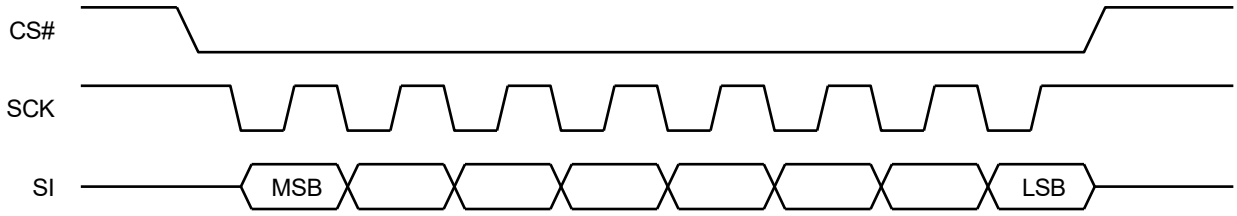
Pin Name	Description
CS#	Chip Select (input, negative logic) Latches an address by low input, activates the FeRAM, and enables read or write operation. High input goes the device disable state.
WP#	Write Protect(input , negative logic) Write Protect pin controls write-operation to the status-register(BP0,BP1). This pin should be fixed low or high in write-operations.
HOLD#	HOLD(input , negative logic) Hold pin is used when the serial-communication suspended without disable the chip select. When HOLD# is low, the serial-output is in High-Z status and serial-input/serial-clock are “Don’t Care”. CS# should be low in hold operation.
SCK	Serial Clock Serial Clock is the clock input pin for setting for serial data timing. Inputs are latched on the rising edge and outputs occur on the falling edge.
SI	Serial input SI pins are serial input pins for Operation-code, addresses, and data-inputs.
SO	Serial output SO pins are serial output pins.
V_{CC}, V_{SS}	Power supply Apply the specified voltage to V_{CC}. Connect V_{SS} to ground.

SPI

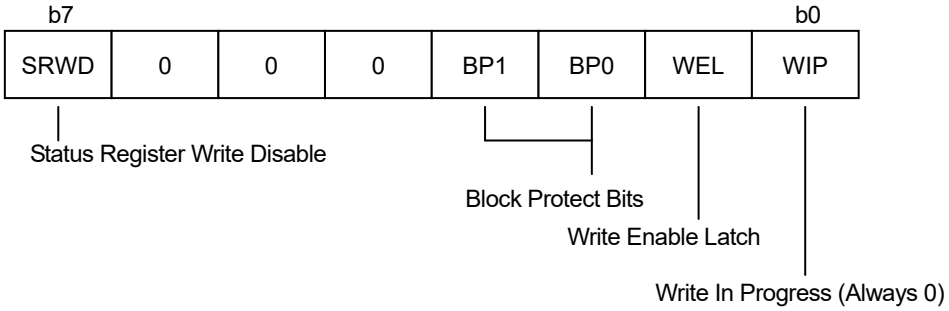
SPI mode0（CPOL=0, CPHA=0）



SPI mode3（CPOL=1, CPHA=1）



Status Register



Name	Function
WIP	Fixed to 0.
WEL	WEL indicates internal Write Enable Latch status. The WEL is set after WREN command. After WRDI command, WRSR command, WRITE command, or Power on, the WEL can be reset.
BP0,BP1	Block Protect: These bits can change protected area. This is the software protect.
SRWD	Status Register Write Disable（SRWD）: SRWD controls the effect of the hardware WP# pin. This device will be in hardware-protect by combination of SRWD and WP#.
0	Fixed to 0.　Reserved for future use. (RFU)

Operation-Code

Operation codes are listed in the table below. If the device receives invalid operation code, the device will be deselected.

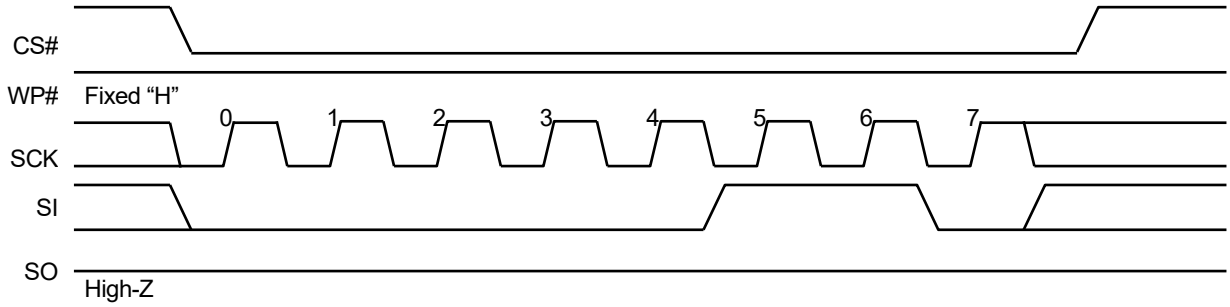
Instruction	Description	Instruction format
WREN	Write Enable	0000 0110
WRDI	Write Disable	0000 0100
RDSR	Read Status Register	0000 0101
WRSR	Write Status Register	0000 0001
READ	Read from Memory Array	0000 0011
WRITE	Write to Memory Array	0000 0010
RDID	Read Device ID	1001 1111

COMMANDS

WREN(Write Enable)

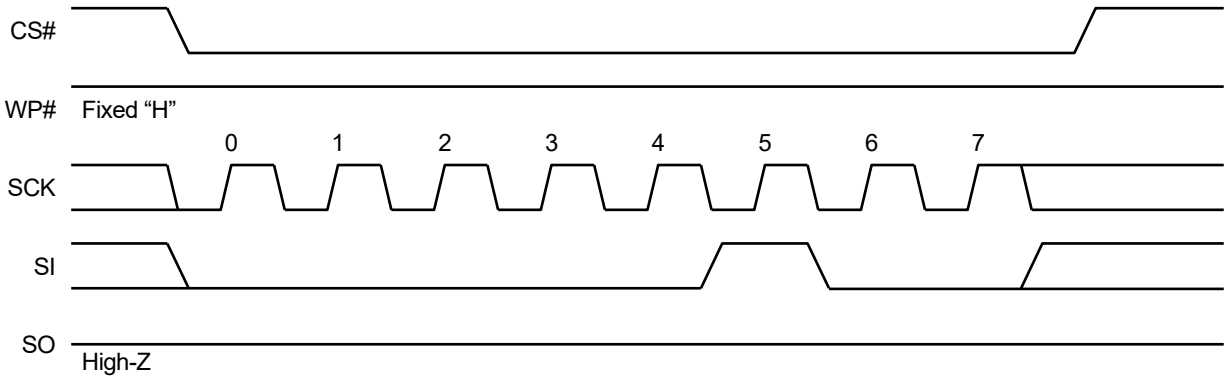
It is necessary to set Write Enable Latch(WEL)bit before write-operation (WRITE and WRSR).

WREN command sets WEL bit.



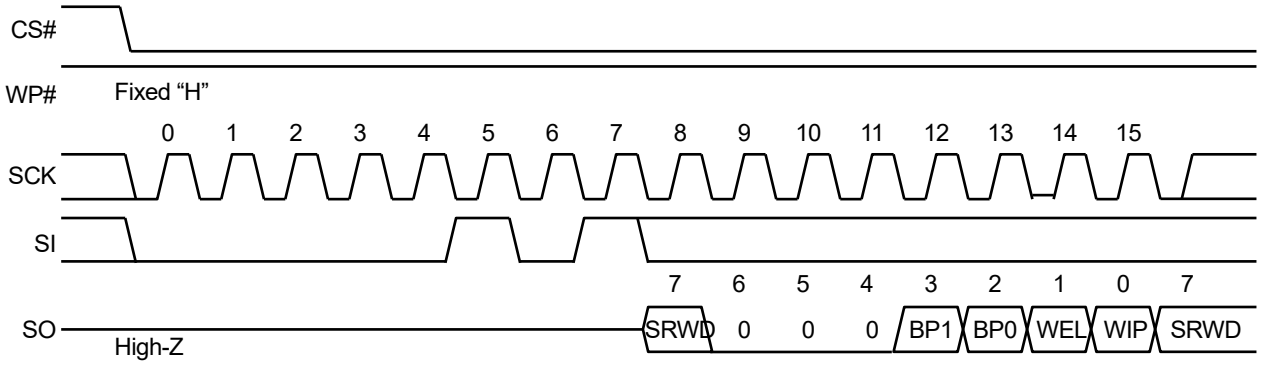
WRDI(Write Disable)

WRDI command resets WEL bit.



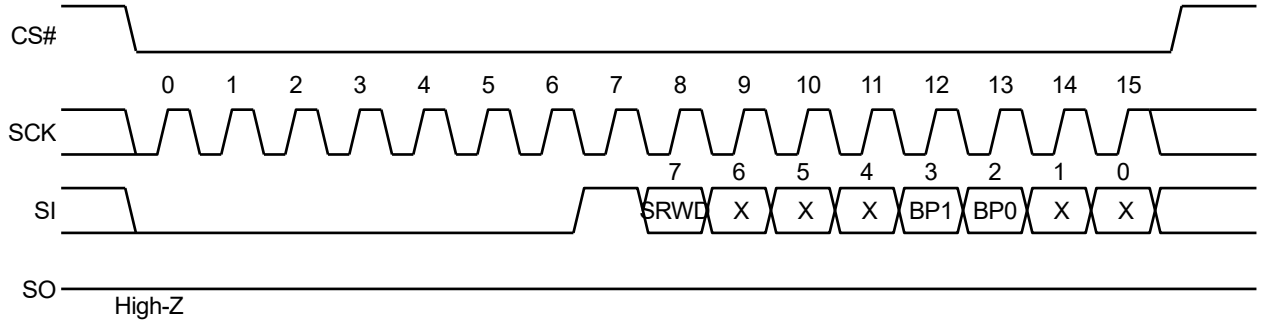
RDSR(READ Status Register)

The RDSR command allows reading data of status register. The Status Register can be read anytime and any number of times.



WRSR(WRITE Status Register）

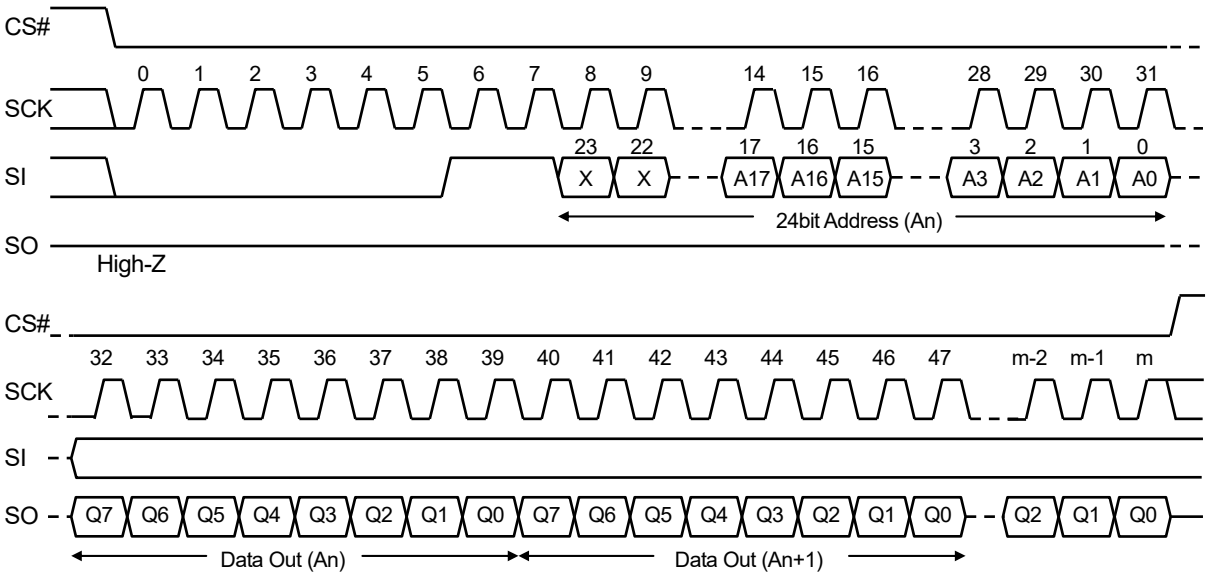
WRSR command allows to write data to status register(SRWD,BP0,BP1). It is necessary to set Write Enable Latch（WEL）bit by WREN command before executing WRSR. WRSR command cannot write RFU(b6,b5,b4), WEL(b1), WIP(b0) of Status Resistor..



Note:
WP#=Fixed ”H”

READ(Read from Memory Array)

READ command can be valid when CS# goes “L”, then the op-code and 24bit-adresses are inputted to serial input ”SI”. The inputted addresses are loaded to internal register, then the data from corresponded address is output at serial-output “SO”. If CS# will keep “L”, the internal address will be increased automatically after 8 clocks and will output the data from new-address. When it reaches the most significant address, the address counter rolls over to starting address and reading cycle can be continued infinitely. To finish read cycle, make the CS# “H” during LSB output clock.

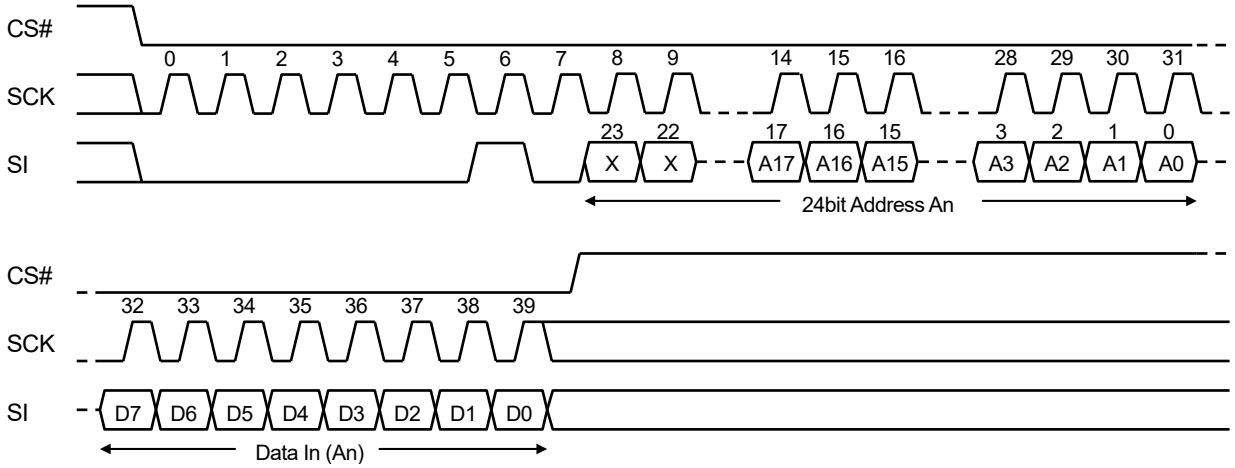


Note : WP# = fixed ”H”

WRITE(Write to Memory Array)

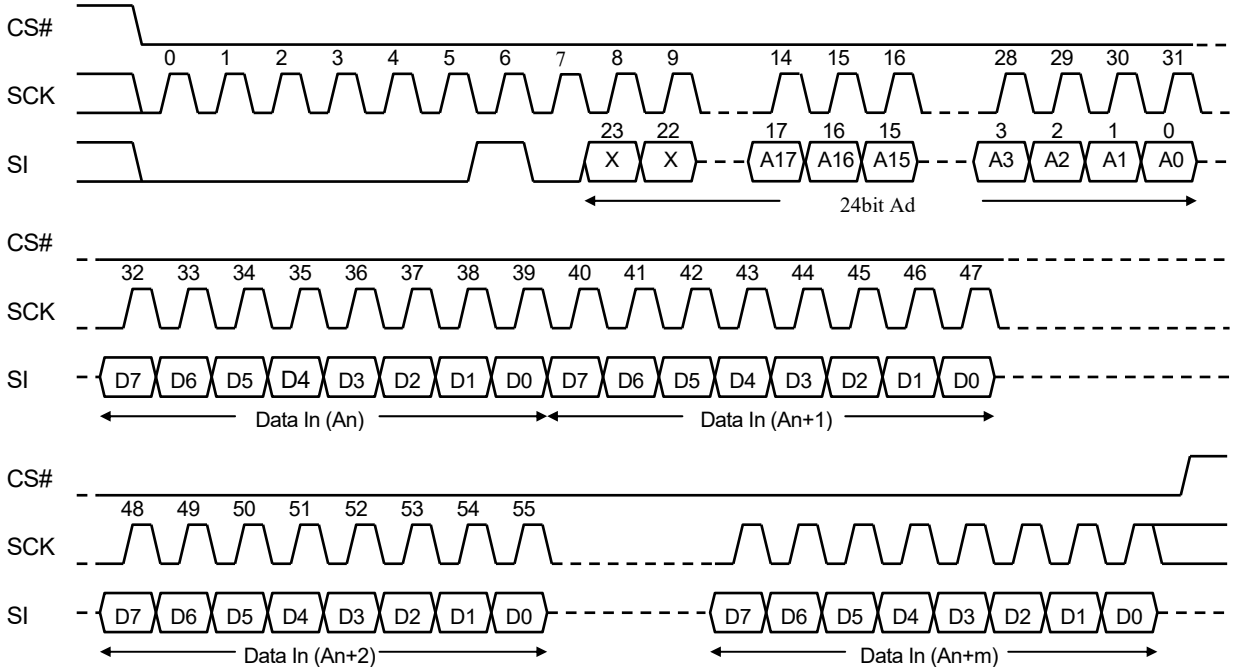
Write command can be valid when CS# goes “L”, then the op-code and 24bit-adresses are inputted to serial input ”SI”. Writing is terminated when CS# goes high after data-input. If CS# will keep “L”, the internal address will be increased automatically. When it reaches the most significant address, the address counter rolls over to starting address 0000h, and writing cycle (overwriting) can be continued infinitely. To finish write cycle, make CS# “H” during LSB input clock.

WRITE(1Byte)



Note : WP# = Fixed ”H” , SO=High-Z

WRITE(Page)

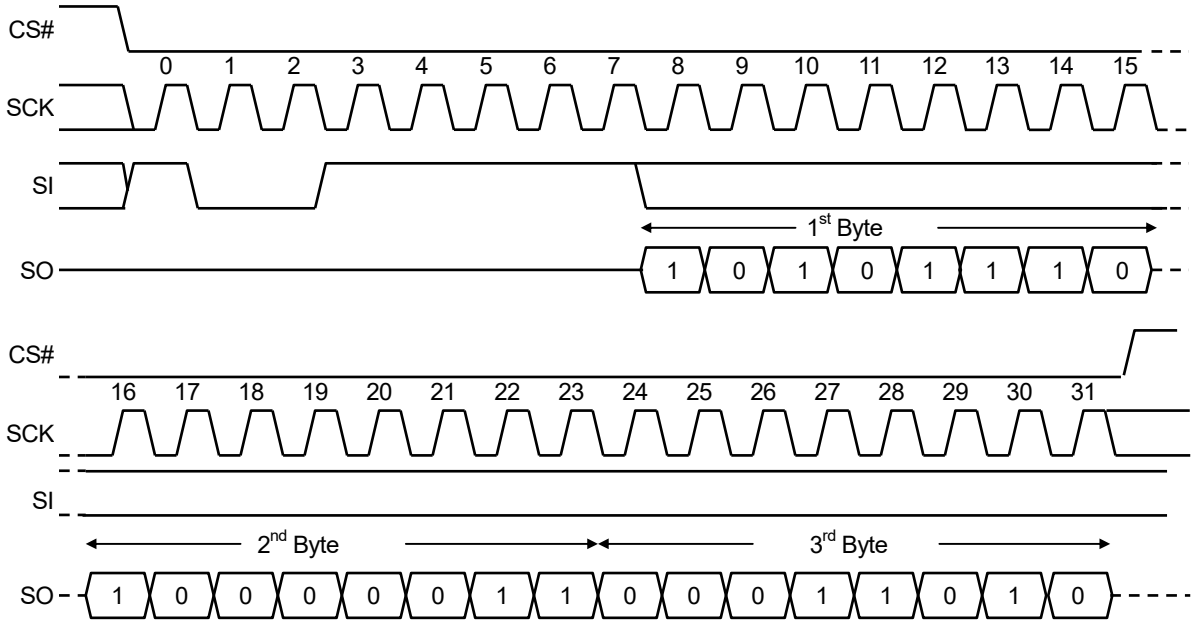


Note : WP# = Fixed ”H” , SO=High-Z

RDID (Read device ID)

RDID command can be valid when CS# goes “L”, then the op-code are inputted to serial input ”SI”. Then 3bytes of device ID is output at serial-output “SO”.

Manufacture ID (LAPIS)	Device type (MR45V200B)	
1st Byte	2nd Byte	3rd Byte
AEh	83h	1Ah



Note : WP# = Fixed ”H”

Write Protection

Writing protection block is shown as follows: When Status Resister Write Disable(SRWD) bit is reset to “0”, Status Resister number can be changed

Protect Block size

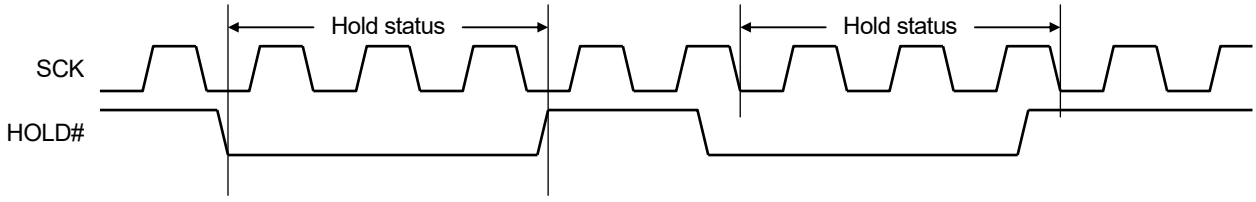
Block Protect BIT		Protected Block	Protected Address Area
BP1	BP0		
0	0	None	None
0	1	Upper 1/4 block	30000h – 3FFFFh
1	0	Upper 1/2 block	20000h – 3FFFFh
1	1	All	00000h – 3FFFFh

Writing Protect

WP#	SRWD	mode	Writing protection status in status register	Protection status in memory	
				Protected blocks	Unprotected blocks
1	0	Software protection (SPM)	Status register is unprotected when WEL-bit is set by WREN command. BP0 and BP1 are unprotected.	Protected	Unprotected
0	0				
1	1				
0	1	Hardware protection (HPM)	Status register is protected. BP0 and BP1 are protected.	Protected	Unprotected

HOLD

Hold status is used for suspending serial communication without disable the chip. SO becomes “High-Z” and SI is “Don’t care” during the hold status. It is necessary to keep CS#=L in hold status.



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

The application of stress (voltage, current, or temperature) that exceeds the absolute maximum rating may damage the device. Therefore, do not allow actual characteristics to exceed any one parameter ratings

Pin voltages

Parameter	Symbol	Rating		Unit
		Min.	Max.	
Pin Voltage (Input Signal)	V_{IN}	–0.5	V_{CC} + 0.5	V
Pin Voltage (Input/Output Voltage)	V_{INQ}, V_{OUTQ}	–0.5	V_{CC} + 0.5	V
Power Supply Voltage	V_{CC}	–0.5	4.0	V

Temperature Range

Parameter	Symbol	Rating		Unit
		Min.	Max.	
Storage Temperature (Extended Temperature Version)	Tstg	–55	125	°C
Operating Temperature (Extended Temperature Version)	Topr	–40	85	°C

Others

Parameter	Symbol	Rating	Unit
Power Dissipation	P_D	1,000mW	
Allowable Input Current	I_{IN}	+/- 20mA	Ta=25°C
Allowable Output Current	I_{OUT}	+/- 20mA	Ta=25°C

Recommended Operating Conditions

Power Supply Voltage

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	2.7	3.3	3.6	V
Ground Voltage	V_{SS}	0	0	0	V

DC Input Voltage

Parameter	Symbol	Min.	Max.	Unit
Input High Voltage	V_{IH}	V_{CC} x 0.8	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	–0.3	V_{CC} x 0.15	V

DC Characteristics

DC Input/Output Characteristics

Parameter	Symbol	Condition	Min.	Max.	Unit
Output High Voltage	V_{OH}	I_{OH} =−2mA	$V_{CC} \times 0.85$	—	V
Output Low Voltage	V_{OL}	I_{OL} =2mA	—	$V_{CC} \times 0.15$	V
Input Leakage Current	I_{LI}	—	–10	10	μA
Output Leakage Current	I_{LO}	—	–10	10	μA

Power Supply Current

V_{CC}=Max.to Min, Ta=Topr

Parameter	Symbol	Condition	Min.	Max.	Unit	Note
Power Supply Current (Standby)	I_{CCS}	CS#= V_{CC} ,V_{IN}=0V or V_{CC}	—	100	μA	
Power Supply Current (Operating)	I_{CCA}	V_{IN}=0.2V or V_{CC}−0.2V, SCK=Max., I_{OUT}=0mA	—	10	mA	1

Note1: average current.

AC Characteristics

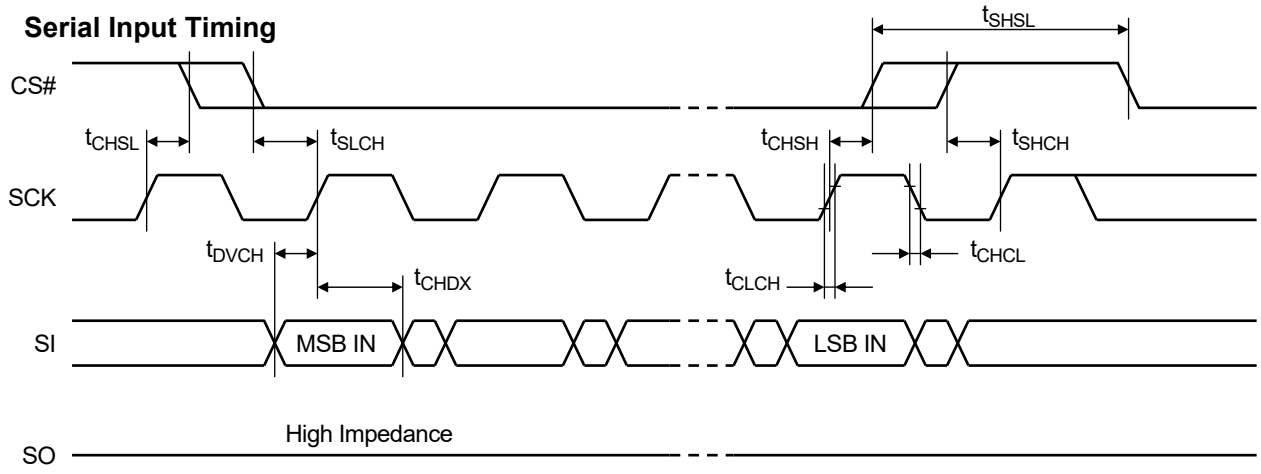
V_{CC}=Max. to Min., Ta=Topr.

Parameter	Symbol	MR45V200B		Unit	Note
		Min.	Max.		
Clock frequency	f_C	D.C.	34	MHz	
CS# Active setup time	t_{SLCH}	10	—	ns	
CS# In-active setup-time	t_{SHCH}	10	—	ns	
CS# De-select time	t_{SHSL}	10	—	ns	
CS# Active hold time	t_{CHSH}	10	—	ns	
CS# In-active hold-time	t_{CHSL}	10	—	ns	
SCK High time	t_{CH}	13	—	ns	1
SCK Low time	t_{CL}	13	—	ns	1
SCK Rise time	t_{CLCH}	—	50	ns	2
SCK Fall time	t_{CHCL}	—	50	ns	2
Data Setup time	t_{DVCH}	5	—	ns	
Data Hold time	t_{CHDX}	5	—	ns	
SCK Low Hold time after HOLD# inactive	t_{HHCH}	10	—	ns	
SCK Low Hold time after HOLD# active	t_{HLCH}	10	—	ns	
SCK High Setup time before HOLD# active	t_{CHHL}	10	—	ns	
SCK High Setup time before HOLD# inactive	t_{CHHH}	10	—	ns	
Output disable time	t_{SHQZ}	—	12	ns	2
SCK Low to Output Valid time	t_{CLQV}	—	12	ns	
Output Hold time	t_{CLQX}	0	—	ns	
HOLD# High to Output Low impedance time	t_{HHQX}	—	20	ns	2
HOLD# High to Output High impedance time	t_{HLQZ}	—	20	ns	2

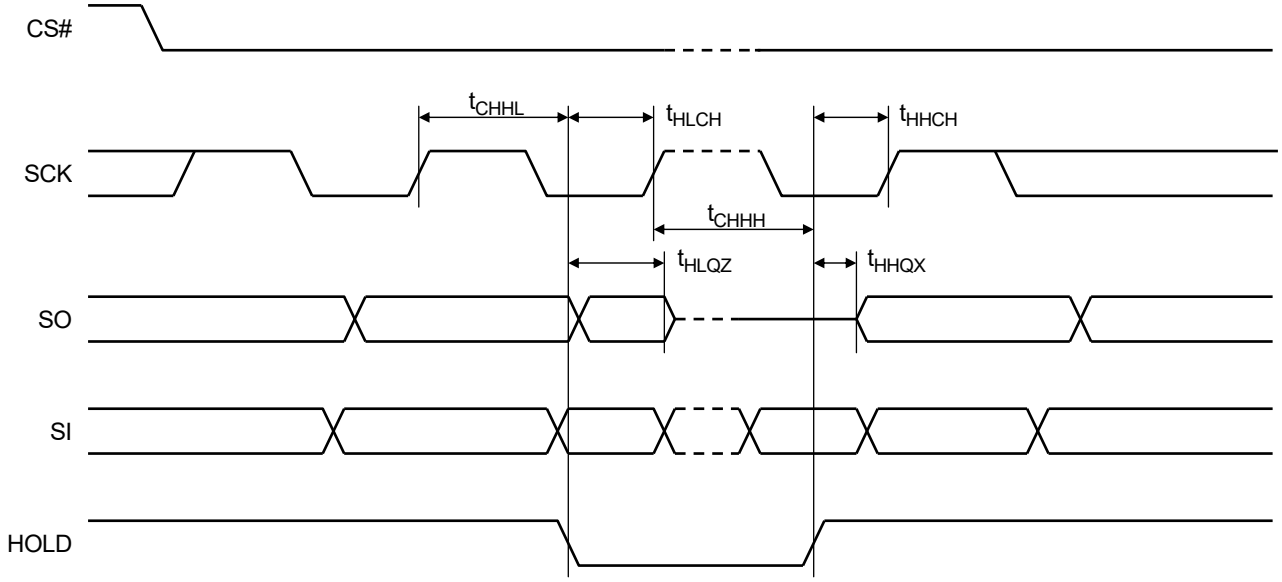
Note: 1. $t_{CH}+t_{CL} \geqq 1/f_C$
2. sample value

Timing Diagrams

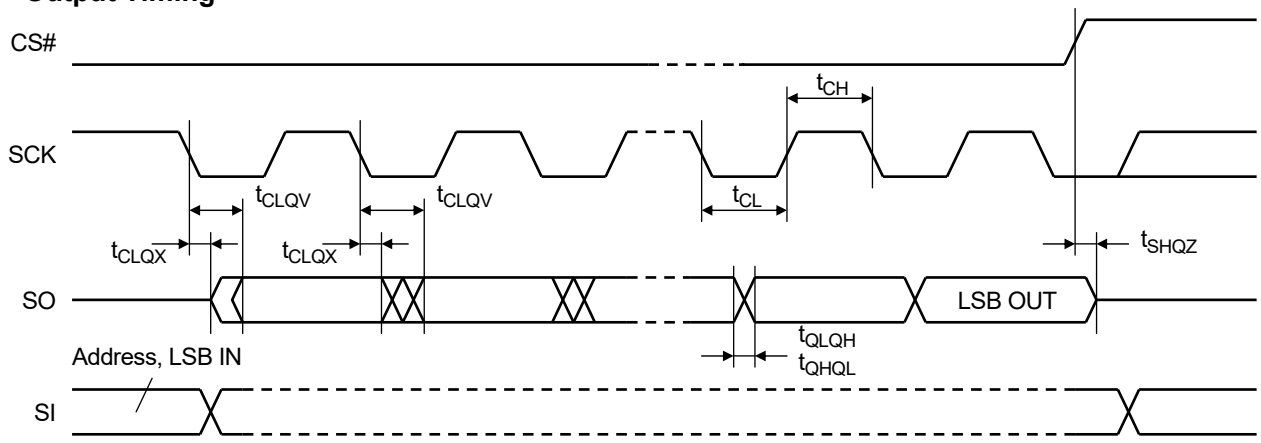
Serial Input Timing



Hold Timing



Output Timing



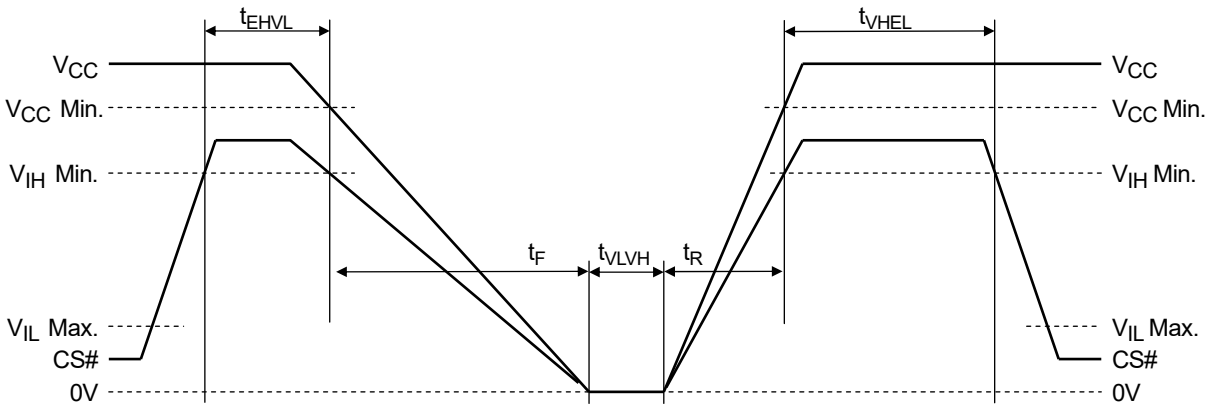
•Power-On and Power-Off Characteristics

(Under recommended operating conditions)

Parameter	Symbol	Min.	Max.	Unit	Note
Power-On CS# High Hold Time	t_{VHEL}	50	—	μs	1, 2
Power-Off CS# High Hold Time	t_{EHVL}	100	—	ns	1
Power-On Interval Time	t_{VLVH}	1	—	μs	2
Power-On Rise time	t_R	50	100,000	μs/V	
Power-down Fall time	t_F	100		μs/V	

Notes:
1. To prevent an erroneous operation, be sure to maintain CS#="H", and set the FeRAM in an inactive state (standby mode) before and after power-on and power-off.
2. Powering on at the intermediate voltage level will cause an erroneous operation; thus, be sure to power up from 0 V.
3. Enter all signals at the same time as power-on or enter all signals after power-on.

•Power-On and Power-Off Sequences



Read/Write Cycles and Data Retention

(Under recommended operating conditions)

Parameter	Min.	Max.	Unit	Note
Read/Write Cycle	10^{13}	—	Cycle	1
Data Retention	10	—	Year	

Note: 1. Total power on time ≤ 10 years

Capacitance

Signal	Symbol	Min.	Max.	Unit	Note
Input Capacitance	C_{IN}	—	10	pF	1
Input/Output Capacitance	C_{OUT}	—	10	pF	1

Note:
Sampling value. Measurement conditions are $V_{IN} = V_{OUT}$ = GND, Vcc=3.3V, f = 1MHz, and Ta = 25°C

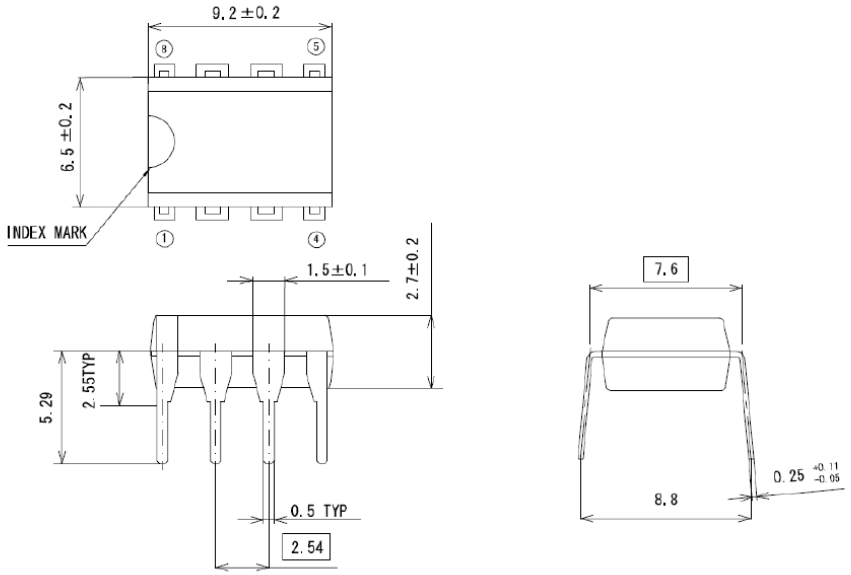
ORDERING INFORMATION

Product No.	Package Type (Package Code)	Packing	Temp. Range
MR45V200BRAZAARL	8-pin plastic DIP (P-DIP8-300-2.54-T6)	Plastic Tube	−40 to 85°C

PACKAGE DIMENSIONS

P-DIP8-300-2.54-T6

(Unit: mm)



NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION DIEPAD SUPPORT PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.

LAPIS Semiconductor Co.,Ltd.

Package material	Epoxy resin
Lead frame material	Cu alloy
Lead finish	Sn (100%)
Solder thickness	More Than 5μm
Package weight (g)	0.43 TYP.
Rev. No./Last Revised	1 / Nov. 14, 2013

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDR45V200B-01	Sep. 14, 2018	–	–	Final edition 1
FEDR45V200B-02	Oct. 02, 2018	9 –	8 17	Moved RDID to page8 Added ordering information

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