SLA7050M/SLA7051M/SLA7052M 2-Phase/1-2 Phase Excitation, Built-in Sequencer

■Absolute Maximum Ratings

(T_a=25°C)

Parameter	Symbol	Ratings			Unit
		SLA7050M	SLA7051M	SLA7052M	
Motor Supply Voltage	V_M	46			V
Load Supply Voltage	V_S	46			V
Logic Supply Voltage	V_{CC}	6			V
Output Current	I_O	1	2	3	A
Logic Input Voltage	V_{IN}	–0.3 to V_{CC}+0.3			V
REF Input Voltage	V_{REF}	–0.3 to V_{CC}+0.3			V
Sense Voltage	V_{RS}	–2 to +2			V
Power Dissipation	P_{D1}	4 (Without Heatsink)			W
	P_{D2}	20 (T_C=25°C)			W
Junction Temperature	T_j	+150			°C
Operating Ambient Temperature	T_a	–20 to +85			°C
Storage Temperature	T_{stg}	–30 to +150			°C

■Recommended Operating Conditions

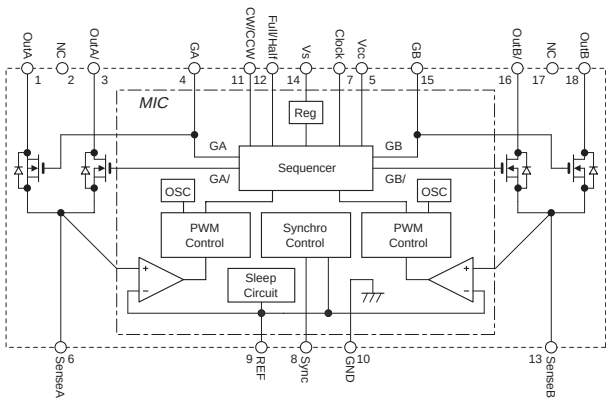
Parameter	Symbol	Ratings		Unit	Remarks
		min.	max.		
Motor Supply Voltage	V_M		44	V	
Load Supply Voltage	V_S	10	44	V	
Logic Supply Voltage	V_{CC}	3.0	5.5	V	The V_{CC} surge voltage should be 0.5V or lower.
REF Input Voltage	V_{REF}	0.1	1.0	V	The control current precision is degraded at 0.1V or lower.
Case Temperature	T_C		100	°C	Temperature at pin-10 Lead (Without heatsink)

■Electrical Characteristics

(V_{CC} = 5V, V_S = 24V, T_a = 25°C, unless otherwise specified)

Parameter	Symbol	Ratings									Unit
		SLA7050M			SLA7051M			SLA7052M			
		min.	typ.	max.	min.	typ.	max.	min.	typ.	max.	
Main Supply Current	I_{SS}			15			15			15	mA
	Conditions	Normal operation			Normal operation			Normal operation			
	I_S			100			100			100	μA
	Conditions	Sleep mode			Sleep mode			Sleep mode			
Logic Supply Current	I_{CC}			3			3			3	mA
Output MOSFET Breakdown Voltage	V_{DSS}	100			100			100			V
	Conditions	V_S=44V, I_{DSS}=1mA			V_S=44V, I_{DSS}=1mA			V_S=44V, I_{DSS}=1mA			
Output MOSFET ON Resistance	$R_{DS\ (ON)}$			0.85			0.5			0.27	Ω
	Conditions	I_D=1A			I_D=1A			I_D=3A			
Output MOSFET Diode Forward Voltage	V_{SD}			1.2			1.1			2.3	V
	Conditions	I_{SD}=1A			I_{SD}=1A			I_{SD}=3A			
Maximum Clock Frequency	F_{clock}			100			100			100	kHz
Logic Input Voltage	V_{IL}			V_{CC}·0.25			V_{CC}·0.25			V_{CC}·0.25	V
	V_{IH}	V_{CC}·0.75			V_{CC}·0.75			V_{CC}·0.75			
Logic Input Current	I_{IL}		±1			±1			±1		μA
	I_{IH}		±1			±1			±1		
REF Input Voltage	V_{REF}	0		1.5	0		1.5	0		1.5	V
	Conditions	Normal-operation current control			Normal-operation current control			Normal-operation current control			
	V_{REFS}	2		V_{CC}	2		V_{CC}	2		V_{CC}	
	Conditions	Output OFF (sleep)			Output OFF (sleep)			Output OFF (sleep)			
REF Input Current	I_{REF}		±10			±10			±10		μA
Sense Voltage	V_{RS}		V_{REF}			V_{REF}			V_{REF}		V
PWM OFF Time	T_{OFF}		12			12			12		μS
PWM Minimum ON Time	$T_{ON\ (min)}$		5			5			5		μS
Sleep - Enable Recovery Time	T_{SE}	100			100			100			
	Conditions	V_{REF} : 2.0→1.5V, I_O : 0.75A			V_{REF} : 2.0→1.5V, I_O : 1.5A			V_{REF} : 2.0→1.5V, I_O : 2.0A			μS
Switching Time	T_{ONC}		2.5			2.5			2.5		μS
	Conditions	Clock→Out			Clock→Out			Clock→Out			
	T_{OFFC}		2.0			2.0			2.0		
	Conditions	Clock→Out			Clock→Out			Clock→Out			

■Internal Block Diagram and Pin Assignment



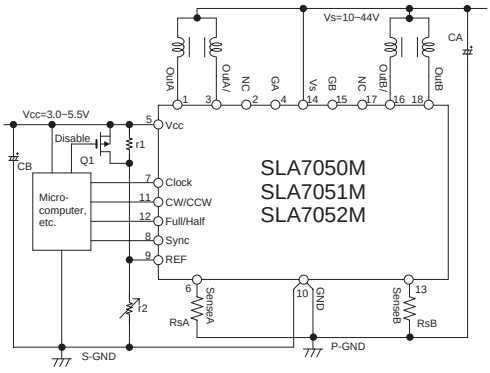
Pin No.	Symbol	Function
1	OutA	Phase A output
2	NC	No Connection
3	OutA/	Phase $\overline{A}$ output
4	GA	No Connection
5	V_{CC}	Logic supply
6	SenseA	Phase A current sense
7	Clock	Step Clock input
8	Sync	Synchronous PWM control signal input
9	Ref	Control current setting & output OFF
10	GND	Device GND
11	CW/CCW	Normal/reverse control input
12	Full/Half	Full/Half Step control input
13	SenseB	Phase B current sense
14	V_S	Load supply (motor supply)
15	GB	No Connection
16	OutB/	Phase $\overline{B}$ output
17	NC	No Connection
18	OutB	Phase B output

Truth Table

	L	H
CW/CCW	CW	CCW
Full/Half	Full	Half
REF	Enable	Disable
Sync	Asynchronous	Synchronous
Clock		

* REF terminal turns into normal operation at VREF < 1.5V.
The output is disabled (Output OFF) at VREF > 2V.

■Typical Connection Diagram

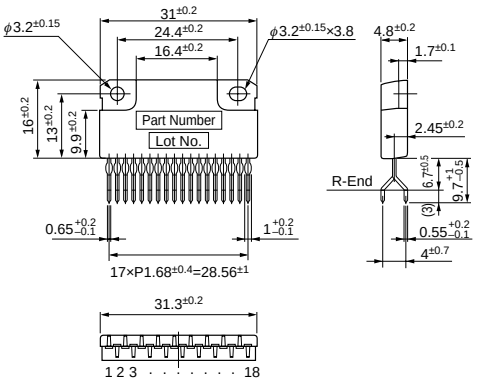


Rs=0.1 to 2Ω (Power dissipation should be: P≒Io² × Rs)
R1=10kΩ CA=100μF/50V
R2=5.1kΩ (VR) CB=10μF/10V
Q1:T.B.D

* V_{CC} line noise precaution:
The device may malfunction if the V_{CC} line noise exceeds 0.5V.
* Be sure to connect the unused logic input terminals (CW/CCW, F/H, Sync) to V_{CC} or GND. If they are open, the device will malfunction.
* GND pattern precaution:
Separating the V_{CC} system GND (S-GND) and V_S system GND (P-GND) from the device GND (10-Pin) helps to reduce noise.

■External Dimensions (ZIP18 with Fin [SLA18Pin])

(Unit : mm)



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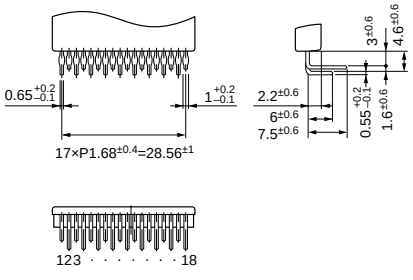

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Product Mass : Approx.6g