

QUAD BILATERAL SWITCH

- **HIGH SPEED:**
 $t_{PD} = 0.4 \text{ ns}$ (TYP.) at $V_{CC} = 3.3 \text{ V}$
 $t_{PD} = 0.1 \text{ ns}$ (TYP.) at $V_{CC} = 5 \text{ V}$
- **LOW POWER DISSIPATION:**
 $I_{CC} = 2\mu\text{A}$ (MAX.) at $T_A = 25^\circ\text{C}$
- **LOW "ON " LOW RESISTANCE**
 $R_{ON} = 14\Omega$ at $V_{CC} = 3.3\text{V}$, $I_{I/O} \leq 1 \text{ mA}$
 $R_{ON} = 12\Omega$ at $V_{CC} = 5.0\text{V}$, $I_{I/O} \leq 1 \text{ mA}$
- **SINE WAVE DISTORTION:**
 0.04% at $V_{CC} = 3.3\text{V}$, $f = 1\text{KHz}$
- **OPERATING VOLTAGE RANGE:**
 $V_{CC(OPR)} = 2\text{V to } 5.5\text{V}$
- **PIN AND FUNCTION COMPATIBLE WITH**
74 SERIES 4066
- **IMPROVED LATCH-UP IMMUNITY**

DESCRIPTION

The 74LVQ4066 is a low voltage CMOS QUAD BILATERAL SWITCH fabricated with sub-micron silicon gate and double-layer metal wiring C²MOS technology.

It is ideal for low power and low noise 3.3V applications and each switch is designed to handle both analog and digital signals.

The switches permit signals with amplitudes up to V_{CC} (peak) to be transmitted in either direction

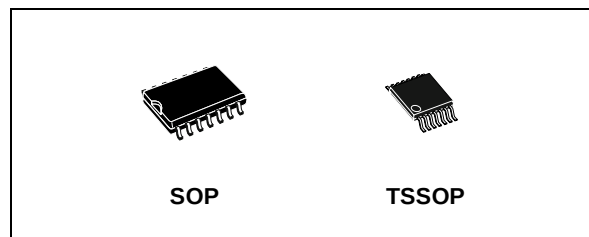


Table 1: Order Codes

PACKAGE	T & R
SOP	74LVQ4066MTR
TSSOP	74LVQ4066TTR

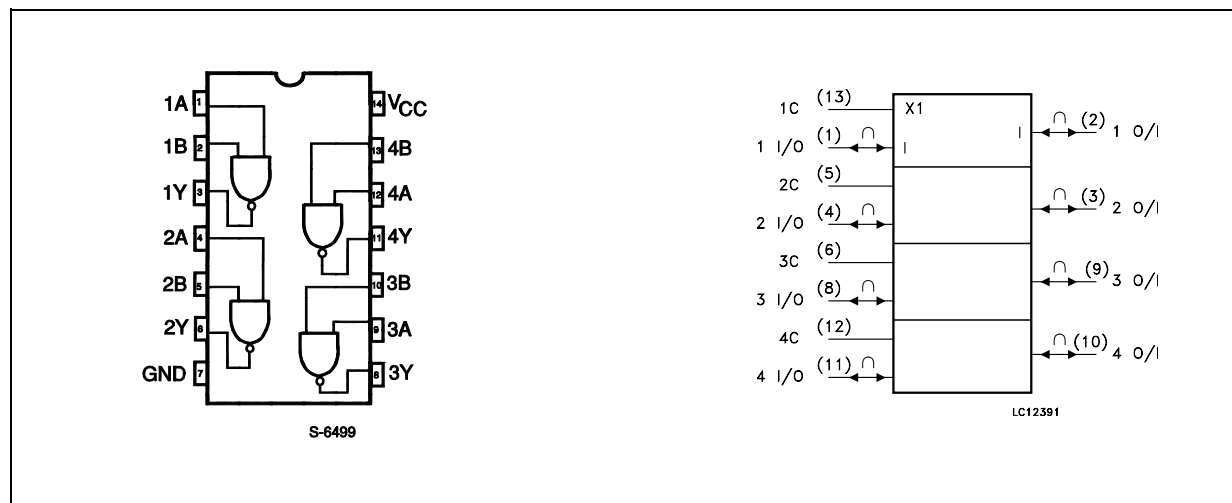
without relevant propagation delay and without generating additional ground bounce noise.

It has an ON-Resistance which is greatly reduced in comparison with 74HC4066.

It is provided of four individual enable inputs to control the switches; the switch is ON when the C input is held high and OFF (High Impedance) when C is held low.

All inputs and outputs are equipped with protection circuits against static discharge, giving them ESD immunity and transient excess voltage.

Figure 1: Pin Connection And IEC Logic Symbols



The diagram illustrates the internal logic of the LC12380 microcontroller. It features three main input/output pins: **I/O**, **C IN**, and **O/I**. The logic consists of several interconnected components:

- I/O Pin:** Connected to a 4-input AND gate. One input of this AND gate is also connected to the **O/I** pin.
- C IN Pin:** Connected to a NOT gate, followed by a 2-input AND gate. The output of this AND gate is connected to a 3-input AND gate.
- O/I Pin:** Connected to a 4-input AND gate. The output of this AND gate is connected to a NOT gate, which then feeds into a 3-input AND gate.
- Internal Connections:**
 - The output of the first NOT gate (from C IN) is connected to a 2-input AND gate, which also receives input from the I/O pin.
 - The output of the second NOT gate (from O/I) is connected to a 2-input AND gate, which also receives input from the I/O pin.
 - The output of the third NOT gate (from the second 3-input AND gate) is connected to a 2-input AND gate, which also receives input from the I/O pin.

The final output of the logic is connected to the **O/I** pin.

PIN N°	SYMBOL	NAME AND FUNCTION
1, 4, 8, 11	1 to 4 I/O	Independent Input/Output
2, 3, 9, 10	1 to 4 O/I	Independent Output/Input
13, 5, 6, 12	1C to 4C	Enable Input (Active HIGH)
7	GND	Ground (0V)
14	V _{CC}	Positive Supply Voltage

A	B
H	ON
L	OFF*

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
V_O	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 50	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 200	mA
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Table 5: Recommended Operating Conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (note 1)	2 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature	-55 to 125	°C
dt/dv	Input Rise and Fall Time on control pin $V_{CC} = 3.0V$ (note 2)	0 to 10	ns/V

2) V_{IN} from 30% to 70% V_{CC}

Table 6: DC Specifications

Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V _{IH}	High Level Input Voltage	2.7 to		0.7 V _{CC}			0.7 V _{CC}		0.7 V _{CC}		V
V _{IL}	Low Level Input Voltage	5.5				0.3 V _{CC}		0.3 V _{CC}		0.3 V _{CC}	V
R _{ON}	ON Resistance	3.3 (**)	V _I =V _{IH} V _{I/O} =V _{CC} to GND		16.5	23		32		40	Ω
		5.0(*)	I _{I/O} ≤ 1mA		12	17		22		26	
		3.3 (**)	V _I =V _{IH} V _{I/O} =V _{CC} or GND		12	17		24		30	
		5.0(*)	I _{I/O} ≤ 1mA		9.5	13		17		20	
R _{ON}	Difference of ON Resistance Between Switches	3.0 to 5.5	V _I =V _{IH} V _{I/O} =V _{CC} to GND I _{I/O} ≤ 1mA		2						Ω
I _{OFF}	Input/Output Leakage Current (SWITCH OFF)	5.5	V _{OS} = V _{CC} to GND V _{IS} = V _{CC} to GND V _I = V _{IL}			± 0.1		± 1.0		± 1.0	μA
I _{IZ}	Switch Input Leakage Current (SWITCH ON, OUTPUT OFF)	5.5	V _{OS} = V _{CC} to GND V _I = V _{IH}			± 0.1		± 1.0		± 1.0	μA
I _{IN}	Control Input Leakage Current	5.5	V _I = V _{CC} or GND			± 0.1		± 1.0		± 1.0	μA
I _{CC}	Quiescent Supply Current	5.5	V _I = V _{CC} or GND			2		20		20	μA

(*)Voltage range is 5V ±0.5V

(**)Voltage range is 3.3V ±0.3V

Table 7: AC Electrical Characteristics ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 3\text{ns}$)

Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t _{PD}	Delay Time	3.3(*)			0.4	0.8		1.2		2.0	ns
		5.0 (**)			0.1	0.2		1.0		1.8	
t _{PZL} t _{PZH}	Output Enable Time	3.3(*)	R _L = 1 kΩ		2.5	4.0		5.0		7.0	ns
		5.0 (**)			2.0	4.0		5.0		7.0	
t _{PLZ} t _{PHZ}	Output Disable Time	3.3(*)	R _L = 1 kΩ		5.0	7.5		9.0		11.0	ns
		5.0 (**)			5.0	7.5		9.0		11.0	
C _{IN}	Input Capacitance				5						pF
C _{I/O}	Switch Terminal Capacitance				10						pF
C _{PD}	Power Dissipation Capacitance (note 1)	3.3			2.5						pF
		5.0			3						

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/4$ (Switch).

(*) Voltage range is $3.3\text{V} \pm 0.3\text{V}$

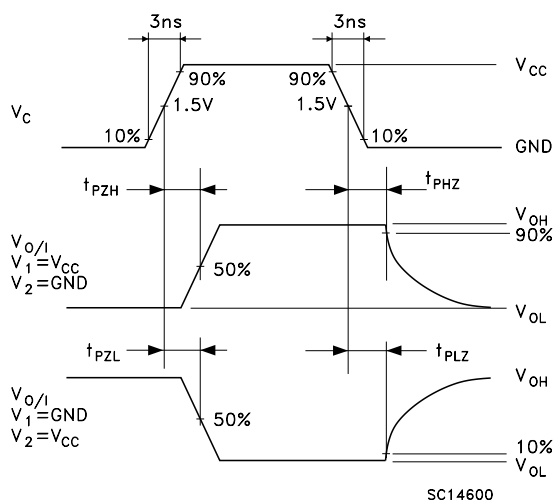
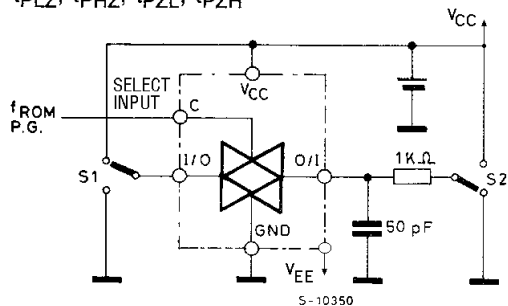
(*) Voltage range is $5\text{V} \pm 0.5\text{V}$

Table 8: Analog Switch Characteristics ($\text{GND} = 0 \text{ V}$, $T_A = 25^\circ\text{C}$)

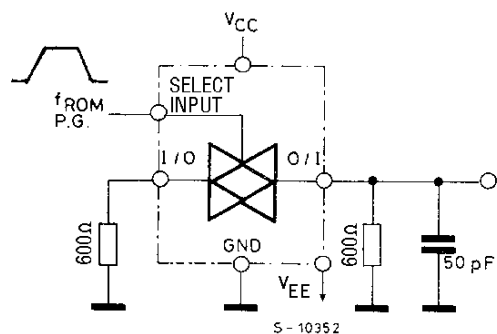
Symbol	Parameter	Test Condition			Value	Unit	
		V _{CC} (V)	V _{IN} (V _{p-p})				
	Sine Wave Distortion (THD)	3.3	2.75	f _{IN} = 1 KHz R _L = 10KΩ C _L = 50 pF	0.04	%	
		5.0(*)	4		0.04		
f _{MAX}	Frequency Response (Switch ON)	3.3	Adjust f _{IN} voltage to Obtain 0dBm at V _{OS} . Increase f _{IN} Frequency until dB Meter reads -3dB R _L = 50Ω , C _L = 10pF			150	MHz
		5.0(*)				180	
	Feed through Attenuation (Switch OFF)	3.3	V _{IN} is centered at V _{CC} /2. Adjust input for 0dBm R _L = 600Ω, C _L = 50pF, F _{IN} = 1 MHz sine wave			-60	dB
		5.0(*)				-60	
	Crosstalk (Control Input to Signal Output)	3.3	R _L = 600Ω, C _L = 50pF, f _{IN} = 1MHz square wave			60	mV
		5.0(*)				60	
	Crosstalk (Between Any Switches)	3.3	R _L = 600Ω, C _L = 50pF, f _{IN} = 1MHz sine wave			-60	dB
		5.0(*)				-60	

(*) Voltage range is $5\text{V} \pm 0.5\text{V}$

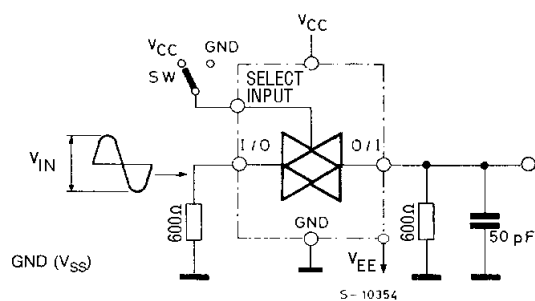
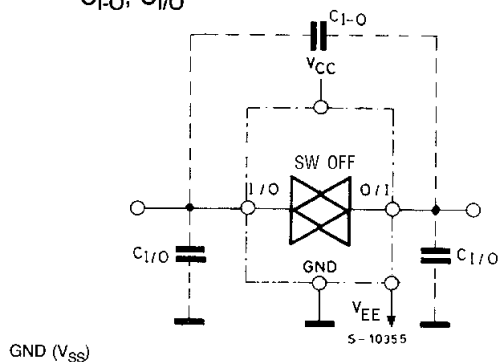
Figure 3: Switching Characteristics Test Circuit

 t_{PLZ} , t_{PHZ} , t_{PZL} , t_{PZH} 

CROSSTALK (control to output)



BANDWIDTH AND FEEDTHROUGH ATTENUATION

 $C_{I/O}$, $C_{I/O}$ 

MAXIMUM CONTROL FREQUENCY

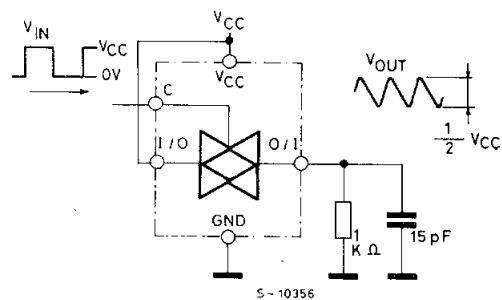


Figure 4: Channel Resistance (R_{ON})

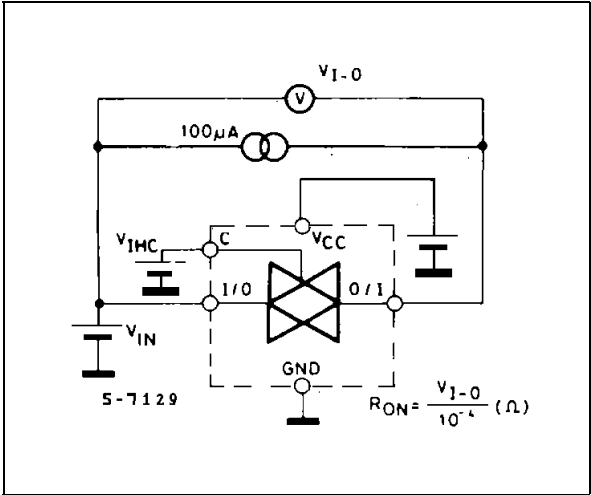
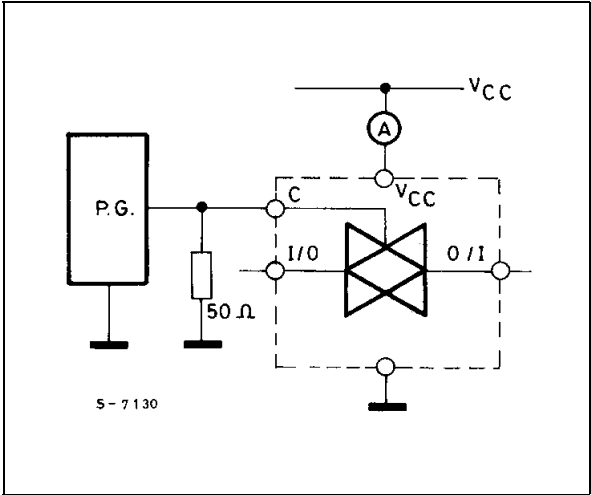
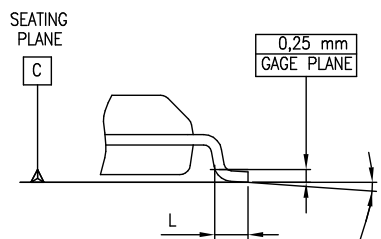
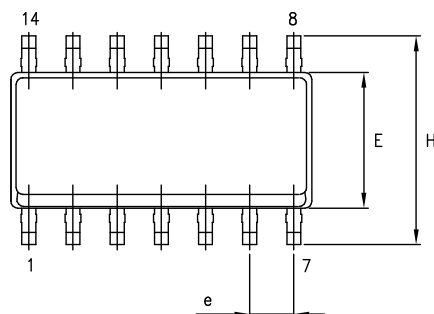
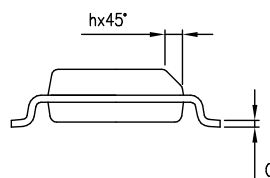
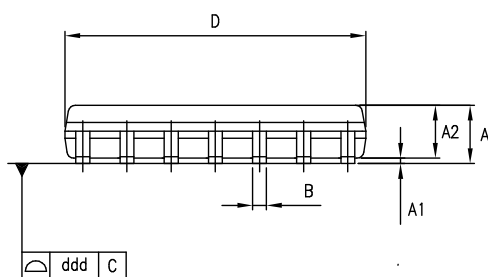


Figure 5: I_{CC} (Opr.)



SO-14 MECHANICAL DATA

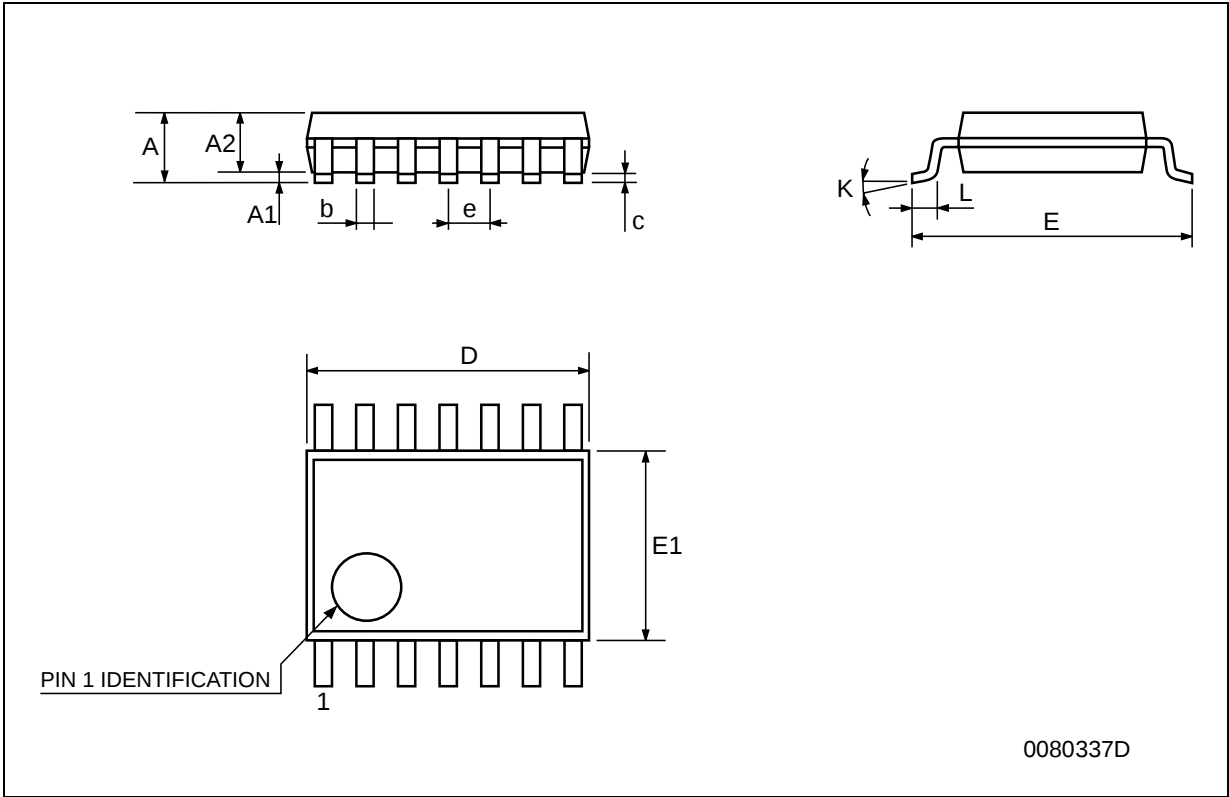
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	1.35		1.75	0.053		0.069
A1	0.1		0.25	0.004		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D	8.55		8.75	0.337		0.344
E	3.8		4.0	0.150		0.157
e		1.27			0.050	
H	5.8		6.2	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.4		1.27	0.016		0.050
k	0°		8°	0°		8°
ddd			0.100			0.004



0016019D

TSSOP14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



Tape & Reel SO-14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.4		6.6	0.252		0.260
Bo	9		9.2	0.354		0.362
Ko	2.1		2.3	0.082		0.090
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319



Tape & Reel TSSOP14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.7		6.9	0.264		0.272
Bo	5.3		5.5	0.209		0.217
Ko	1.6		1.8	0.063		0.071
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319



Table 9: Revision History

Date	Revision	Description of Changes
29-Jul-2004	8	Ordering Codes Revision - pag. 1.

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