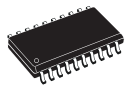
L9826

Octal Low-Side Driver for Resistive and Inductive Loads with Serial/Parallel Input Control, Output Protection and Diagnostic

Features

- OUTPUTS CURRENT CAPABILITY UP TO 450mA
- TYPICAL R_{ON} = 1.5Ω AT T_J = 25°C
- PARALLEL CONTROL INPUTS FOR OUTPUTS 1 AND 2
- SPI CONTROL FOR OUTPUTS 1 TO 8
- RESET FUNCTION WITH RESET SIGNAL AT NRES PIN OR UNDERVOLTAGE AT V_{CC}
- INTRINSIC OUTPUT VOLTAGE CLAMPING AT TYP. 50V
- OVERCURRENT SHUTDOWN AT OUTPUTS 3 TO 8
- SHORT CIRCUIT CURRENT LIMITATION AND SELECTIVE THERMAL SHUTDOWN AT OUTPUTS 1 AND 2
- OUTPUT STATUS DATA AVAILABLE ON THE SPI



SO20

Description

The L9826 is a Octal Low-Side Driver Circuit, dedicated for automotive applications. Output voltage clamping is provided for flyback current recirculation, when inductive loads are driven. Chip Select and Serial Peripheral Interface for outputs control and diagnostic data transfer. Parallel Control inputs for two outputs.

.

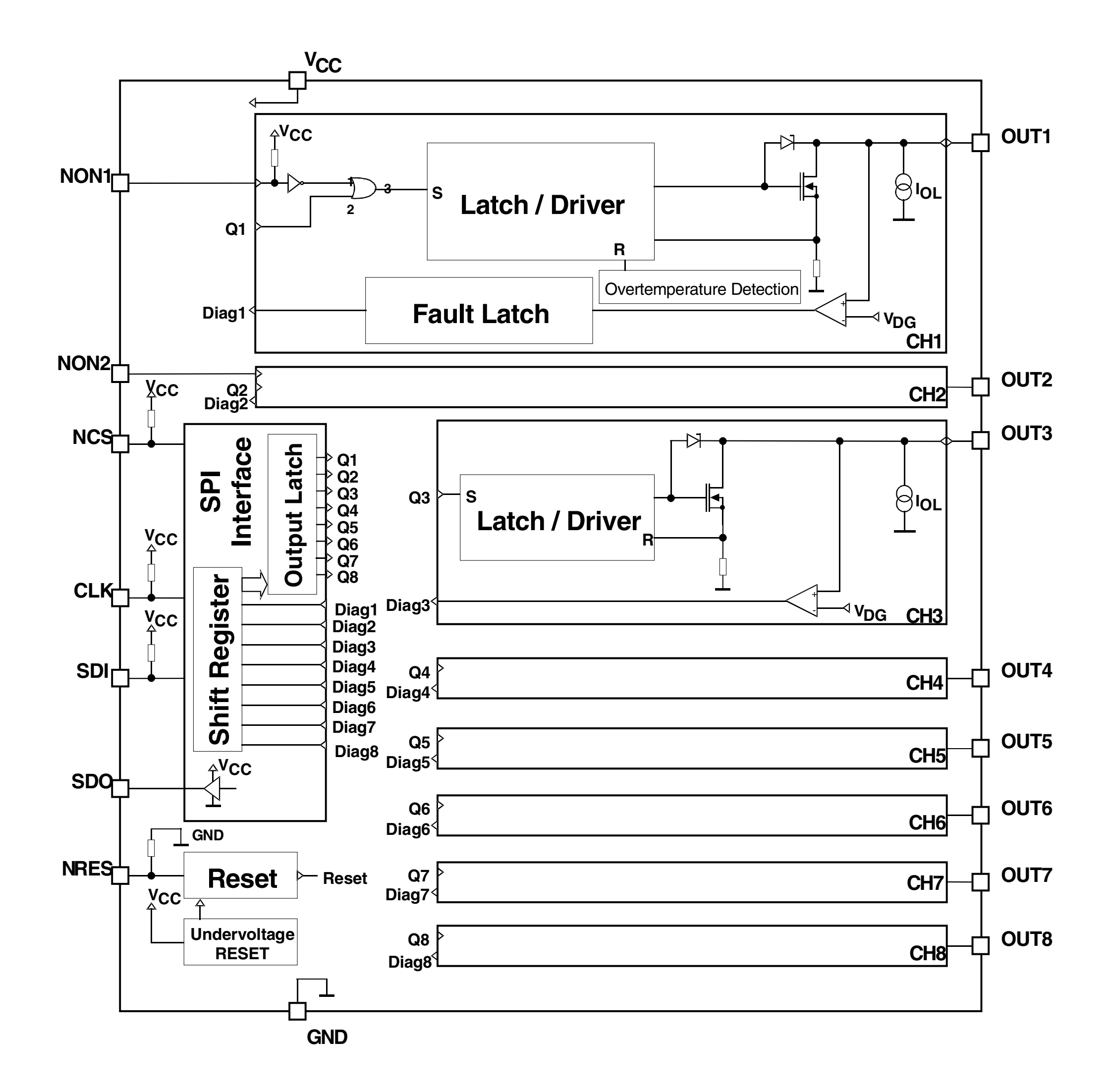
Order codes

Part number	Temp range, °C	Package	Packing
L9826		SO20 (16+2+2)	Tube
L9826TR		SO20	Tape & Reel

Contents

1 Block Diagram

Figure 1. Block diagram



2 Pins Description and Connection Diagrams

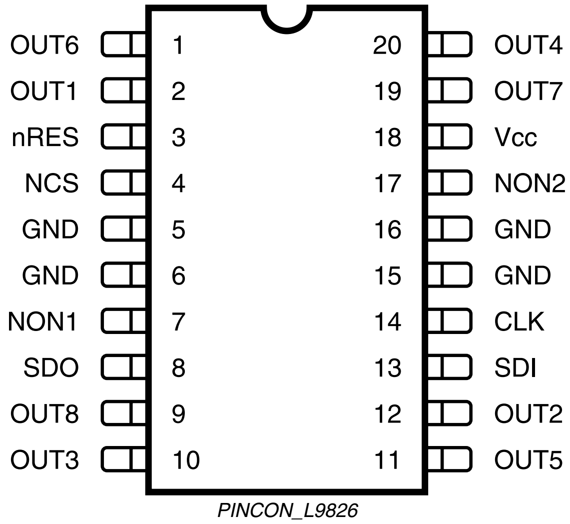
2.1 Pin description

Table 1. Pin description

N°	Pin	Description
1	Out 6	output 6
2	Out 1	output 1
3	NRes	asynchronous reset
4	NCS	chip select (active low)
5	GND	device ground
6	GND	device ground
7	NON1	control input 1
8	SDO	serial data output
9	Out 8	output 8
10	Out 3	output 3
11	Out 5	output 5
12	Out 2	output 2
13	SDI	serial data input
14	CLK	serial clock
15	GND	device ground
16	GND	device ground
17	NON2	control input 2
18	V_{CC}	supply voltage
19	Out 7	output 7
20	Out 4	output 4

2.2 Pins connection

Figure 2. Connection diagram



2.3 Thermal data

Table 2. Thermal data

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Thermal shutdown						
T_{JSC}	Thermal shutdown threshold		150	165		°C
Thermal resistance						
$R_{thjA\text{-}one}$	Single output (junction ambient)				90	°C/W
$R_{thjA\text{-}all}$	All outputs (junction ambient)				75	°C/W
$R_{thj\text{-}pin}$	Junction to Pin				18	°C/W

3 Electrical Specifications

3.1 Absolute maximum ratings

Table 3. For voltages and currents applied externally to the device

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		-0.3		7	V
Inputs and data lines (NONx, NCS, CLK, SDI, nRes)						
V_{IN}	Voltage (NONx, NCS, CLK, SDI, nRes)		-0.3		7	V
I_{IN}	Protection diodes current [1)]	$T \leq 1ms$	-20		20	mA
Outputs (Out1 ... Out8)						
V_{OUTc}	Continuous output voltage		-0.7		45	V
I_{OUT}	Output current [2)]		-2		1.0	A
E_{OUTcl}	Output clamp energy	$I_{OUT} \leq 150mA$			10	mJ

Note: 1 All inputs are protected against ESD according to MIL 883C; tested with HBM at 2KV. It corresponds to a dissipated energy $E \leq 0{,}2mJ$.

2 Transient pulses in accordance to DIN40839 part 1, 3 and ISO 7637 Part 1, 3.

Figure 3. For currents determined within the device:

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Outputs (Out1 ... Out8)						
I_{OUT}	Output current (Out1, Out2)				I_{LIM}	A
	Output current (Out3 ... Out8)				I_{SCB}	A
ΣI_{OUT1} i = 1-8	Total average-current all outputs [3)]	$T_{amb} = 60°C$	2.0			A

3 When operating the device with short circuit at more than 2 outputs at the same time, damage due to electrical overstress may occur.

3.2 Electrical characteristics

Table 4. Electrical Characteristcs
($4.5V \le V_{CC} \le 5{,}5V$; $-40°C \le T_J \le 150°C$; unless otherwise specified).

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Supply voltage						
I_{ccSTB}	Standby current	without load (nRes = Low)			70	µA
I_{ccOPM}	Operating mode	$I_{OUT1 ... 8}$ = 500mA SPI - CLK = 3MHz NCS = LOW SDO no load			5	mA
ΔI_{CC}	ΔI_{CC} during reverse output current	I_{out} = -2A			100	mA
V_{DDRES}	Undervoltage Reset	Reset of all registers and disable of all outputs	3		4	V
Inputs (NONx. NCS, CLK, SDI, nRes)						
V_{INL}	Low level		-0.3		$0.2{\cdot}V_{CC}$	V
V_{INH}	High level		$0.7{\cdot}V_{CC}$		V_{CC} +0,3	V
V_{hyst}	Hysteresis voltage		0.85			V
I_{IN}	Input current	NONx, NCS, CLK, SDI $V_{IN} = V_{CC}$			10	µA
		NRES (V_{IN} = 0V)	-10			µA
R_{IN}	Pullup resistance	(NONx, NCS, CLK, SDI) Pulldown resistance (NRes)	50		250	kΩ
C_{IN}	Input capacitance	Guaranteed by design			10	pF
Serial data outputs						
V_{SDOH}	High output level	I_{SDO} = -4mA	V_{CC} -0.4			V
V_{SDOL}	Low output level	I_{SDO} = 3,2mA			0.4	V
I_{SDOL}	Tristate leakage current	NCS = high; $0V \le V_{SDO} \le V_{CC}$	-10		10	µA
C_{SDO}	Output capacitance	f_{SDO} = 300kHz, Guaranteed by design			10	pF
Outputs OUT 1 ... 8						
$I_{OUTL1-8}$	Leakage current	OUTx = OFF; V_{OUTx} = 25V; V_{CC} = 5V			100	µA
$I_{OUTL1-8}$	Leakage current	OUTx = OFF; V_{OUTx} = 16V; V_{CC} = 5V			100	µA

Table 4. Electrical Characteristcs (continued)
($4.5V \le V_{CC} \le 5{,}5V$; $-40°C \le T_J \le 150°C$; unless otherwise specified).

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$I_{OUTL1-8}$	Leakage current	OUTx = OFF; V_{OUTx} = 16V; V_{CC} = 1V			10	µA
V_{clp}	Output clamp voltage	$1mA \le I_{clp} \le I_{outp}$; I_{test} = 10mA with correlation	45		62	V
R_{DSon}	On resistance OUT 1 ... 8	I_{OUT} = 250mA; T_j = +150°C			3.0	Ω
C_{OUT}	Output capacitance	V_{OUT} = 16V; f = 1MHz guaranteed by design			300	pF
Outputs short circuit protection						
I_{SBC}	Overcurrent shutoff threshold	OUT3 ... OUT8	0.45		1.1	A
I_{LIM}	Short circuit current limitation	OUT1; OUT2	0.5		1.1	A
t_{SCB}	Delay shutdown		0.2	3,0	12	µs
Diagnostics						
V_{DG}	Diagnostic threshold voltage		$0.32 \cdot V_{CC}$		$0.4 \cdot V_{CC}$	V
I_{OL}	Open load detection sink current	$V_{out} = V_{DG}$	20		100	µA
t_{df}	Diagnostic detection filter time	for output 1 & 2 on each diagnostic condition	15		50	µs
Outputs timing						
t_{don1}	Turn ON delay of OUT 1 and 2	$NON_{1,2}$ = 50% to $V_{OUT} = 0{,}9 \cdot V_{bat}$ NCS = 50% to $V_{OUT} = 0{,}9 \cdot V_{bat}$ (V_{BAT} = 16V, R_L = 500Ω)			5	µs
t_{don2}	Turn ON delay of OUT 3 to 8	NCS = 50% to $V_{OUT} = 0{,}9 \cdot V_{bat}$ (V_{BAT} = 16V, R_L = 500Ω)			10	µs
t_{doff}	Turn OFF delay of OUT 1 to 8	NCS = 50% to $V_{OUT} = 0{,}1 \cdot V_{bat}$ $NON_{1,2}$ = 50% to $V_{OUT} = 0{,}1 \cdot V_{bat}$ (V_{BAT} = 16V, R_L = 500Ω)			10	µs
$dU_{on1/dt}$	Turn ON voltage slew-rate	For output 3 to 8; 90% to 30% of V_{bat}; R_L = 500Ω; V_{bat} = 16V	0.7		3.5	V/µs
$dU_{on2/dt}$	Turn ON voltage slew-rate	For output 1 and 2; 90% to 30% of V_{bat}; R_L = 500Ω; V_{bat} = 16V	2		10	V/µs
$dU_{off1/dt}$	Turn OFF voltage slew-rate	For output 1 to 8; 30% to 90% of V_{bat}; R_L = 500Ω; V_{bat} = 16V	2		10	V/µs
$dU_{off2/dt}$	Turn OFF voltage slew-rate	For output 1 to 8; 30% to 80% of V_{bat}; R_L = 500Ω; $V_{bat} = 0.9 \cdot V_{clp}$	2		15	V/µs
Serial diagnostic link (Load capacitor at SDO = 100pF)						

Table 4. Electrical Characteristcs (continued)
(4.5V ≤ V_{CC} ≤ 5,5V; -40°C ≤ T_J ≤ 150°C; unless otherwise specified).

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
f_{clk}	Clock frequency	50% duty cycle			3	MHz
t_{clh}	Minimum time CLK = HIGH		160			ns
t_{cll}	Minimum time CLK = LOW		160			ns
t_{pcld}	Propagation delay CLK to data at SDO valid	4,9V ≤ V_{CC} ≤ 5,1V			100	ns
t_{csdv}	NCS = LOW to data at SDO active				100	ns
t_{sclch}	CLK low before NCS low	Setup time CLK to NCS change H/L	100			ns
t_{hclcl}	CLK change L/H after NCS = low		100			ns
t_{scld}	SDI input setup time	CLK change H/L after SDI data valid	20			ns
t_{hcld}	SDI input hold time	SDI data hold after CLK change H/L			20	ns
t_{sclcl}	CLK low before NCS high		150			ns
t_{hclch}	CLK high after NCS high		150			ns
t_{pchdz}	NCS L/H to output data float				100	ns
	NCS pulse filter time	Multiple of 8 CLK cycles inside NCS period				

4 Functional Description

4.1 General

The L9826 integrated circuit features 8 power low-side-driver outputs. Data is transmitted to the device using the Serial Peripheral Interface, SPI protocol. Outputs 1 and 2 can be controlled parallel or serial. The power outputs features voltage clamping function for flyback current recirculation and are protected against short circuit to Vbat.

The diagnostics recognizes two outputs fault conditions: 1) overcurrent for outputs 3 to 8 , overcurrent and thermal overload for outputs 1 and 2 in switch-on condition and 2) open load or short to GND in switch-off condition for all outputs. The outputs status can be read out via the serial interface.

The chip internal reset is a OR function of the external nRes signal and internally generated undervoltage nRes signal.

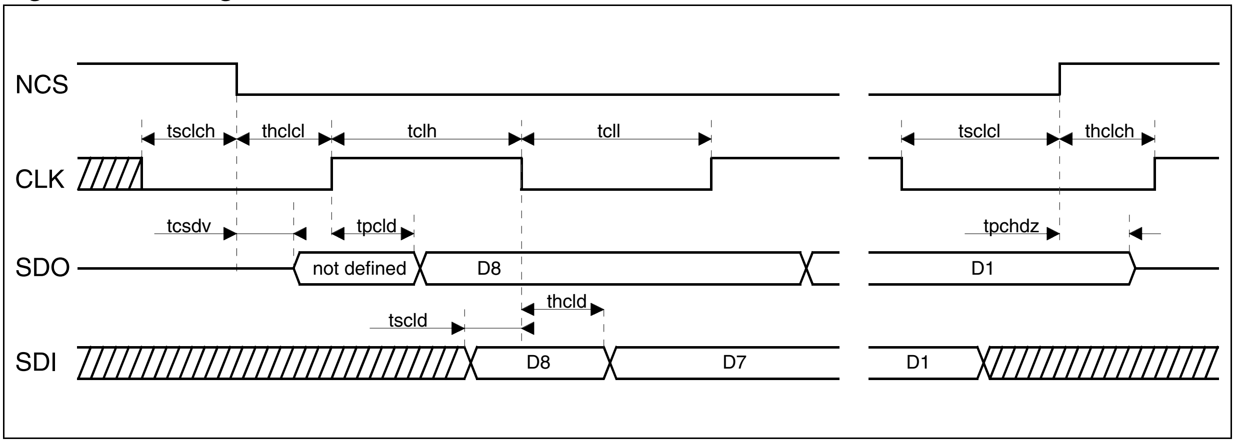
4.2 Output Stages Control

Each output is controlled with its latch and with common reset line, which enables all eight outputs. Outputs 1 and 2 can be controlled also by its NON1, NON2 inputs. It allows PWM control independently on the SPI. These inputs features internal pull-up resistors to assure that the outputs are switched off, when the inputs are open.

The control data are transmitted via the SDI input, the timing of the serial interface is shown in *Figure 4.*.

The device is selected with low NCS signal and the input data are transferred into the 8 bit shift register at every falling CLK edge. The rising edge of the NCS latches the new data from the shift register to the drivers.

Figure 4. Timing of the Serial Interface



The SPI register data are transferred to the output latch at rising NCS edge. The digital filter between NCS and the output latch ensures that the data are transferred only after 8 CLK cycles or multiple of 8 CLK cycles since the last NCS falling edge. The NCS changes only at low CLK.

Outputs Control Tables :

Table 5.

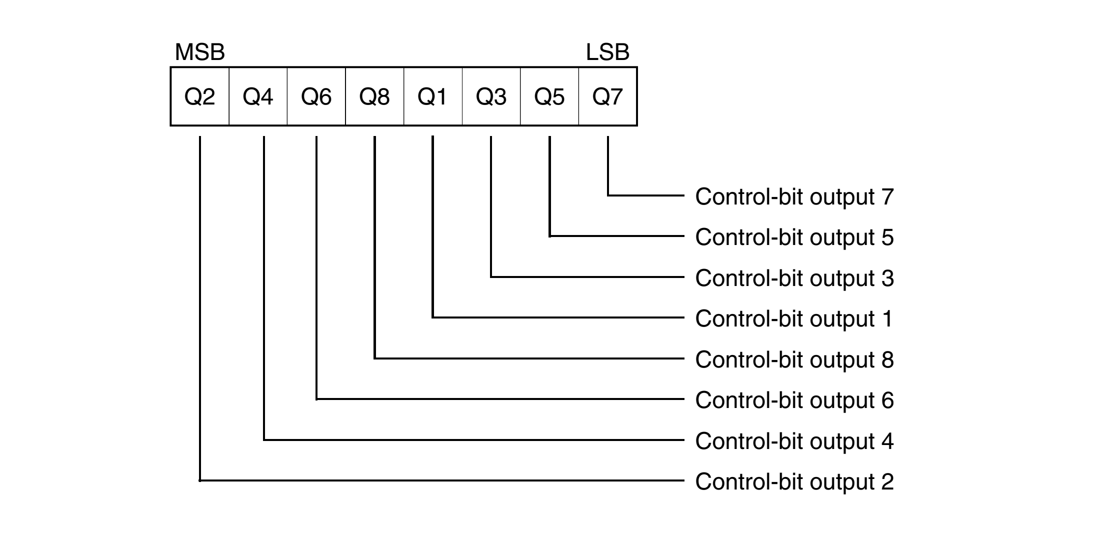
Outputs 1, 2:

NON1, 2	1	0	0	1
SPI-bit 1, 2	0	0	1	1
Output 1, 2	off	on	on	on

Outputs 3 to 8:

SPI-bit 3 ... 8	0	1
Output 3 ... 8	off	on

Figure 5. Output control register structure



4.3 Power outputs characteristics

for flyback current, outputs short circuit protection and diagnostics

For output currents flowing into the circuit the output voltages are limited. The typical value of this voltage is 50V. This function allows that the flyback current of a inductive load recirculates into the circuit; the flyback energy is absorbed in the chip.

Output short circuit protection for outputs 3 to 8 (dedicated for loads without inrush current): when the output current exceeds the short circuit threshold, the corresponding output overload latch is set and the output is switched off immediately.

Output short circuit protection for outputs 1 and 2 (dedicated for loads with inrush current, as lamps): when the load current would exceed the short circuit limit value, the corresponding output goes in a current regulation mode.

The output current is determined by the output characteristics and the output voltage depends on the load resistance. In this mode high power is dissipated in the output transistor and its temperature increases rapidly. When the power transistor temperature exceeds the thermal shutdown threshold, the overload latch is set and the corresponding output switched off.

For the load diagnostic in output off condition each output features a diagnostic current sink, typ 60µA.

4.4 Diagnostics

The output voltage at all outputs is compared with the diagnostic threshold, typ 0,38 · V_{CC}.

Outputs 1 and 2 features dedicated fault latches. The output status signal is filtered and latched. The fault latches are cleared during NCS low. The latch stores the status bit, so the first reading after the error occurred might be wrong. The second reading is right.

Table 6. Diagnostic Table for outputs 1 and 2 in parallel controlled mode:

Output 1, 2	Output-voltage	Status-bit	Output-mode
off	> DG-threshold	high	correct operation
off	< DG-threshold	low	fault condition 2)
on	< DG-threshold	high	correct operation
on	> DG-threshold	low	fault condition 1)

Fault condition 1) "output short circuit to Vbat" : the output was switched on and the voltage at the output exceeds the diagnostics threshold. The output operates in current regulation mode or has been switched off due to thermal shutdown. The status bit is low.

Fault condition 2) "open load" or "output short circuit to GND" : the output is switched off and the voltage at the output drops below the diagnostics threshold, because the load current is lower than the output diagnostic current source, the load is interrupted. The diagnostic bit is low.

For outputs 3 to 8 the output status signals, are fed directly to the SPI register.

Table 7. Diagnostic Table for outputs 1 to 8 in SPI controlled mode:

Output 1 ... 8	Output-voltage	Status-bit	Output-mode
off	> DG-threshold	high	correct operation
off	< DG-threshold	low	fault condition 2)
on	< DG-threshold	low	correct operation
on	> DG-threshold	high	fault condition 1)

The fault condition 1) "output short circuit to Vbat" : the output was switched on and the voltage at the output exceeded the diagnostics threshold due to overcurrent, the output overload latch was set and the output has been switched off. The diagnostic bit is high.

Fault condition 2) "open load" or "output short circuit to GND" is the same as of outputs 1 and 2. At the falling edge of NCS the output status data are transferred to the shift register.

When NSC is low, data bits contained in the shift register are transferred to SDO output et every rising CLK edge.

Figure 6. The Pulse Diagram to Read the Outputs Status Register

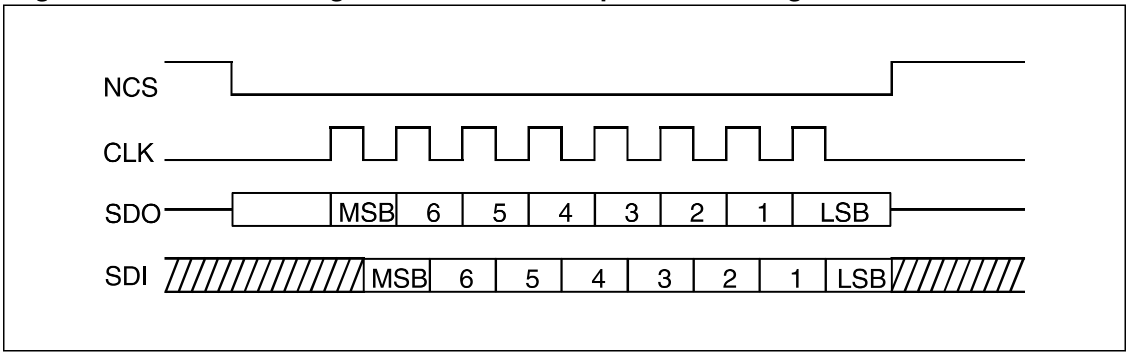
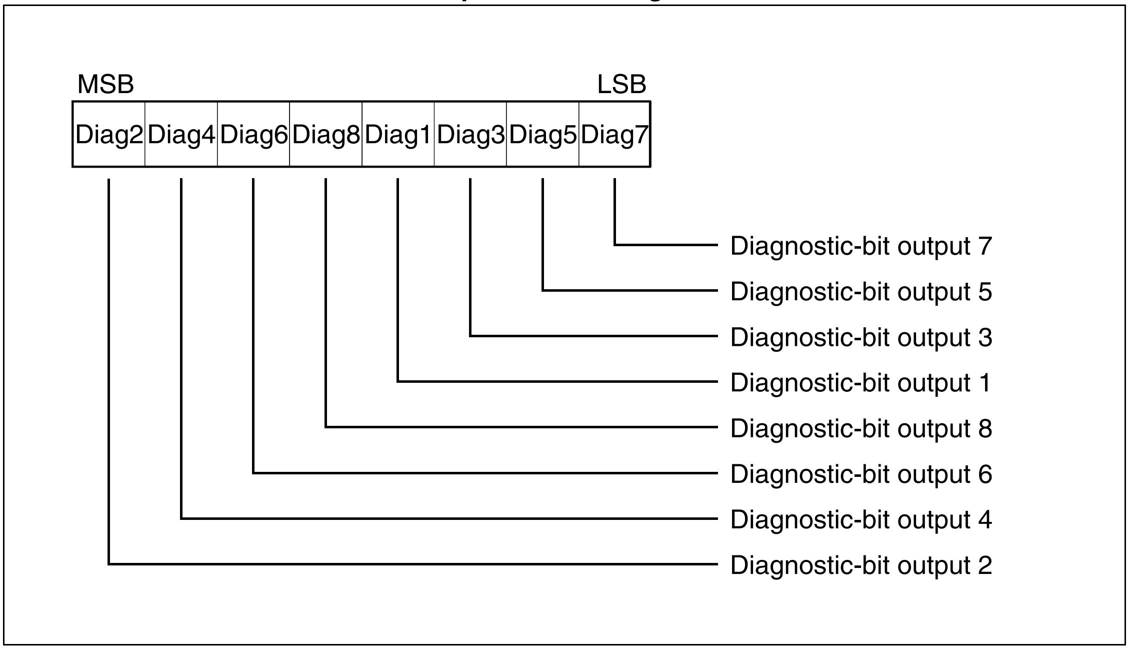


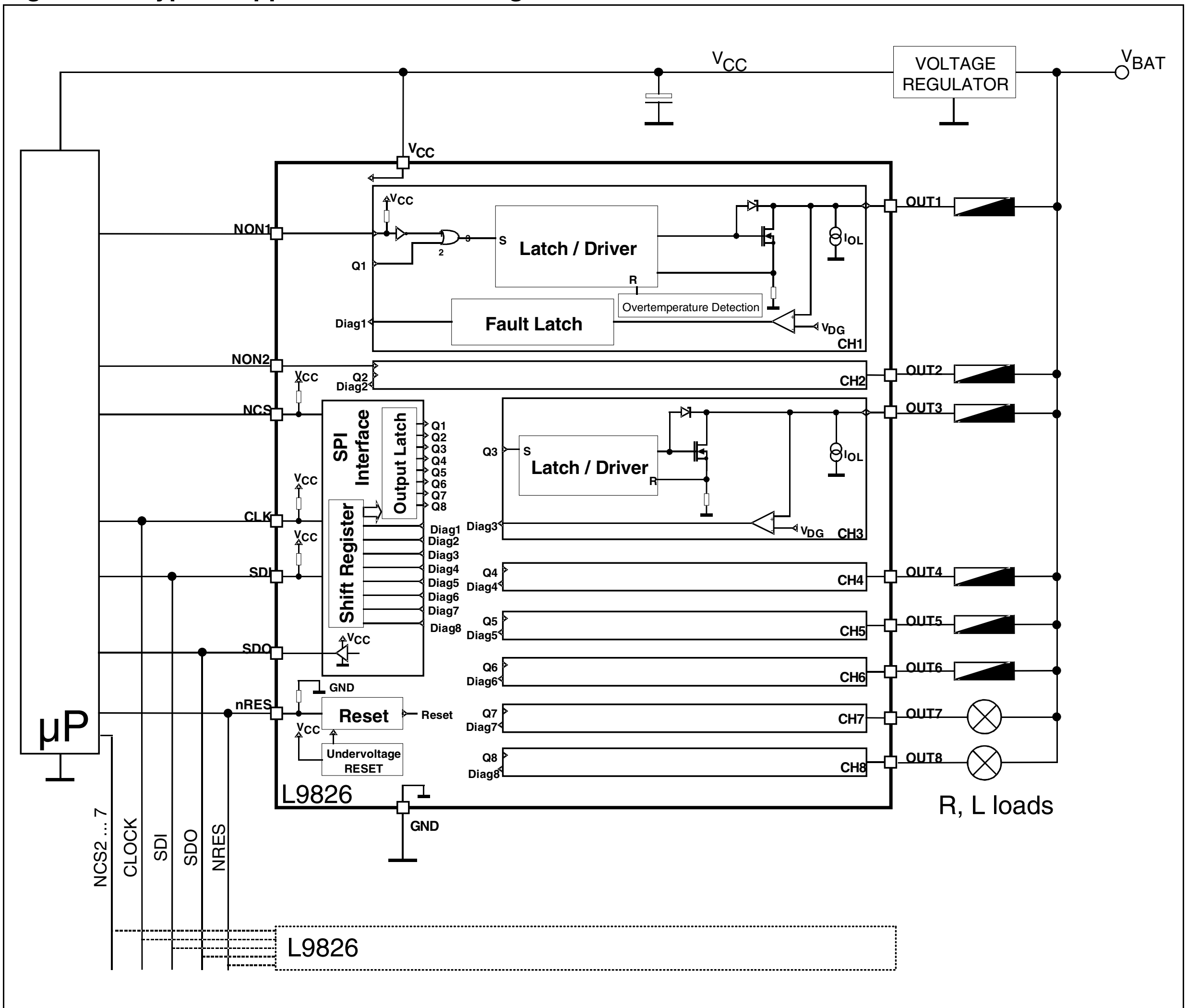
Table 8. The Structure of the Outputs Status Register



5 Application Information

The typical application diagram is shown in *Figure 7.*.

Figure 7. Typical Application Circuit Diagram for the L9826 Circuit



For higher current driving capability two outputs of the same kind can be paralleled. In this case the maximum flyback energy should not exceed the limit value for single output.

The immunity of the circuit with respect to the transients at the output is verified during the characterization for Test Pulses 1, 2 and 3a, 3b, DIN40839 or ISO7637 part 3. The Test Pulses are coupled to the outputs with 200pF series capacitor. All outputs withstand testpulses without damage.

The correct function of the circuit with the Test Pulses coupled to the outputs is verified during the characterization for the typical application with R = 30Ω to 100Ω, L= 0 to 600mH loads. The Test Pulses are coupled to the outputs with 200pF series capacitor.

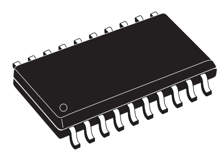
6 Package Informations

Figure 8. PowerSO20 Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.35		2.65	0.093		0.104
A1	0.10		0.30	0.004		0.012
B	0.33		0.51	0.013		0.200
C	0.23		0.32	0.009		0.013
D (1)	12.60		13.00	0.496		0.512
E	7.40		7.60	0.291		0.299
e		1.27			0.050	
H	10.0		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

(1) "D" dimension does not include mold flash, protusions or gate burrs. Mold flash, protusions or gate burrs shall not exceed 0.15mm per side.

OUTLINE AND MECHANICAL DATA



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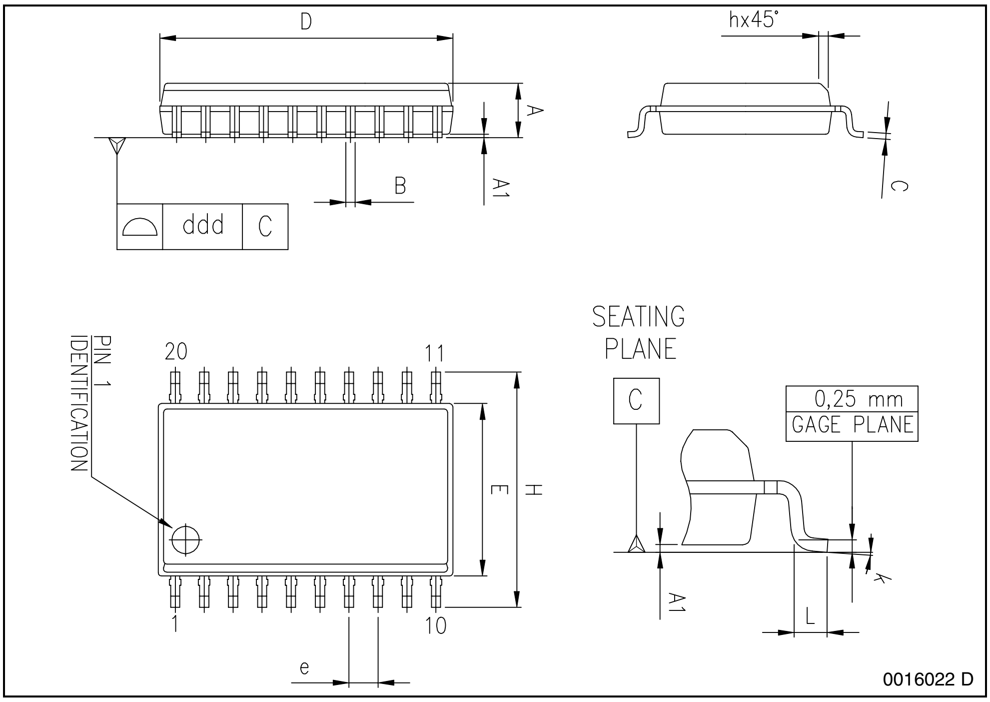

7 Revision history

Date	Revision	Changes
22 April 2004	7	Initial release in EDOCS.
26 July 2005	8	Updated the Layout look & feel. Modify value R_{ON} in Features