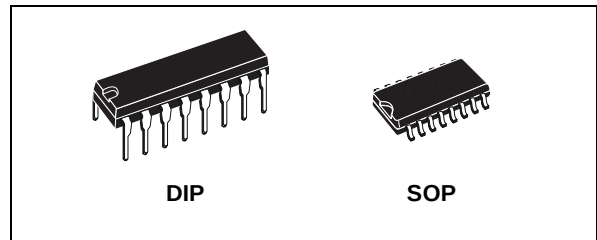


DECADE COUNTER WITH 10 DECODED OUTPUTS

- MEDIUM SPEED OPERATION :
10 MHz (Typ.) at $V_{DD} = 10V$
- FULLY STATIC OPERATION
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED UP TO 20V
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT LEAKAGE CURRENT
 $I_l = 100nA$ (MAX) AT $V_{DD} = 18V$ $T_A = 25^\circ C$
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B " STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"



ORDER CODES

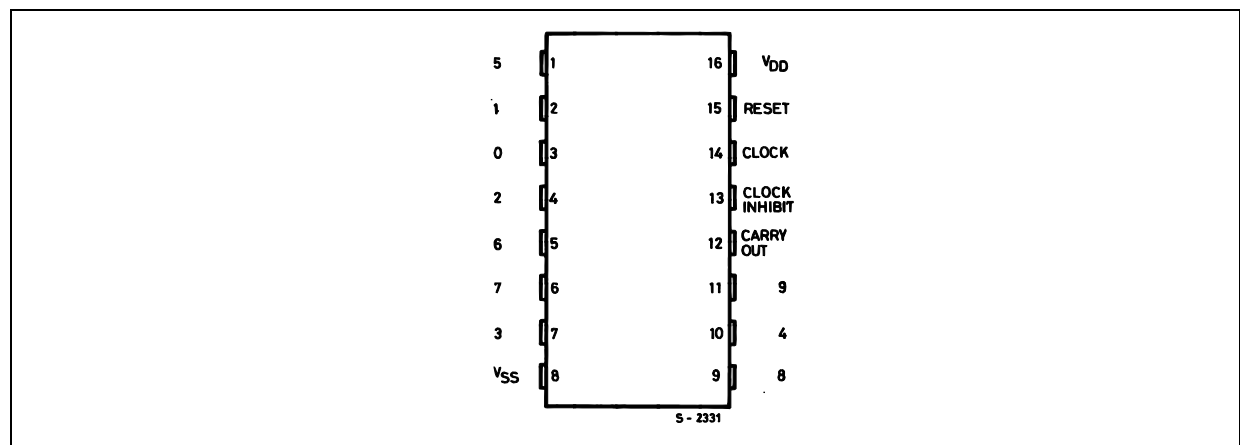
PACKAGE	TUBE	T & R
DIP	HCF4017BEY	
SOP	HCF4017BM1	HCF4017M013TR

DESCRIPTION

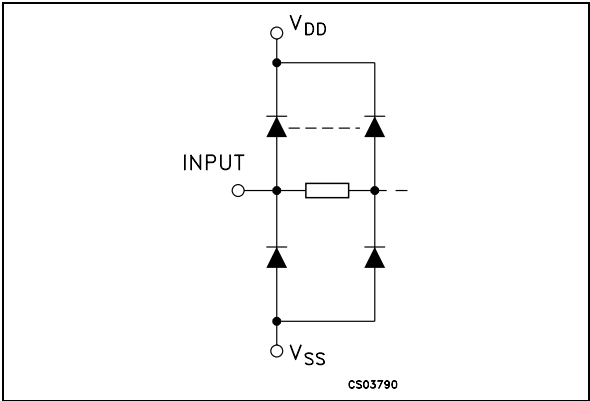
The HCF4017B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in DIP and SOP packages. The HCF4017B is 5-stage Johnson counter having 10 decoded outputs. Inputs include a CLOCK, a RESET, and a CLOCK INHIBIT signal. Schmitt trigger action in the clock input circuit provides pulse shaping that allows unlimited clock input pulse rise and fall times. This counter is advanced one count at the positive clock signal transition if the CLOCK INHIBIT signal is low. Counter advanced via the clock line is inhibited

when the CLOCK INHIBIT signal is high. A high RESET signal clears the counter to its zero count. Use of the Johnson decade-counter configuration permits high speed operation, 2-input decimal decode gating and spike-free decoded outputs. Anti-lock gating is provided, thus assuring proper counting sequence. The decoded outputs are normally low and go high only at their respective decoded time slot. Each decoded output remains high for one full clock cycle. A CARRY - OUT signal completes one cycle every 10 clock input cycles and is used to ripple-clock the succeeding device in a multi-device counting chain.

PIN CONNECTION



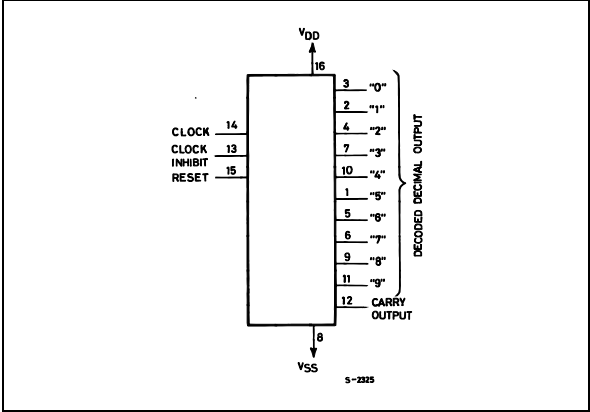
INPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
3, 2, 4, 7, 10, 1, 5, 6, 9, 11	0 to 9	Decoded Decimal Output
14	CLOCK	Clock Input
13	CLOCK INHIBIT	Clock Inhibit Input
15	RESET	Reset Input
12	CARRY OUT	Carry Output
8	V _{SS}	Negative Supply Voltage
16	V _{DD}	Positive Supply Voltage

FUNCTIONAL DIAGRAM

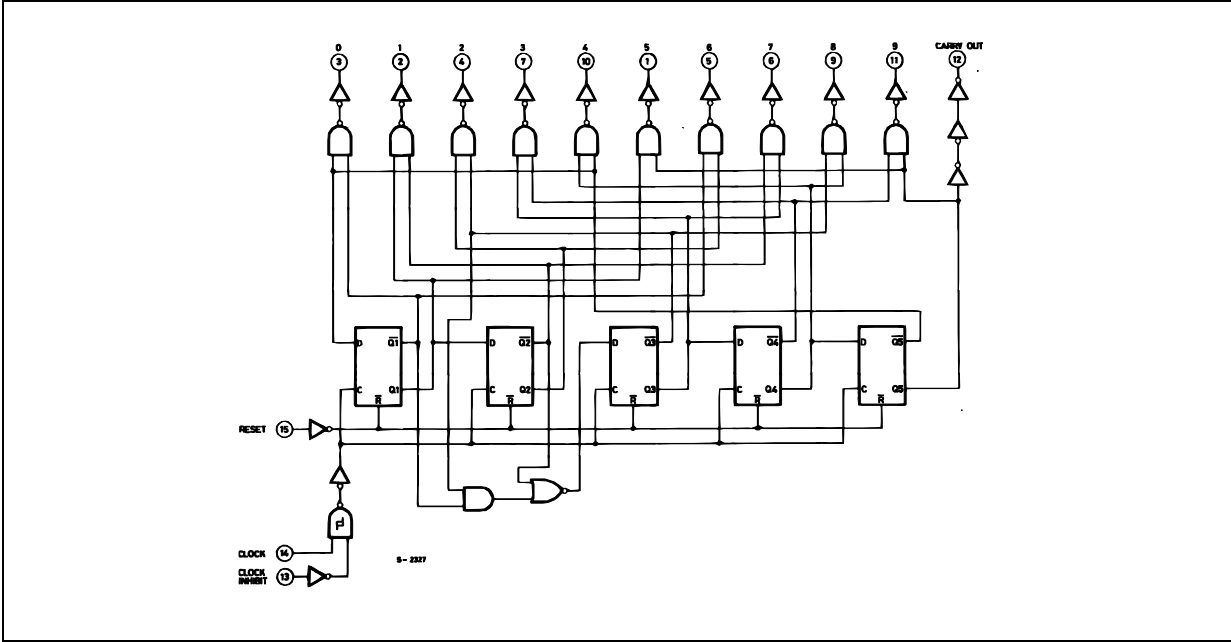


TRUTH TABLE

CLOCK	CLOCK INHIBIT	RESET	DECODED OUTPUT
X	X	H	Q ₀
L	X	L	Q _n
X	H	L	Q _n
	L	L	Q _{n+1}
	L	L	Q _n
H		L	Q _n
H		L	Q _{n+1}

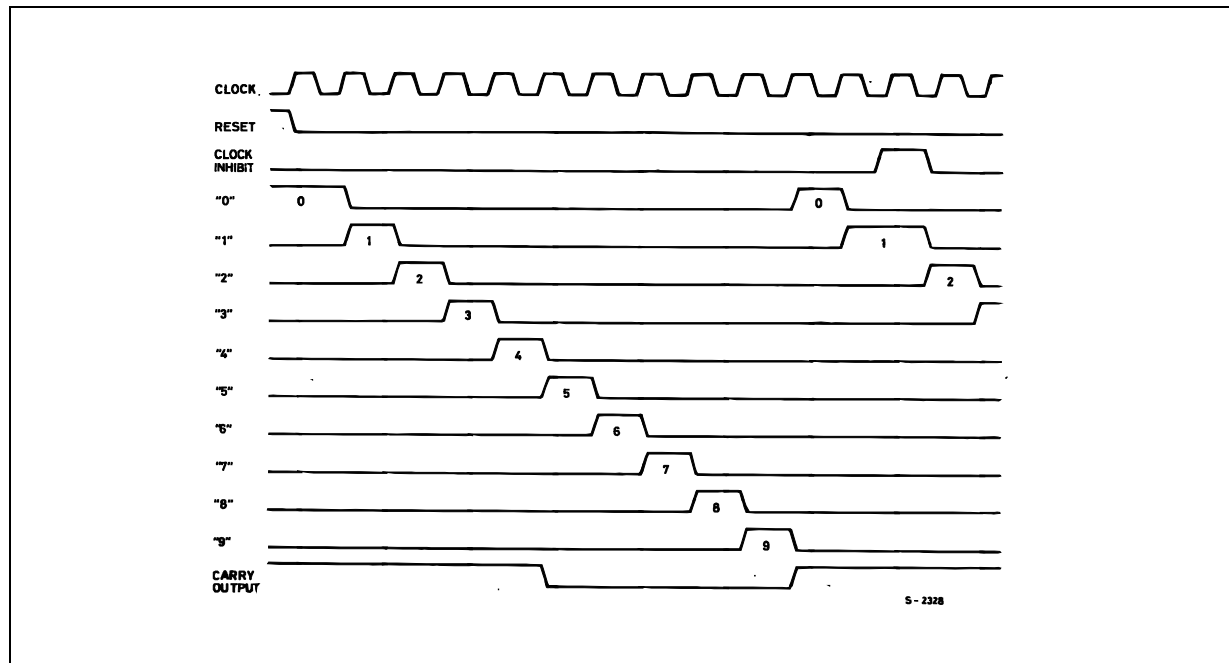
X : Don't Care
Q_n : No Change

LOGIC DIAGRAM



This logic diagram has not be used to estimate propagation delays

TIMING CHART



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.5 to +22	V
V_I	DC Input Voltage	-0.5 to $V_{DD} + 0.5$	V
I_I	DC Input Current	± 10	mA
P_D	Power Dissipation per Package	200	mW
	Power Dissipation per Output Transistor	100	mW
T_{op}	Operating Temperature	-55 to +125	°C
T_{stg}	Storage Temperature	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

All voltage values are referred to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	3 to 20	V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature	-55 to 125	°C

DC SPECIFICATIONS

Symbol	Parameter	Test Condition				Value							Unit
		V _I (V)	V _O (V)	I _{OL} (μA)	V _{DD} (V)	T _A = 25°C			-40 to 85°C		-55 to 125°C		
						Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
I _L	Quiescent Current	0/5			5		0.04	5		150		150	μA
		0/10			10		0.04	10		300		300	
		0/15			15		0.04	20		600		600	
		0/20			20		0.08	100		3000		3000	
V _{OH}	High Level Output Voltage	0/5		<1	5	4.95			4.95		4.95		V
		0/10		<1	10	9.95			9.95		9.95		
		0/15		<1	15	14.95			14.95		14.95		
V _{OL}	Low Level Output Voltage	5/0		<1	5		0.05			0.05		0.05	V
		10/0		<1	10		0.05			0.05		0.05	
		15/0		<1	15		0.05			0.05		0.05	
V _{IH}	High Level Input Voltage		0.5/4.5	<1	5	3.5			3.5		3.5		V
			1/9	<1	10	7			7		7		
			1.5/13.5	<1	15	11			11		11		
V _{IL}	Low Level Input Voltage		4.5/0.5	<1	5			1.5		1.5		1.5	V
			9/1	<1	10			3		3		3	
			13.5/1.5	<1	15			4		4		4	
I _{OH}	Output Drive Current	0/5	2.5	<1	5	-1.36	-3.2		-1.1		-1.1		mA
		0/5	4.6	<1	5	-0.44	-1		-0.36		-0.36		
		0/10	9.5	<1	10	-1.1	-2.6		-0.9		-0.9		
		0/15	13.5	<1	15	-3.0	-6.8		-2.4		-2.4		
I _{OL}	Output Sink Current	0/5	0.4	<1	5	0.44	1		0.36		0.36		mA
		0/10	0.5	<1	10	1.1	2.6		0.9		0.9		
		0/15	1.5	<1	15	3.0	6.8		2.4		2.4		
I _I	Input Leakage Current	0/18	Any Input		18		±10 ⁻⁵	±0.1		±1		±1	μA
C _I	Input Capacitance		Any Input				5	7.5					pF

The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}=5V, 2V min. with V_{DD}=10V, 2.5V min. with V_{DD}=15V

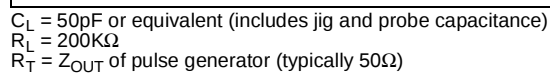
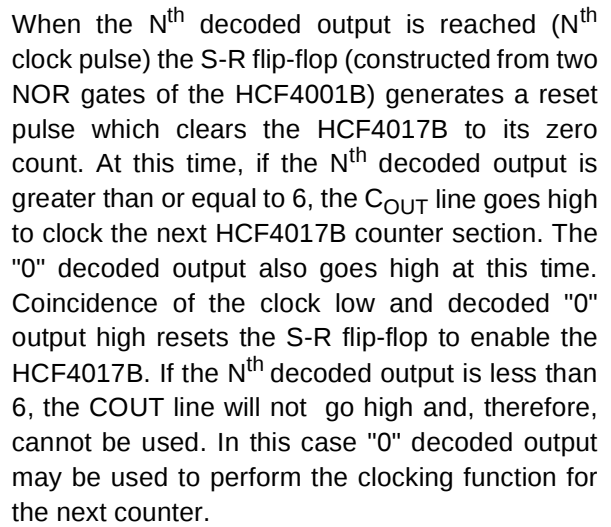
DYNAMIC ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}\text{C}$, $C_L = 50\text{pF}$, $R_L = 200\text{K}\Omega$, $t_r = t_f = 20\text{ ns}$)

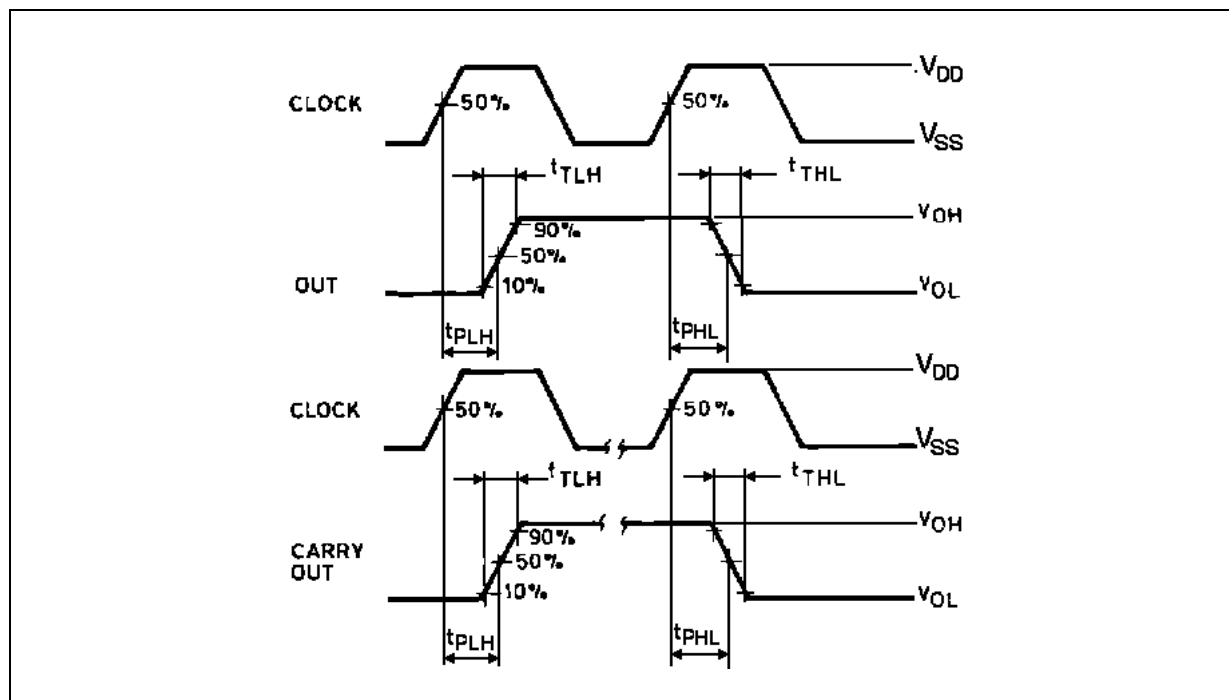
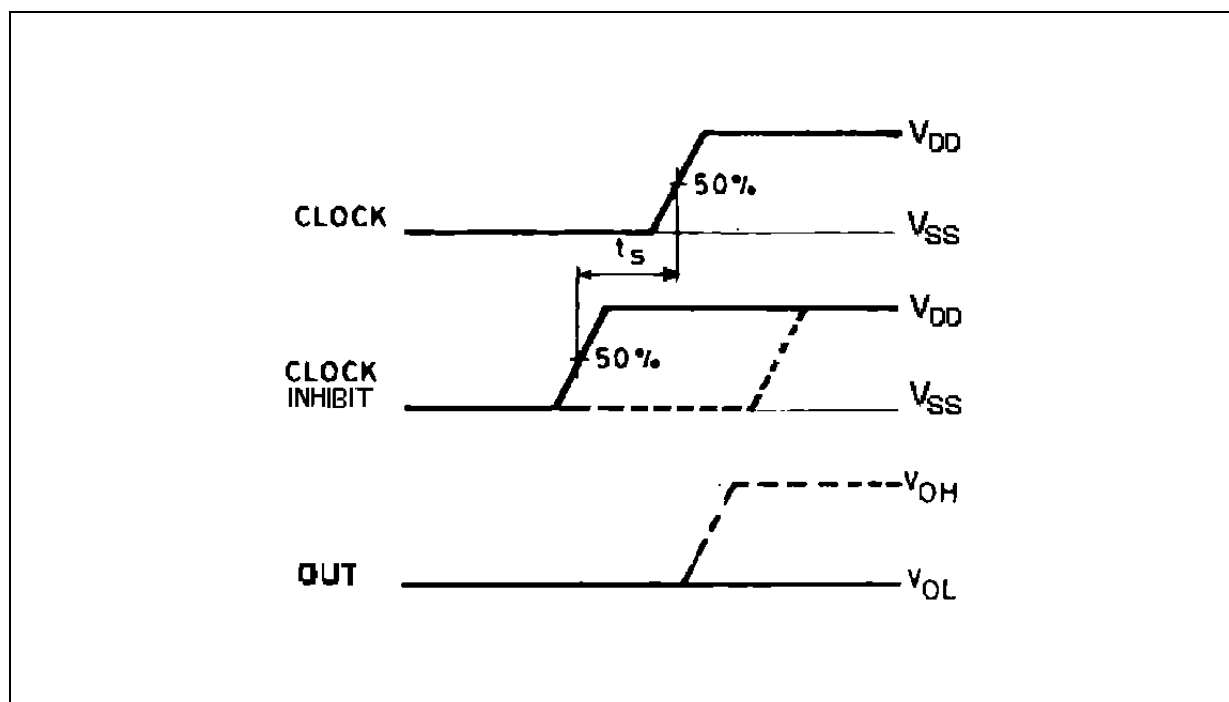
Symbol	Parameter	Test Condition		Value (*)			Unit
		V _{DD} (V)		Min.	Typ.	Max.	
CLOCKED OPERATION							
t _{PLH} t _{PHL}	Propagation Delay Time (decode out)	5			325	650	ns
		10			135	270	
		15			85	170	
	Propagation Delay Time (carry out)	5			300	600	ns
		10			125	250	
		15			80	160	
t _{THL} t _{TLH}	Transition Time (carry out or decoded out lines)	5			100	200	ns
		10			50	100	
		15			40	80	
f _{CL} ⁽¹⁾	Maximum Clock Input Frequency	5		2.5	5	5	MHz
		10		5	10		
		15		5.5	11		
t _W	Minimum Clock Pulse Width	5			100	200	ns
		10			45	90	
		15			30	60	
t _r , t _f	Clock Input Rise or Fall Time	5		unlimited			μs
		10					
		15					
t _{setup}	Data Setup Time Minimum Clock Inhibit	5			115	230	ns
		10			50	100	
		15			35	75	
RESET OPERATION							
t _{PLH} , t _{PHL}	Propagation Delay Time (carry out or decoded out lines)	5			265	530	ns
		10			115	230	
		15			85	170	
t _W	Minimum Reset Pulse Width	5			130	260	ns
		10			55	110	
		15			30	60	
t _{REM}	Minimum Reset Removal Time	5			200	400	ns
		10			140	280	
		15			75	150	

(*) Typical temperature coefficient for all V_{DD} value is 0.3 %/°C.

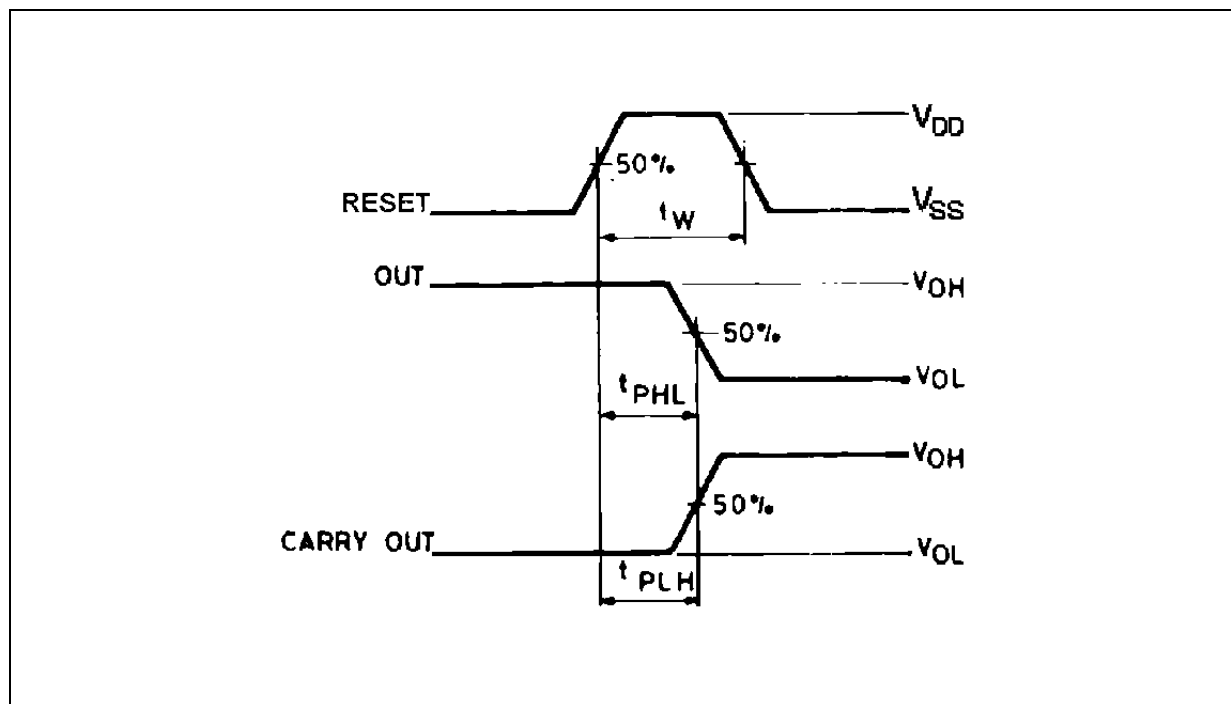
(1) Measured with respect to carry out line.

DIVIDE BY N COUNTER($N \leq 10$) WITH DECODED OUTPUTS

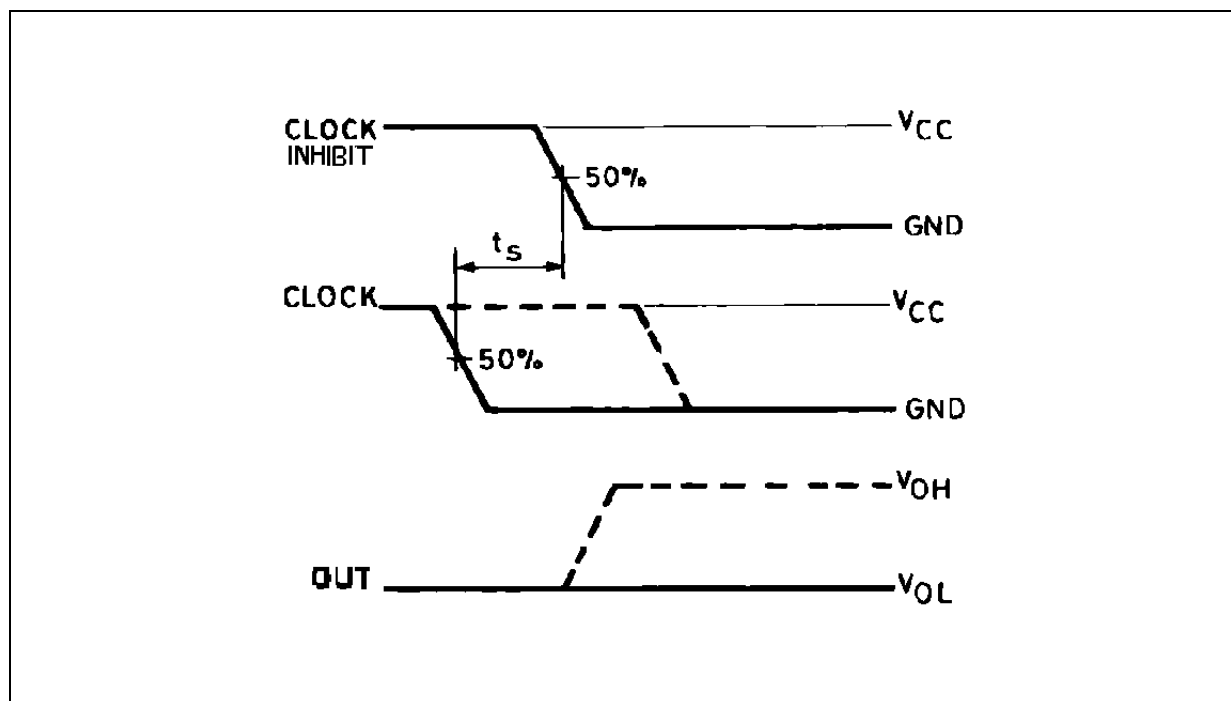


WAVEFORM 1 : PROPAGATION DELAY TIMES ($f=1\text{MHz}$; 50% duty cycle)**WAVEFORM 2 : MINIMUM SETUP TIME (CLOCK INHIBIT TO CLOCK)** ($f=1\text{MHz}$; 50% duty cycle)

WAVEFORM 3 : PROPAGATION DELAY TIMES, MINIMUM RESET PULSE WIDTH ($f=1\text{MHz}$; 50% duty cycle)



WAVEFORM 4 : MINIMUM SETUP TIME (CLOCK TO CLOCK INHIBIT) ($f=1\text{MHz}$; 50% duty cycle)



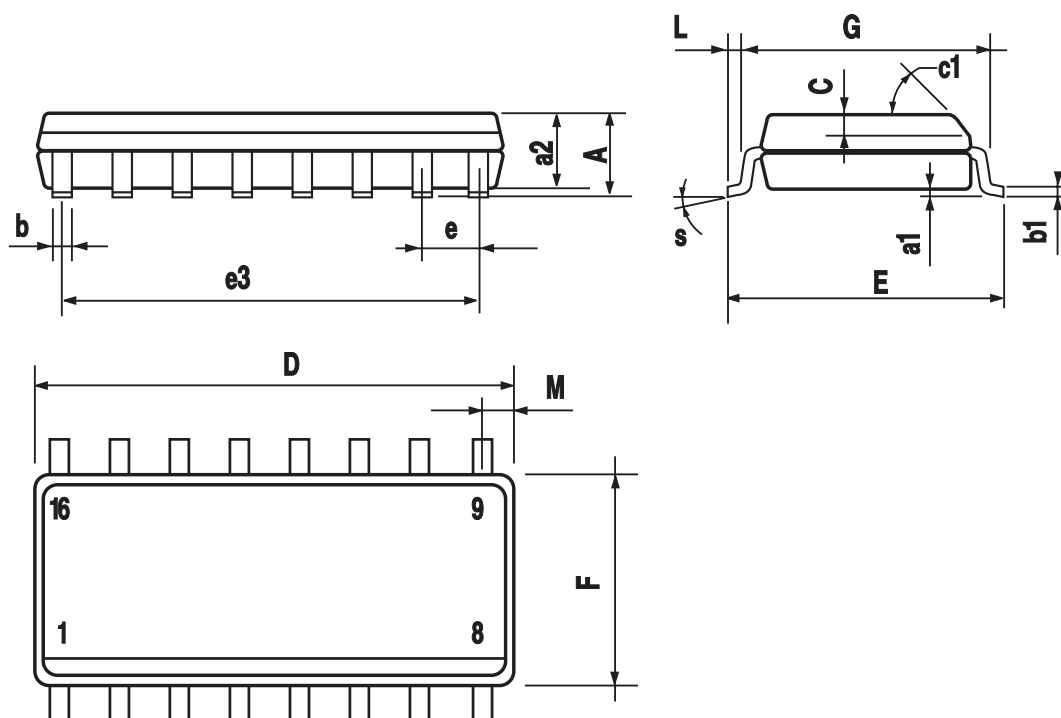
Plastic DIP-16 (0.25) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



SO-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



PO13H

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2001 STMicroelectronics - Printed in Italy - All Rights Reserved
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco
Singapore - Spain - Sweden - Switzerland - United Kingdom

© <http://www.st.com>

