

5V, 500mA low drop voltage regulator

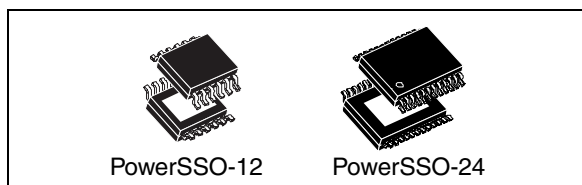
Features

Max DC supply voltage	V_S	40V
Max output voltage tolerance	ΔV_O	+/-2%
Max dropout voltage	V_{dp}	500mV
Output current	I_O	500mA
Quiescent current	I_{qn}	3 μ A ⁽¹⁾

1. Typical value with regulator disabled

- Operating DC supply voltage range 5.6V to 31V
- Low dropout voltage
- Low quiescent current consumption
- Reset circuit sensing of output voltage down to 1V
- Programmable reset pulse delay with external capacitor
- Programmable watchdog^(a) timer with external capacitor
- Thermal shutdown and short circuit protection
- Wide temperature range ($T_j = -40^{\circ}\text{C}$ to 150°C)
- Enable^(a) input for enabling/disabling the voltage regulator

a. Watchdog and Enable facilities are available according to Device summary table.



Description

L4995 is a family of monolithic integrated 5V voltage regulators with a low drop voltage at currents of up to 500mA, available in both 12 and 24 pin packages.

The output voltage regulating element consists of a p-channel MOS and regulation is performed regardless of input voltage transients of up to 40V. The high precision of the output voltage is obtained using a pre-trimmed reference voltage. The L4995 family is protected against short circuit and overtemperature protection switches off the devices in the case of extremely high power dissipation. The L4995 integrates the watchdog, enable and externally programmable reset circuits. The L4995A features the externally programmable reset and enable. Finally the L4995R features the externally programmable reset.

The combination of such features makes this device particularly flexible and suitable to supply microprocessor systems in automotive applications.

Table 1. Device summary

Package	Order codes		
	Tube	Tape and reel	
PowerSSO-12 (exposed pad)	L4995J - L4995AJ - L4995RJ	L4995JTR - L4995AJTR - L4995RJTR	
PowerSSO-24 (exposed pad)	L4995K - L4995AK - L4995RK	L4995KTR - L4995AKTR - L4995RKTR	
P/N	Watchdog	Reset	Enable
L4995J - L4995K	X	X	X
L4995AJ - L4995AK	-	X	X
L4995RJ - L4995RK	-	X	-

Contents

1	Block diagrams and pins descriptions	5
2	Electrical specifications	8
2.1	Absolute maximum ratings	8
2.2	Thermal data	9
2.3	Electrical characteristics	9
2.4	Electrical characteristics curves	12
2.5	Test circuit and waveforms plot	15
2.5.1	Load regulation	15
3	Application information	16
3.1	Voltage regulator	17
3.2	Reset	17
3.3	Watchdog	18
4	Package and PCB thermal data	19
4.1	PowerSSO-12 thermal data	19
4.2	PowerSSO-24 thermal data	22
5	Package and packing information	25
5.1	ECOPACK®	25
5.2	PowerSSO-24 mechanical data	27
5.3	PowerSSO-12 packing information	29
5.4	PowerSSO-24 packing information	30
6	Revision history	31

List of tables

Table 1. Device summary 1

Table 2. Pins descriptions 6

Table 3. Absolute maximum ratings 8

Table 4. Thermal data 9

Table 5. General 9

Table 6. Reset 10

Table 7. Watchdog 11

Table 8. Enable 11

Table 9. PowerSSO-12 thermal parameter 21

Table 10. PowerSSO-24 thermal parameter 24

Table 11. PowerSSO-12 mechanical data 26

Table 12. PowerSSO-24 mechanical data 28

Table 13. Document revision history 31

List of figures

Figure 1.	Block diagram of L4995	5
Figure 2.	Block diagram of L4995A	5
Figure 3.	Block diagram of L4995R	6
Figure 4.	Pins configurations (L4995)	7
Figure 5.	Output voltage vs T_j	12
Figure 6.	Output voltage vs V_S	12
Figure 7.	Drop voltage vs output current	12
Figure 8.	Current consumption vs output current	12
Figure 9.	Current consumption vs input voltage	12
Figure 10.	Current limitation vs T_j	12
Figure 11.	Current limitation vs input voltage	13
Figure 12.	Short circuit current vs input voltage	13
Figure 13.	Output voltage vs enable voltage	13
Figure 14.	V_{En_high} vs T_j	13
Figure 15.	V_{EN_LOW} vs T_j	13
Figure 16.	V_{Rhth} vs T_j	13
Figure 17.	V_{Rlth} vs T_j	14
Figure 18.	V_{whth} vs T_j	14
Figure 19.	V_{wlth} vs T_j	14
Figure 20.	I_{cr} and I_{cwc} vs T_j	14
Figure 21.	I_{dr} and I_{cwd} vs T_j	14
Figure 22.	T_{wop} vs T_j	14
Figure 23.	PSRR	15
Figure 24.	Load regulation test circuit	15
Figure 25.	Maximum load variation response	15
Figure 26.	L4995 application schematic ⁽¹⁾	16
Figure 27.	Stability region ⁽¹⁾	16
Figure 28.	Behavior of output current versus regulated voltage V_O	17
Figure 29.	Reset timing diagram	18
Figure 30.	Watchdog timing diagram	18
Figure 31.	PowerSSO-12 PC board ⁽¹⁾	19
Figure 32.	$R_{thj-amb}$ vs PCB copper area in open box free air condition	19
Figure 33.	PowerSSO-12 thermal impedance junction ambient single pulse	20
Figure 34.	Thermal fitting model of V_{reg} in PowerSSO-12	20
Figure 35.	PowerSSO-24 PC board ⁽¹⁾	22
Figure 36.	$R_{thj-amb}$ vs PCB copper area in open box free air condition	22
Figure 37.	PowerSSO-24 thermal impedance junction ambient single pulse	23
Figure 38.	Thermal fitting model of V_{reg} in in PowerSSO-24	23
Figure 39.	PowerSSO-12 package dimensions	25
Figure 40.	PowerSSO-24 package dimensions	27
Figure 41.	PowerSSO-12 tube shipment (no suffix)	29
Figure 42.	PowerSSO-12 tape and reel shipment (suffix "TR")	29
Figure 43.	PowerSSO-24 tube shipment (no suffix)	30
Figure 44.	PowerSSO-24 tape and reel shipment (suffix "TR")	30

1 Block diagrams and pins descriptions

Figure 1. Block diagram of L4995

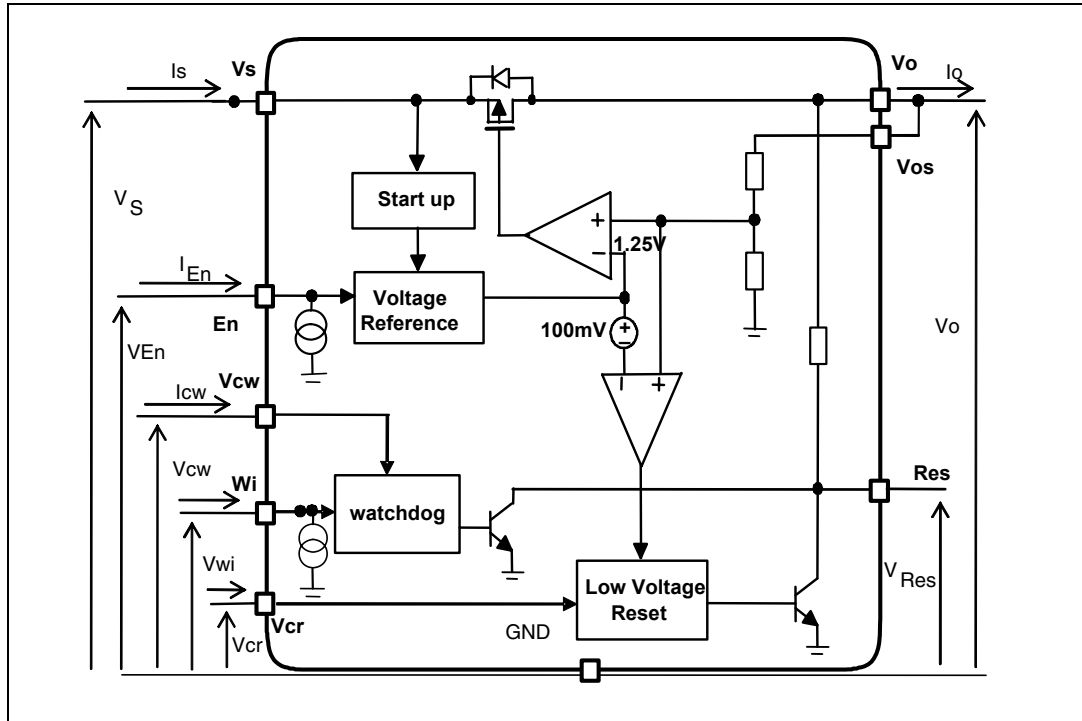


Figure 2. Block diagram of L4995A

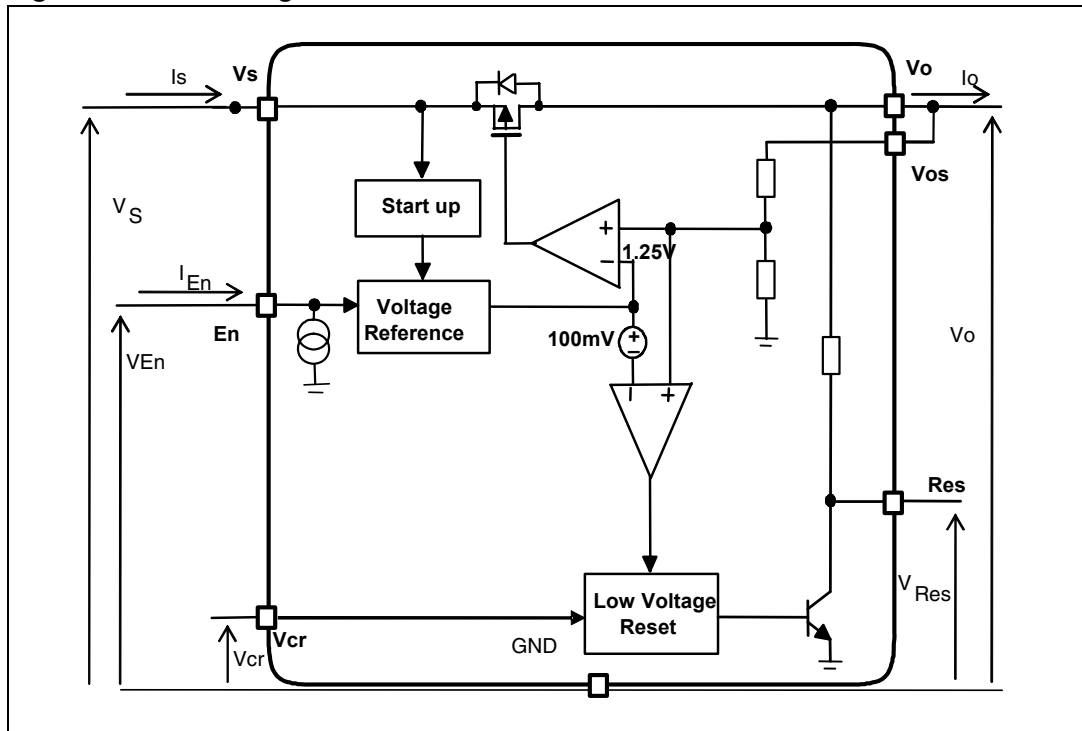


Figure 3. Block diagram of L4995R

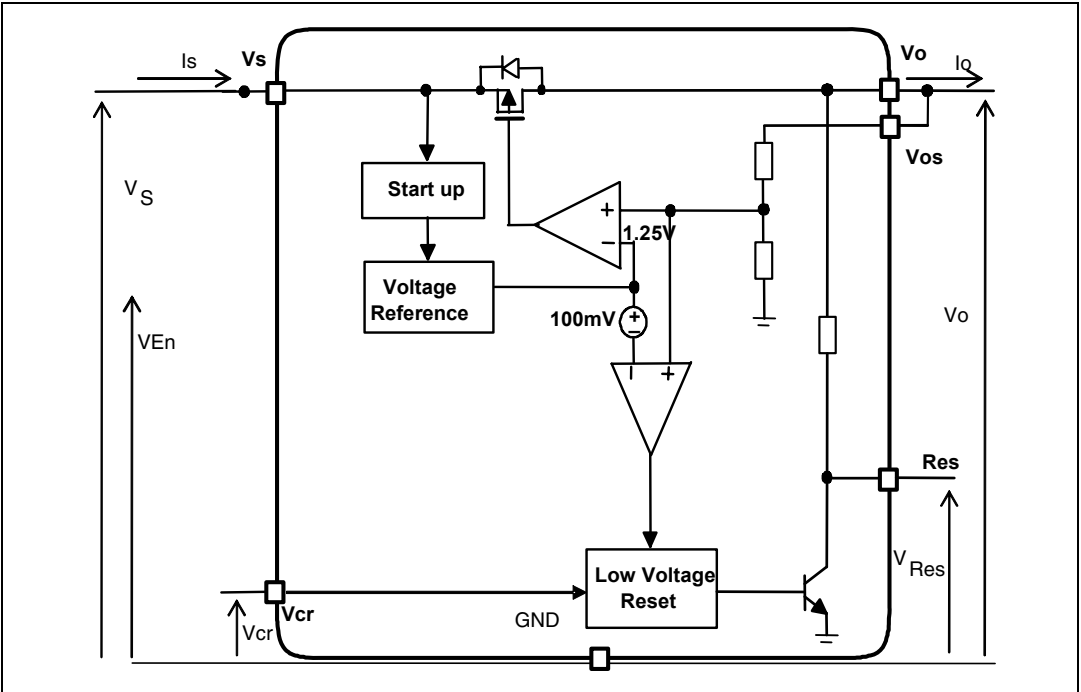


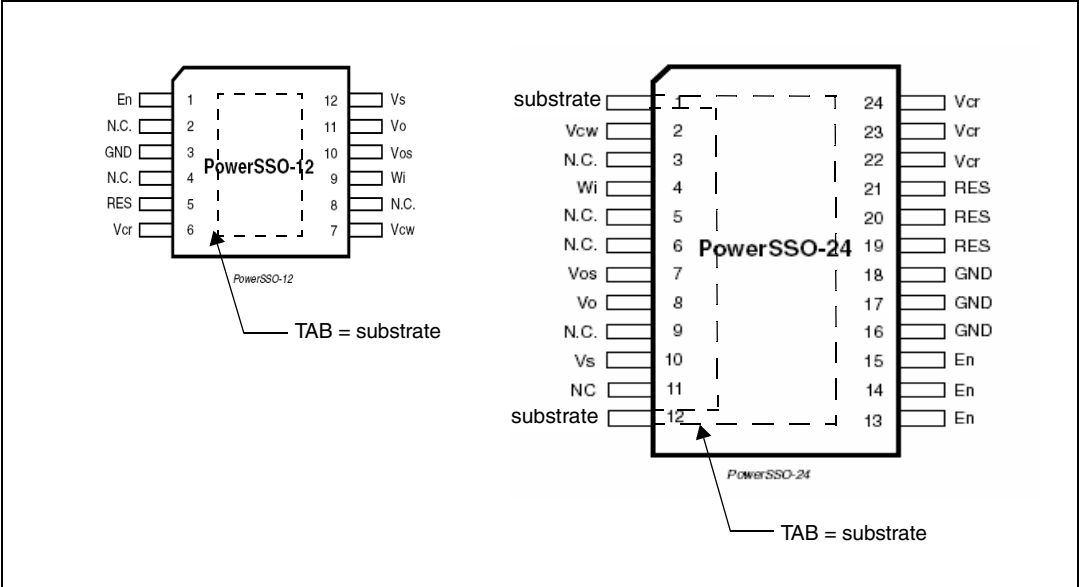
Table 2. Pins descriptions

Pin name	PowerSSO-12 pin #	PowerSSO-24 pin #	Function
E_n	1	13, 14, 15	Enable input (L4995 and L4996A only, otherwise not connected). If high regulator, watchdog and reset are operating. If low regulator, watchdog and reset are shutdown. Connect to V_s if not used.
NC	2, 4, 8	3, 5, 6, 9, 11	Not connected.
GND	3	16, 17, 18	Ground reference.
-	TAB	TAB, 1, 12	Substrate of the chip: connect the pins or the TAB to GND.
R_{es}	5	19, 20, 21	Reset output. It is pulled down when output voltage goes below V_{o_th} or frequency at W_i is too low. Leave floating if not used.
V_{cr}	6	22, 23, 24	Reset timing adjust. A capacitor between V_{cr} pin and GND. Sets the reset delay time (trd). Leave floating if Reset is not used.
V_{cw}	7	2	Watchdog timer adjust (L4995 only, otherwise not connected). A capacitor between V_{cw} pin and GND. Sets the time response of the watchdog monitor.
W_i	9	4	Watchdog input (L4995 only, otherwise not connected). If the frequency at this input pin is too low, the Reset output is activated.

Table 2. Pins descriptions (continued)

Pin name	PowerSSO-12 pin #	PowerSSO-24 pin #	Function
V_{OS}	10	7	Regulator voltage output sensing.
V_O	11	8	5 voltage regulator output. Block to ground with a capacitor >100nF (needed for regulator stability).
V_S	12	10	Supply voltage. Block to ground directly at V_S pin with a ceramic capacitor (e.g. 200nF).

Figure 4. Pins configurations (L4995)



2 Electrical specifications

2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{VsdC}	DC supply voltage	- 0.3 to 40	V
I_{VsdC}	Input current	Internally limited	
V_{Vo}	DC output voltage	- 0.3 to 6	V
I_{Vo}	DC output current	Internally limited	
V_{Wi}	Watchdog input voltage	-0.3 to $V_{Vo} + 0.3$	V
V_{od}	R_{es} output voltage	-0.3 to $V_{Vo} + 0.3$	V
I_{od}	R_{es} output current	Internally limited	
V_{cr}	V_{cr} voltage	- 0.3 to $V_{Vo} + 0.3$	V
V_{cw}	Watchdog delay voltage	- 0.3 to $V_{Vo} + 0.3$	V
V_{En}	Enable input	- 0.3 to $V_{VsdC} + 0.3$	V
T_j	Junction temperature	- 40 to 150	°C
V_{ESD}	ESD voltage level (HBM-MIL STD 883C)	± 2	kV
V_{ESD}	ESD voltage level (CDM AEC-Q100-011)	750	V

2.2 Thermal data

For details, please refer to [Section 4.1: PowerSSO-12 thermal data](#) and [Section 4.2: PowerSSO-24 thermal data](#).

Table 4. Thermal data⁽¹⁾

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance Junction to Case: PowerSSO-12	5	°K/W
	PowerSSO-24	4	°K/W
$R_{thj-amb}$	Thermal resistance Junction to Ambient: PowerSSO-12	52	°K/W
	PowerSSO-24	38	°K/W

1. The values quoted are for PCB 77mm x 86mm x 1.6mm, FR4, double layer; Copper thickness 0.070mm
Copper area 3cm² Thermal Vias, Thermal vias separation 1.2 mm, Thermal via diameter 0.3 mm +/- 0.08 mm, Cu thickness on vias 0.025 mm.

2.3 Electrical characteristics

Values specified in this section are for $V_S = 5.6V$ to $31V$, $T_j = -40\text{ °C}$ to $+150\text{ °C}$ unless otherwise stated.

Table 5. General

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_O	V_{O_ref}	Output voltage	$V_S = 5.6$ to $31V$ $I_O = 0$ to $500mA$	4.9	5.00	5.1	V
V_O	I_{short}	Short circuit current	$V_S = 13.5V$ ⁽¹⁾	550	800	1050	mA
V_O	I_{lim} ⁽²⁾	Output current limitation	$V_S = 13.5V$ ⁽¹⁾	600	900	1250	mA
V_S, V_O	V_{line}	Line regulation voltage	$V_S = 5.6$ to $31V$ $I_O = 0$ to $500mA$			25	mV
V_O	V_{load}	Load regulation voltage	$I_O = 0$ to $500mA$			25	mV
V_S, V_O	V_{dp} ⁽³⁾	Drop voltage	$I_O = 400mA$		270	500	mV
V_S, V_O	SVR	Ripple rejection	$f_r = 100\text{ Hz}$ ⁽⁴⁾	55			dB
V_S, V_O	I_{qs}	Current consumption with regulator disabled	$V_S = 13.5V$, $E_n = low$		3	10	μA
V_S, V_O	I_{qn_1}	Current consumption with regulator enabled	$V_S = 13.5V$, $I_O < 1mA$,		90	160	μA
V_S, V_O	I_{qn_50}	Current consumption with regulator enabled	$V_S = 13.5V$, $I_O = 50mA$,		290	400	μA

Table 5. General (continued)

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_S, V_O	I_{qn_150}	Current consumption with regulator enabled	$V_S = 13.5V$, $I_O = 150mA$,		740	1000	μA
V_S, V_O	I_{qn_250}	Current consumption with regulator enabled	$V_S = 13.5V$, $I_O = 250mA$,		1	1.4	mA
V_S, V_O	I_{qn_500}	Current consumption with regulator enabled	$V_S = 13.5V$, $I_O = 500mA$,		2.1	2.7	mA
	T_w	Thermal protection temperature		150		190	$^{\circ}C$
	T_{w_hy}	Thermal protection temperature hysteresis			10		$^{\circ}C$

1. See [Figure 28](#).
2. Measured output current when the output voltage has dropped 100mV from its nominal value obtained at $V_S=13.5V$ and $I_O=250mA$.
3. V_S-V_O measured when the output voltage has dropped 100mV from its nominal value obtained at $V_S=13.5V$ and $I_O=250mA$.
4. Guaranteed by design.

Table 6. Reset

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
R_{es}	V_{res_l}	Reset output low voltage	$R_{ext} = 5k\Omega$ to V_O , $V_O > 1V$			0.4	V
R_{es}	I_{Res_lkg}	Reset output high leakage current	$V_{Res} = 5V$			1	μA
R_{es}	R_{Res}	Pull up internal resistance (versus V_O)		10	20	40	$k\Omega$
R_{es}	V_{O_th}	V_O out of regulation threshold	$V_S = 5.6$ to $31V$ $I_O = 1$ to $500mA$	6%	8%	10%	below V_{O_ref}
V_{cr}	V_{Rlth}	Reset delay circuit low threshold	$V_S = 13.5V$	10%	13%	16%	V_{O_ref}
V_{cr}	V_{Rhth}	Reset delay circuit high threshold	$V_S = 13.5V$	44%	47%	50%	V_{O_ref}
V_{cr}	I_{cr}	Charge current	$V_S = 13.5V$	8	15	30	μA
V_{cr}	I_{dr}	Discharge current	$V_S = 13.5V$	8	15	30	μA
R_{es}	T_{rr}	Reset reaction time ⁽¹⁾	$V_O = V_{O_th} - 100mV$	100	250	700	μs
R_{es}	T_{rd}	Reset delay time	$V_S = 13.5V$, $C_{tr} = 47nF$	13	39	70	ms

1. When V_O becomes lower than 4V, the reset reaction time decreases down to 2 μs assuring a faster reset condition in this particular case.

Table 7. Watchdog

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
W _i	V _{ih}	Input high voltage	V _S = 13.5V	3.5			V
W _i	V _{il}	Input low voltage	V _S = 13.5V			1.5	V
W _i	V _{ih}	Input hysteresis	V _S = 13.5V		500		mV
W _i	I _{wi}	Pull down current	V _S = 13.5V V _{wi} = 3.5V		6	10	μA
V _{cw}	V _{wlth}	Low threshold	V _S = 13.5V	10%	13%	16%	V _{o_ref}
V _{cw}	V _{whth}	High threshold	V _S = 13.5V	44%	47%	50%	V _{o_ref}
V _{cw}	I _{cwc}	Charge current	V _S = 13.5V, V _{cw} = 0.1V	5	10	20	μA
V _{cw}	I _{cwd}	Discharge current	V _S = 13.5V, V _{cw} = 2.5V	1.25	2.5	5	μA
V _{cw}	T _{wop}	Watchdog period	V _S = 13.5V, C _{tw} = 47nF	20	40	80	ms
R _{es}	t _{wol}	Watchdog output low time	V _S = 13.5V, C _{tw} = 47nF	4	8	16	ms

Table 8. Enable

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
E _n	V _{En_low}	E _n input low voltage				1	V
E _n	V _{En_high}	E _n input high voltage		3			V
E _n	V _{En_hyst}	E _n input hysteresis			830		mV
E _n	I _{En}	Pull down current	V _S = 13.5V		10	18	μA

2.4 Electrical characteristics curves

Figure 5. Output voltage vs T_j

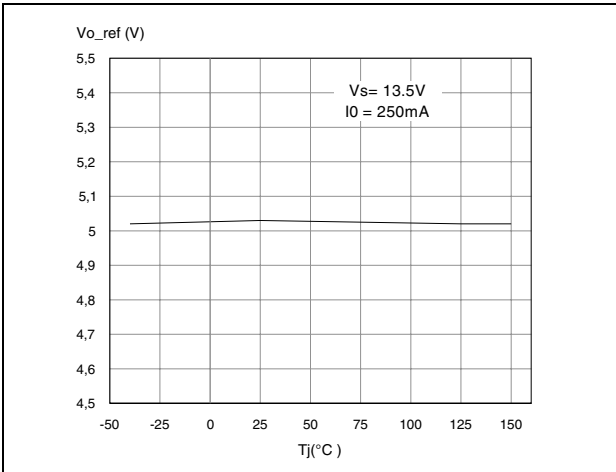


Figure 6. Output voltage vs V_s

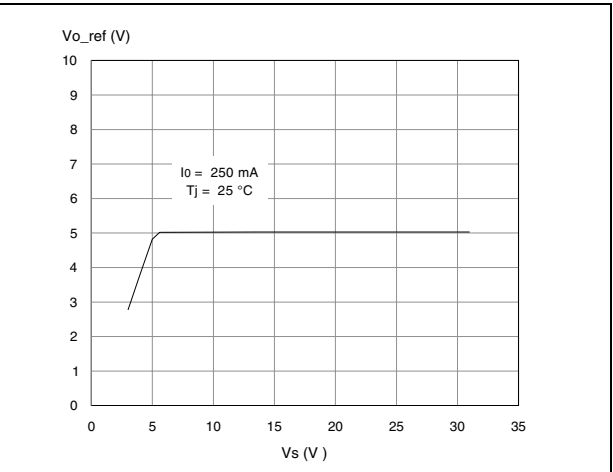


Figure 7. Drop voltage vs output current

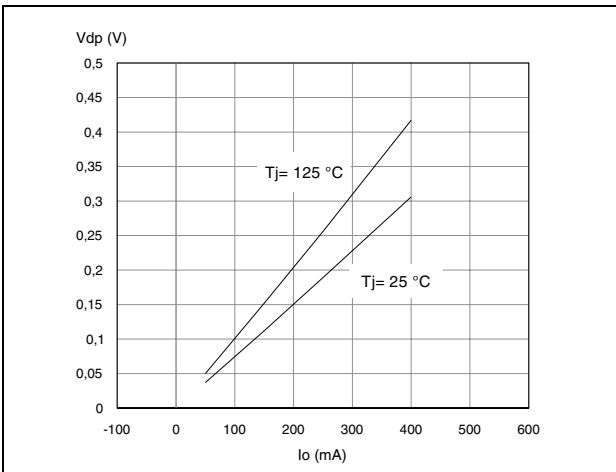


Figure 8. Current consumption vs output current

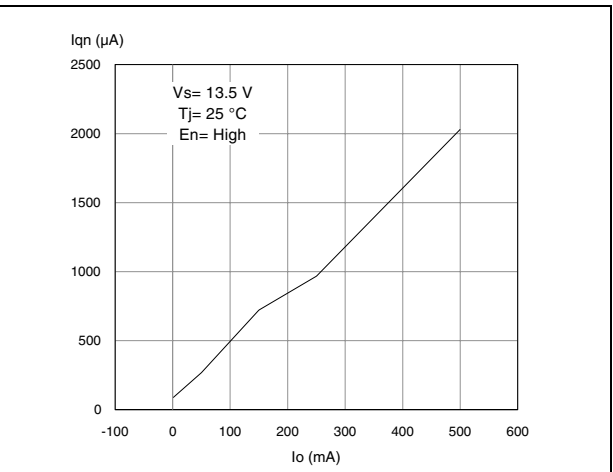


Figure 9. Current consumption vs input voltage

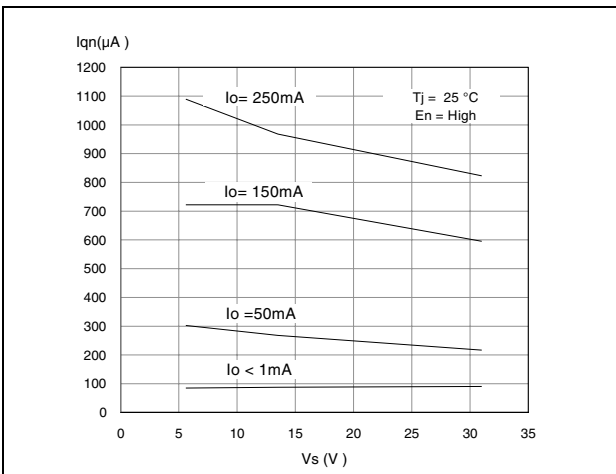


Figure 10. Current limitation vs T_j

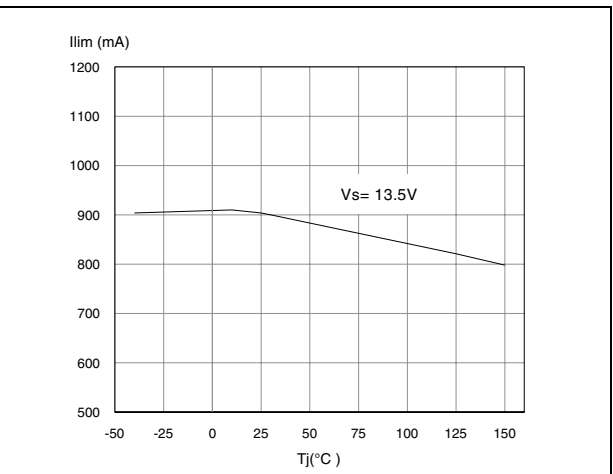


Figure 11. Current limitation vs input voltage

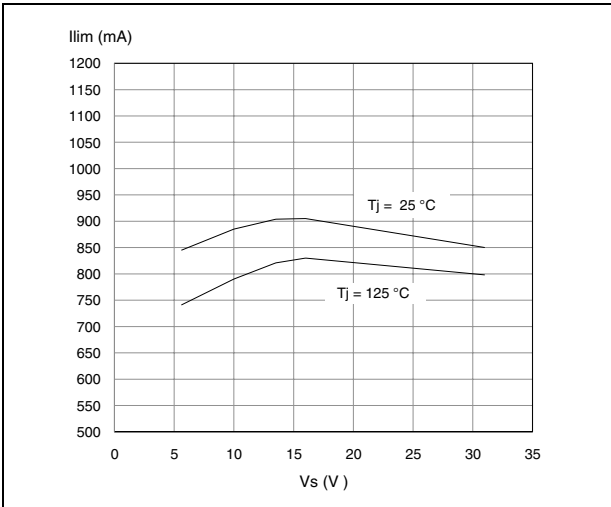


Figure 12. Short circuit current vs input voltage

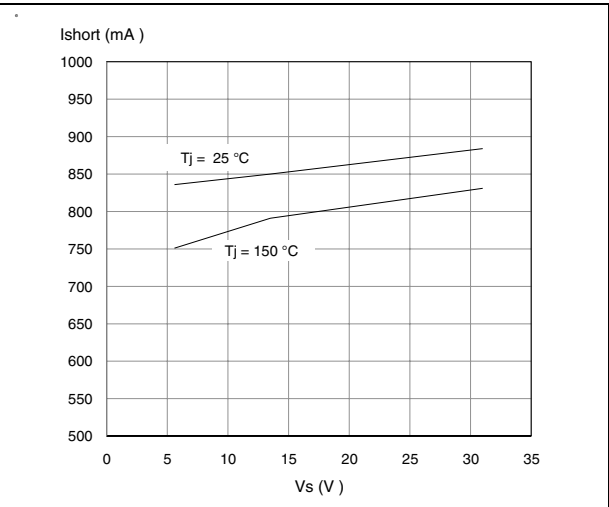


Figure 13. Output voltage vs enable voltage

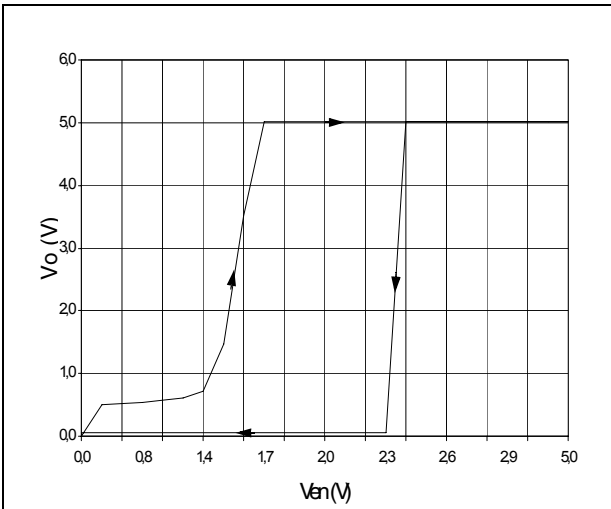


Figure 14. VEn_high vs Tj

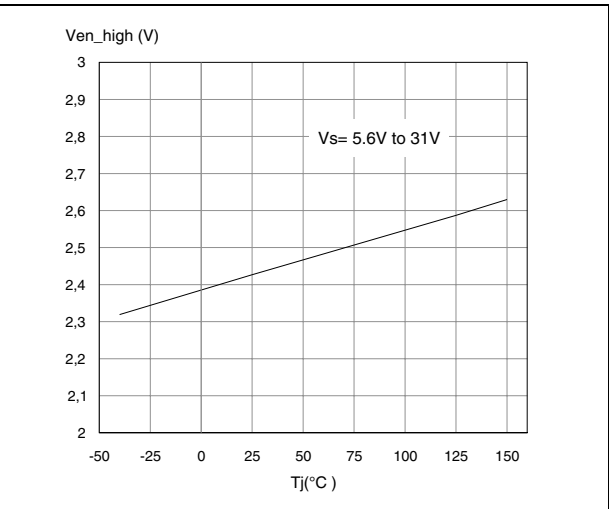


Figure 15. VEN_LOW vs Tj

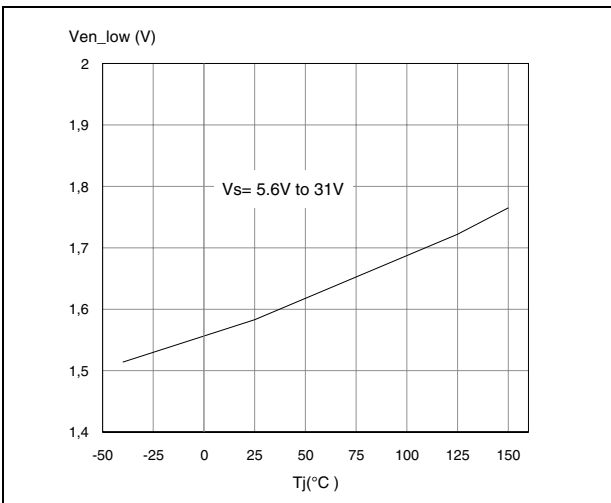


Figure 16. VRhth vs Tj

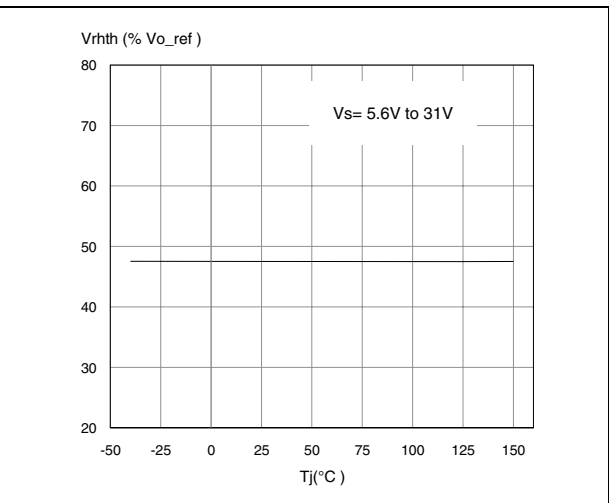


Figure 17. V_{Rlth} vs T_j

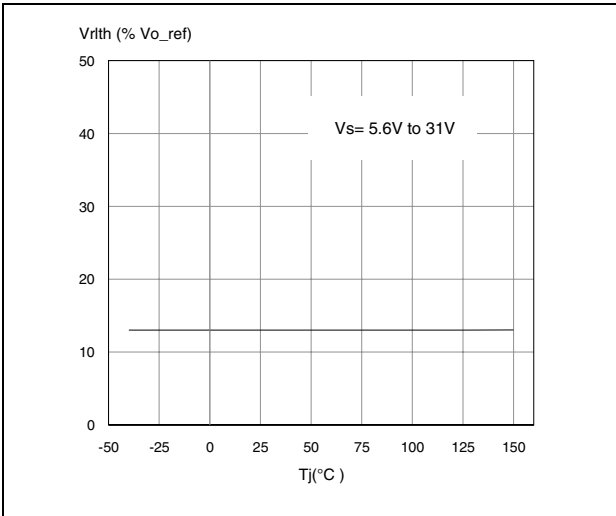


Figure 18. V_{whth} vs T_j

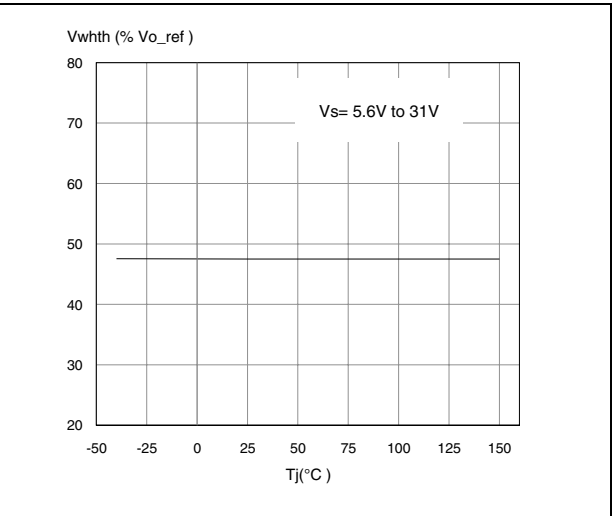


Figure 19. V_{wlth} vs T_j

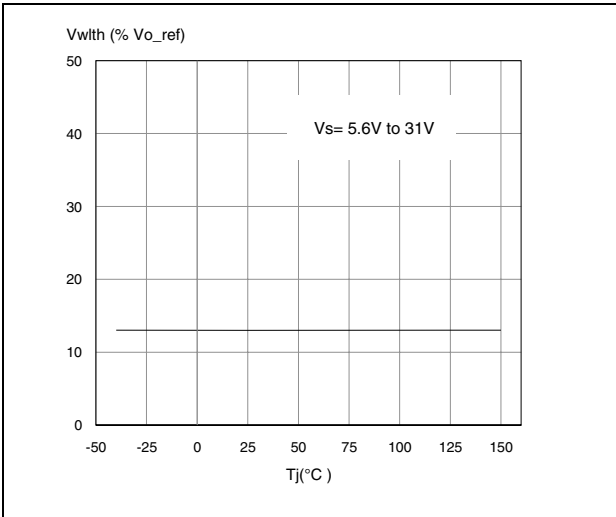


Figure 20. I_{cr} and I_{cwc} vs T_j

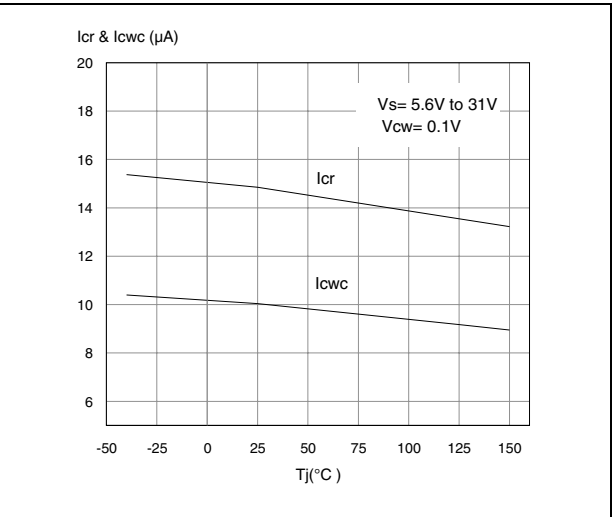


Figure 21. I_{dr} and I_{cwd} vs T_j

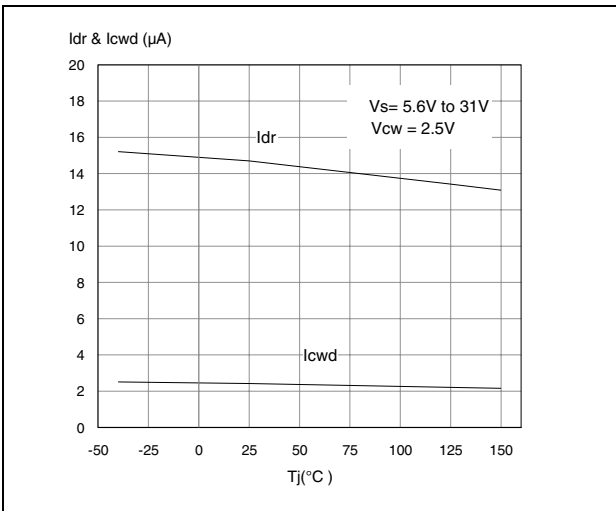


Figure 22. T_{wop} vs T_j

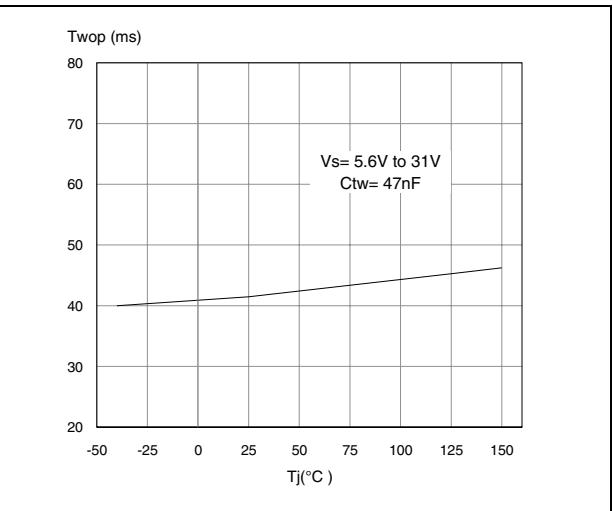
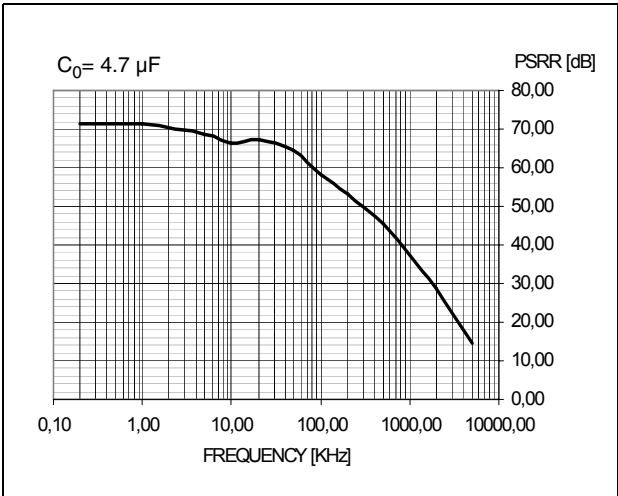


Figure 23. PSRR



2.5 Test circuit and waveforms plot

2.5.1 Load regulation

Figure 24. Load regulation test circuit

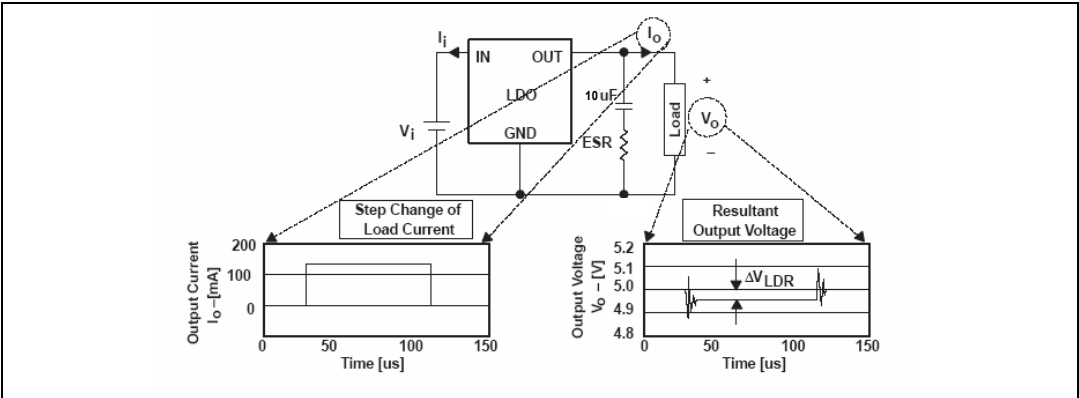
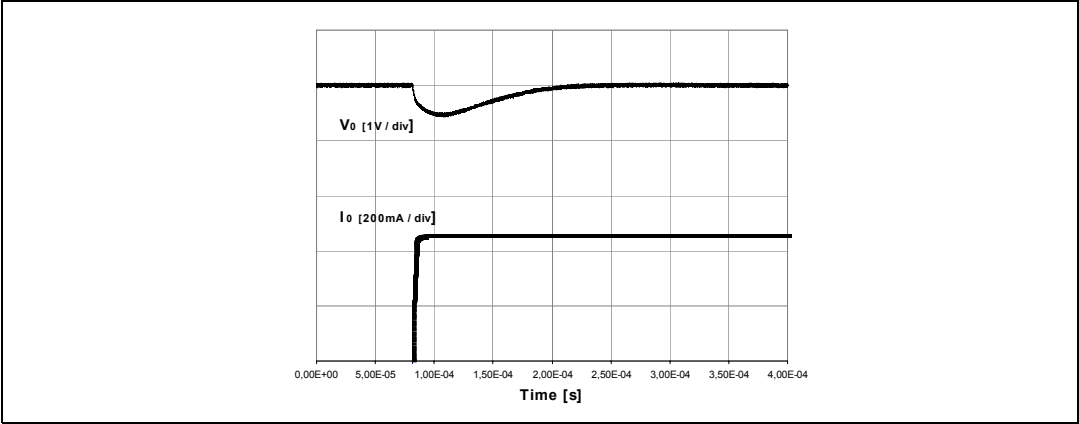
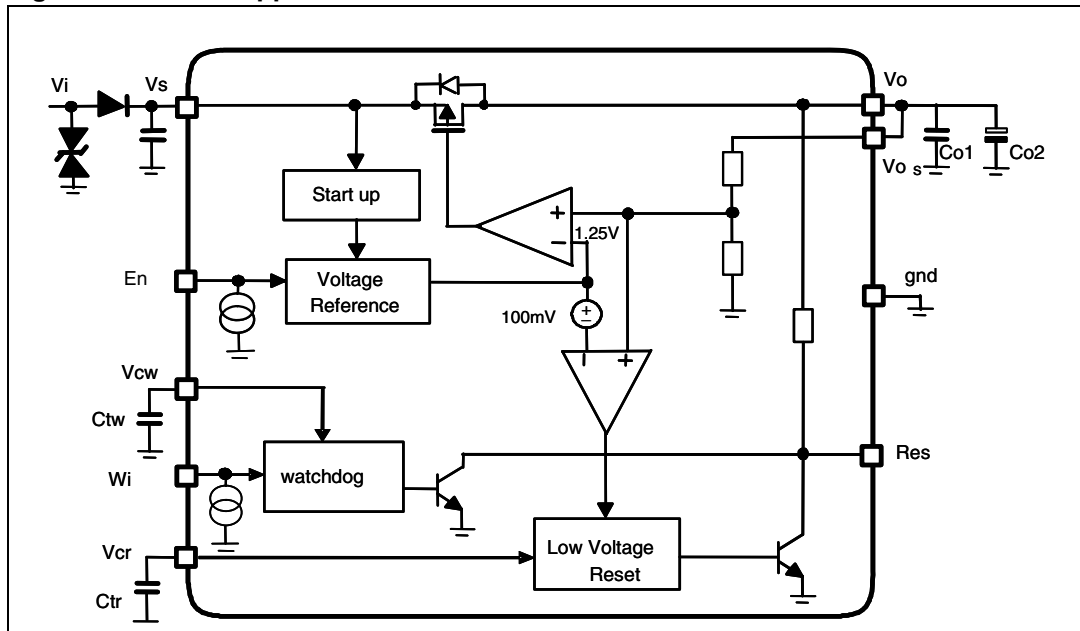


Figure 25. Maximum load variation response



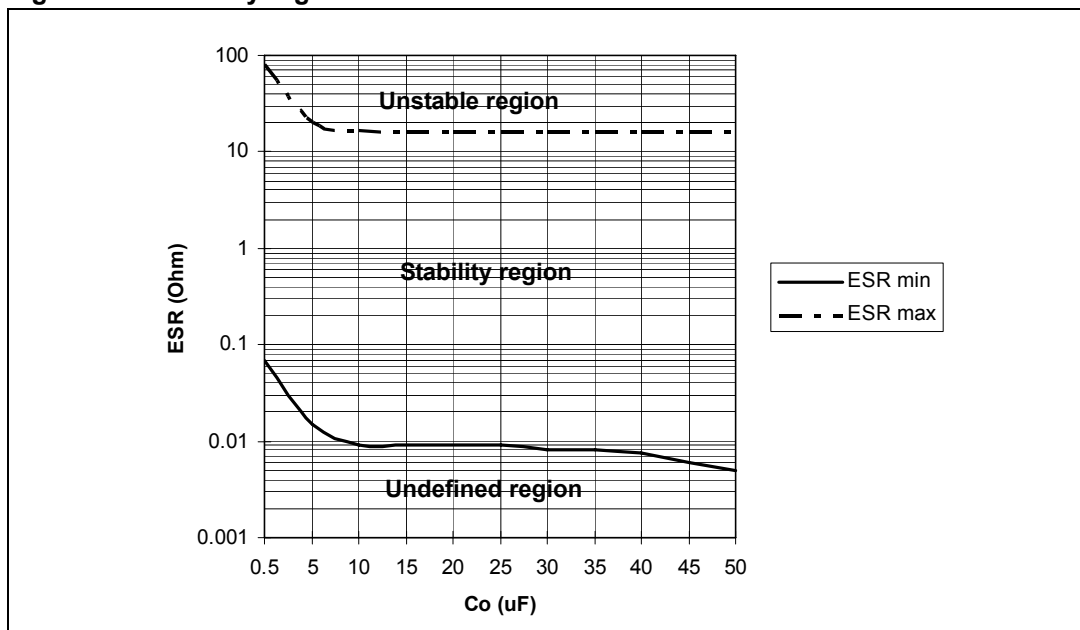
3 Application information

Figure 26. L4995 application schematic⁽¹⁾



1. The input capacitor $C_s > 200\text{nF}$ is necessary for the smoothing of line disturbances. The output capacitor $C_{O1} > 100\text{nF}$ is necessary for the stability of the regulation loop. In order to dampen output voltage oscillations during high load current surges, it is recommended an additional electrolytic capacitor $C_{O2} > 10\mu\text{F}$ to be placed at the output pin.

Figure 27. Stability region⁽¹⁾



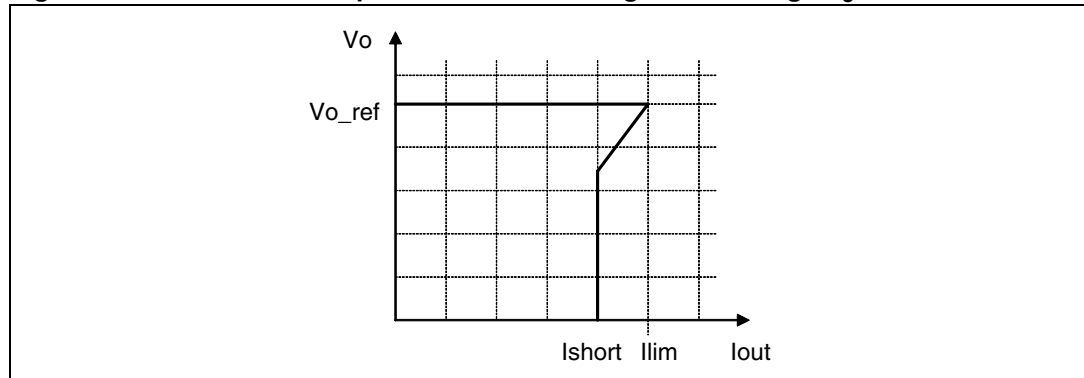
1. The curve which describes the minimum ESR is derived from characterization data on the regulator with connected ceramic capacitors which feature low ESR values (at 100 kHz). Any capacitor with further lower ESR than the given plot value must be evaluated in each and every case.

3.1 Voltage regulator

Voltage regulator uses a p-channel transistor as a regulating element. With this structure, very low dropout voltage at current up to 500mA is obtained. The output voltage is regulated up to transient input supply voltage of 40V. No functional interruption due to over-voltage pulses is generated. A short circuit protection to GND is provided.

The voltage regulator is active when E_n is high.

Figure 28. Behavior of output current versus regulated voltage V_o



3.2 Reset

The reset circuit supervises the output voltage V_o . The V_{o_th} reset threshold is defined with the internal reference voltage and a resistor output divider. If the output voltage becomes lower than V_{o_th} then R_{es} goes low with a reaction time t_{rr} . The reset low signal is guaranteed for an output voltage V_o greater than 1V.

When the output voltage becomes higher than V_{o_th} then R_{es} goes high with a delay t_{rd} . This delay is obtained by an internal oscillator.

The oscillator period is given by:

Equation 1

$$T_{osc} = [(V_{Rhth} - V_{Rlth}) \times C_{tr}] / I_{cr} + [(V_{Rhth} - V_{Rlth}) \times C_{tr}] / I_{dr}$$

where:

I_{cr} : is an internally generated charge current

I_{dr} : is an internally generated discharge current

V_{Rhth} , V_{Rlth} : are two voltages defined with the output voltage and a resistor output divider

C_{tr} : is an external capacitance.

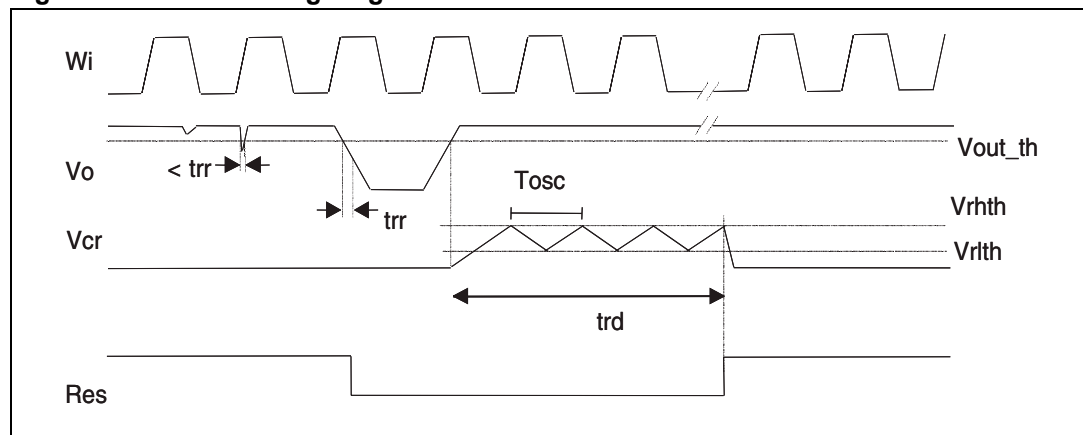
t_{rd} is given by:

Equation 2

$$t_{rd} = (V_{Rhth} \times C_{tr}) / I_{cr} + 3 \times T_{osc}$$

Reset is active when E_n is high.

Figure 29. Reset timing diagram



3.3 Watchdog

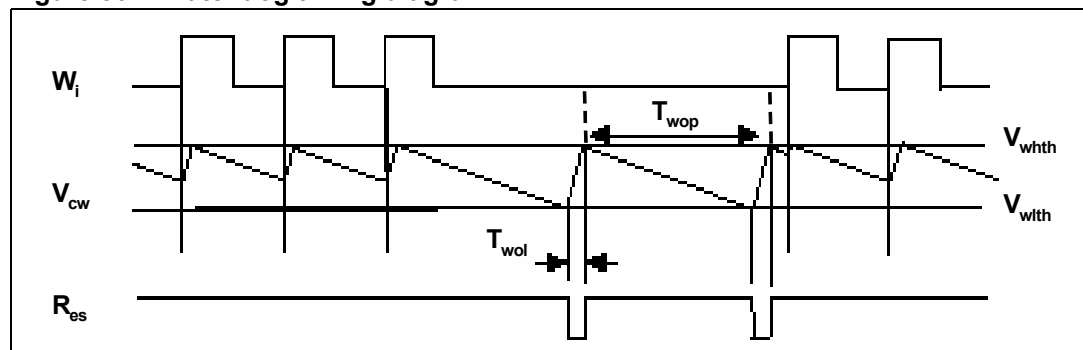
A connected microcontroller is monitored by the watchdog input W_i . If pulses are missing, the Reset output pin is set to low. The pulse sequence time can be set within a wide range with the external capacitor, C_{tw} . The watchdog circuit discharges the capacitor C_{tw} , with the constant current I_{cwd} . If the lower threshold V_{wlth} is reached, a watchdog reset is generated. To prevent this the microcontroller must generate a positive edge during the discharge of the capacitor before the voltage has reached the threshold V_{wlth} . In order to calculate the minimum time t , during which the micro-controller must output the positive edge, the following equation can be used:

Equation 3

$$(V_{whth} - V_{wlth}) \times C_{tw} = I_{cwd} \times t$$

Every W_i positive edge switches the current source from discharging to charging. The same happens when the lower threshold is reached. When the voltage reaches the upper threshold, V_{whth} , the current switches from charging to discharging. The result is a saw-tooth voltage at the watchdog timer capacitor C_{tw} .

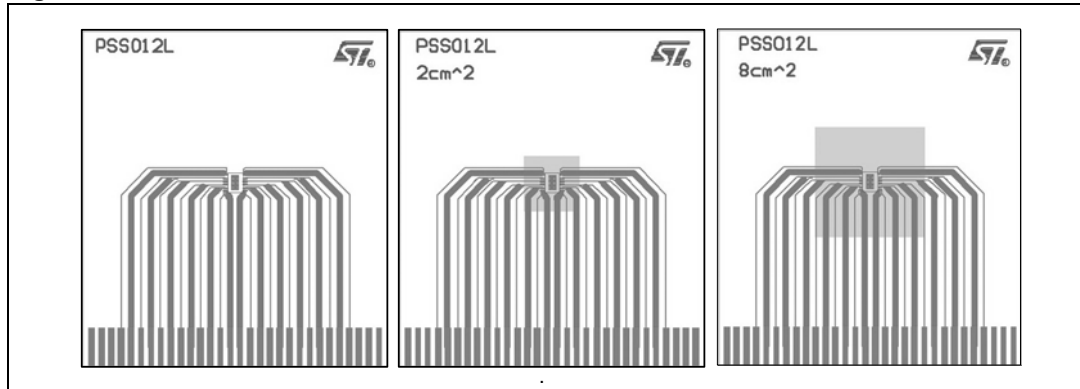
Figure 30. Watchdog timing diagram



4 Package and PCB thermal data

4.1 PowerSSO-12 thermal data

Figure 31. PowerSSO-12 PC board⁽¹⁾



1. Layout condition of R_{th} and Z_{th} measurements (PCB: Double layer, Thermal Vias, FR4 area= 77mm x 86mm, PCB thickness=1.6mm, Cu thickness=70 μ m (front and back side) Thermal vias separation 1.2 mm, Thermal via diameter 0.3 mm +/- 0.08 mm, Cu thickness on vias 0.025 mm, Footprint dimension 4.1 mm x 6.5 mm).

Figure 32. $R_{thj-amb}$ vs PCB copper area in open box free air condition

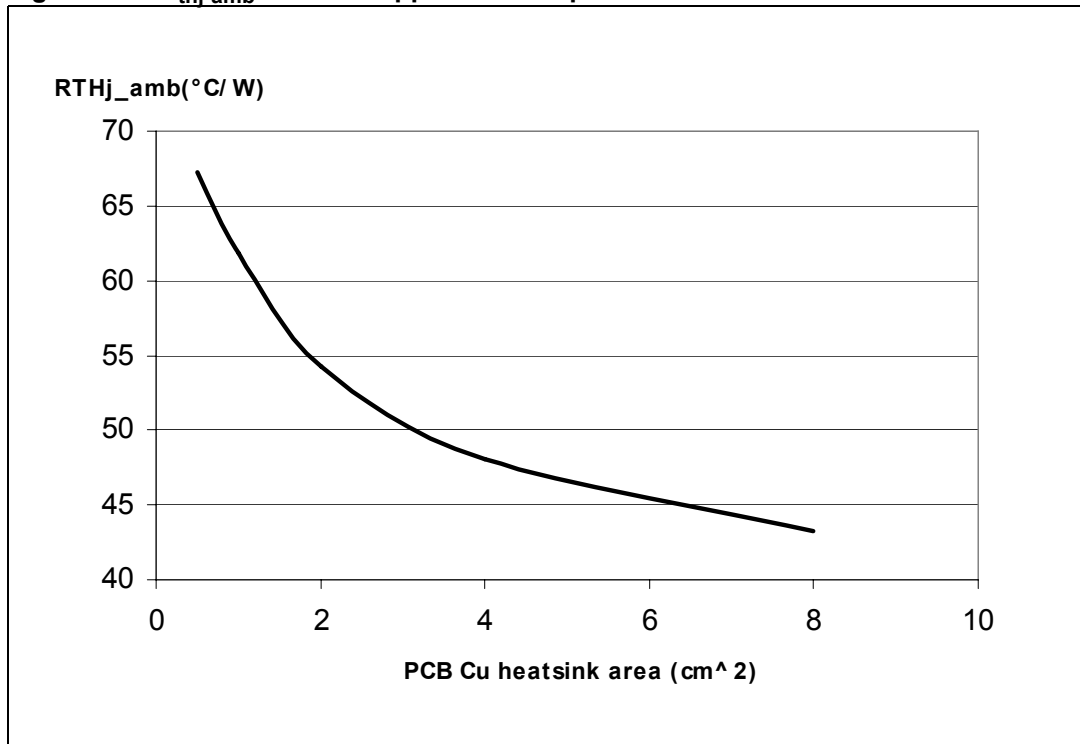
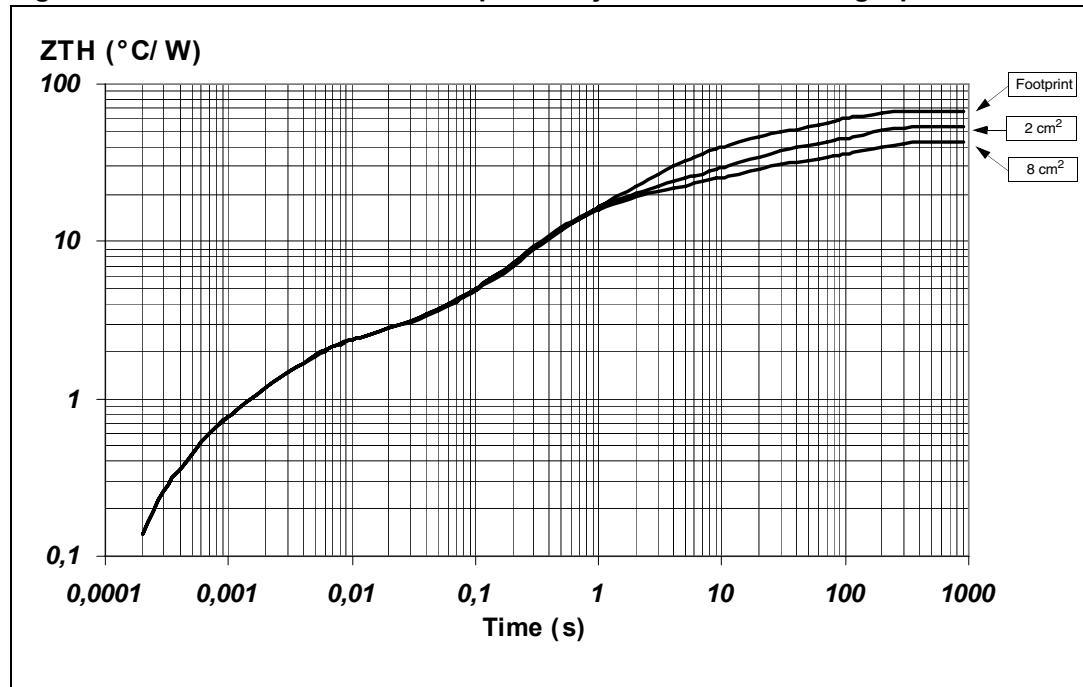


Figure 33. PowerSSO-12 thermal impedance junction ambient single pulse



Equation 4: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Figure 34. Thermal fitting model of Vreg in PowerSSO-12

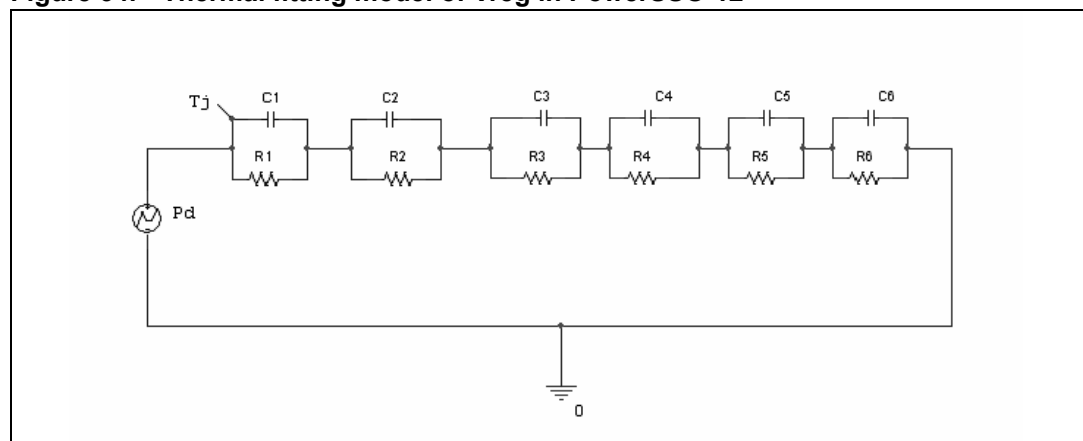
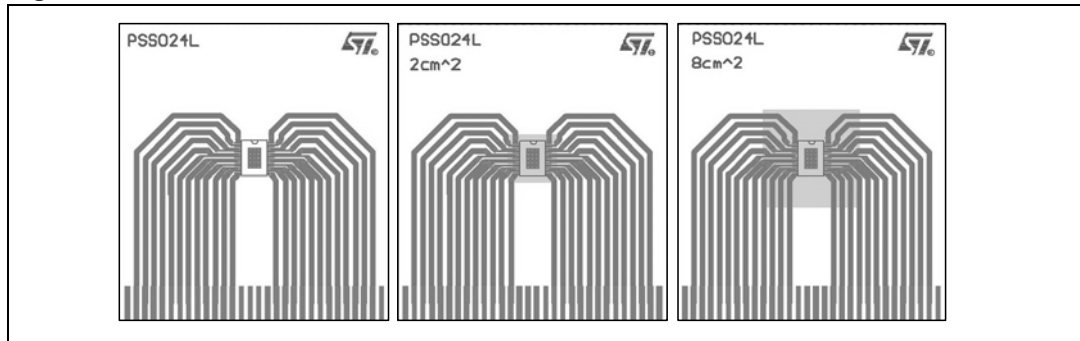


Table 9. PowerSSO-12 thermal parameter

Area/island (cm ²)	Footprint	2	8
R1 (°C/W)	0.45		
R2 (°C/W)	1.79		
R3 (°C/W)	7		
R4 (°C/W)	10	10	9
R5 (°C/W)	22	15	10
R6 (°C/W)	26	20	15
C1 (W.s/°C)	0.001		
C2 (W.s/°C)	0.0022		
C3 (W.s/°C)	0.05		
C4 (W.s/°C)	0.2	0.1	0.1
C5 (W.s/°C)	0.27	0.8	1
C6 (W.s/°C)	3	6	9

4.2 PowerSSO-24 thermal data

Figure 35. PowerSSO-24 PC board⁽¹⁾



1. Layout condition of R_{th} and Z_{th} measurements (PCB: Double layer, Thermal Vias, FR4 area= 77mm x 86mm, PCB thickness=1.6mm, Cu thickness=70 μ m (front and back side) Thermal vias separation 1.2 mm, Thermal via diameter 0.3 mm +/- 0.08 mm, Cu thickness on vias 0.025 mm, Footprint dimension 4.1 mm x 6.5 mm).

Figure 36. $R_{thj-amb}$ vs PCB copper area in open box free air condition

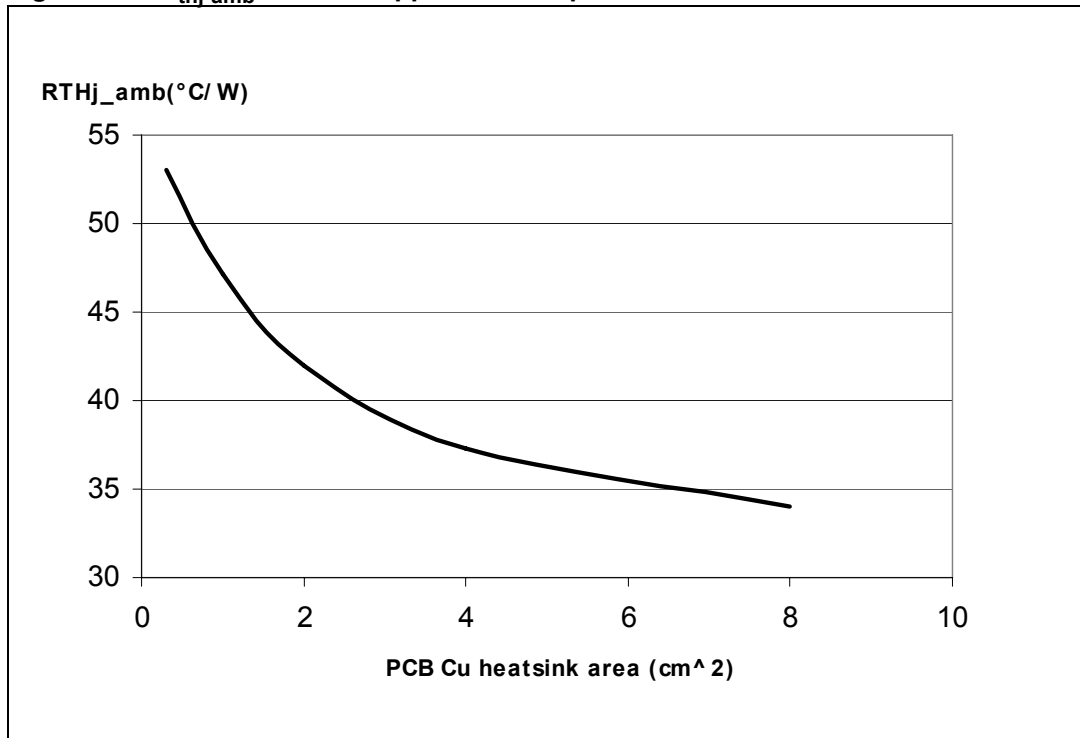
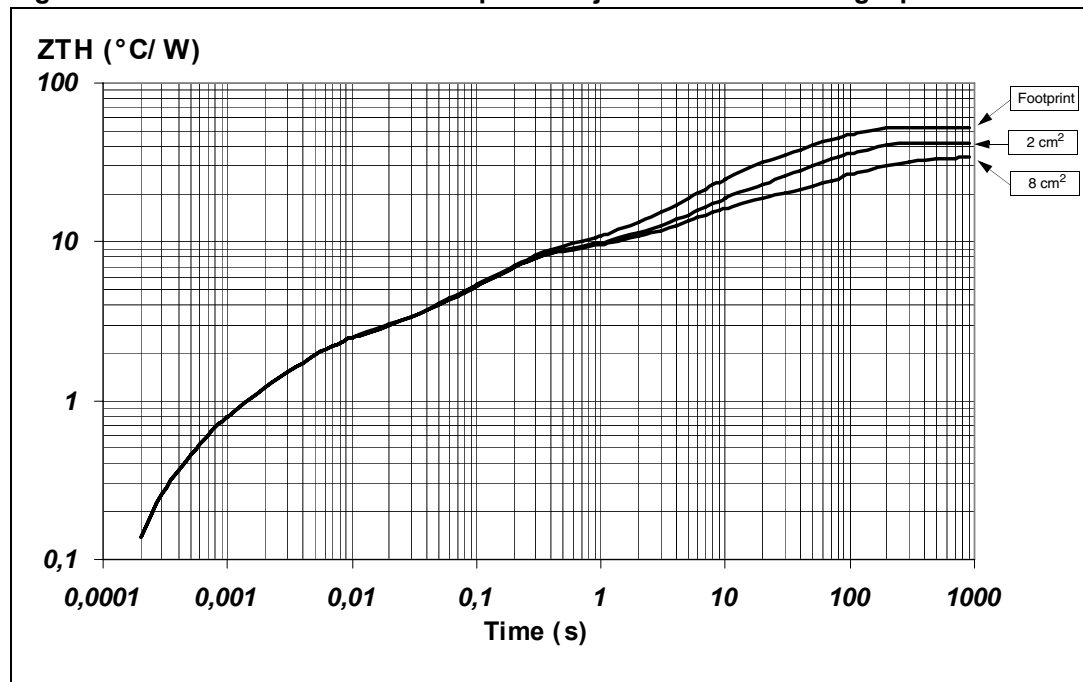


Figure 37. PowerSSO-24 thermal impedance junction ambient single pulse



Equation 5: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

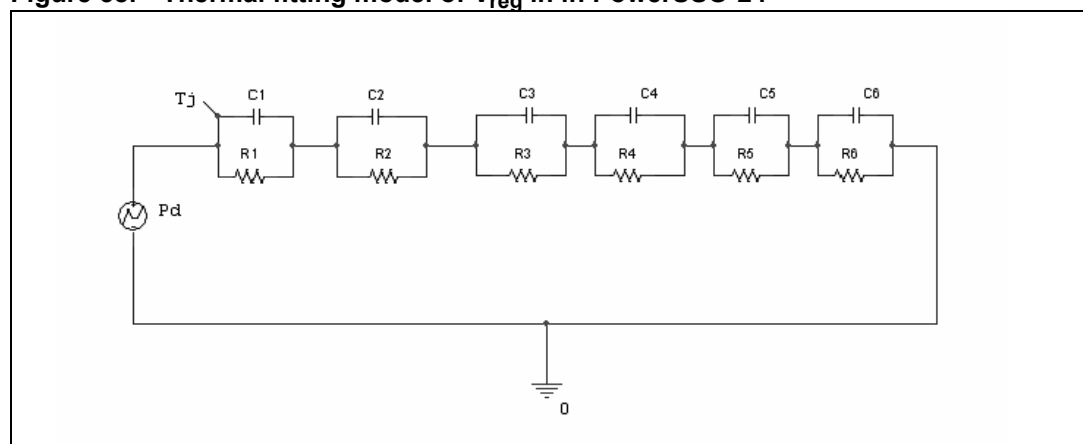
Figure 38. Thermal fitting model of V_{reg} in in PowerSSO-24

Table 10. PowerSSO-24 thermal parameter

Area/island (cm ²)	Footprint	2	8
R1 (°C/W)	0.45		
R2 (°C/W)	1.79		
R3 (°C/W)	6		
R4 (°C/W)	7.7		
R5 (°C/W)	9	9	8
R6 (°C/W)	28	17	10
C1 (W.s/°C)	0.001		
C2 (W.s/°C)	0.0022		
C3 (W.s/°C)	0.025		
C4 (W.s/°C)	0.75		
C5 (W.s/°C)	1	4	9
C6 (W.s/°C)	2.2	5	17

5 Package and packing information

5.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

Figure 39. PowerSSO-12 package dimensions

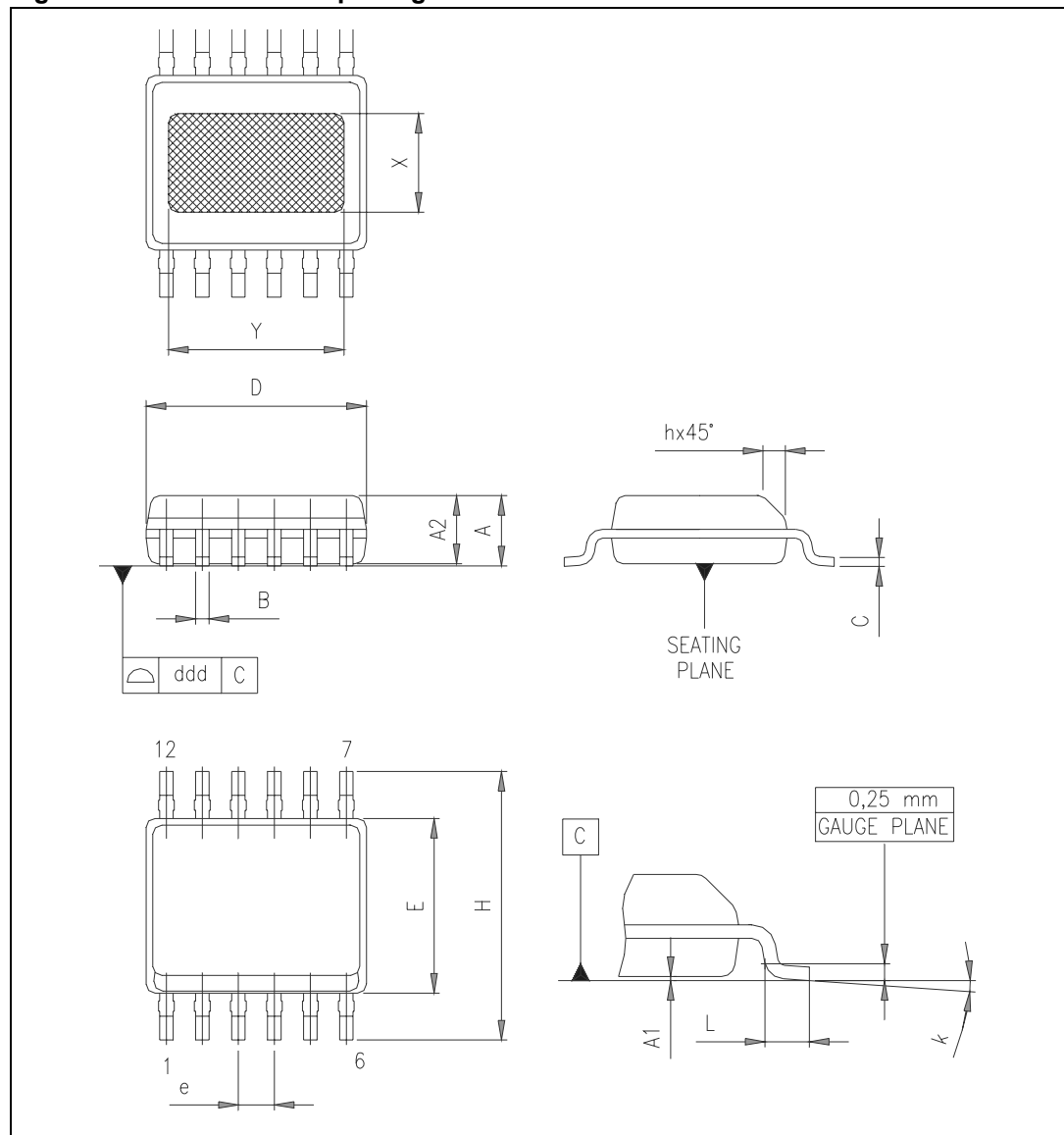


Table 11. PowerSSO-12 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	1.250		1.620
A1	0.000		0.100
A2	1.100		1.650
B	0.230		0.410
C	0.190		0.250
D	4.800		5.000
E	3.800		4.000
e		0.800	
H	5.800		6.200
h	0.250		0.500
L	0.400		1.270
k	0°		8°
X	2.200		2.800
Y	2.900		3.500
ddd			0.100

5.2 PowerSSO-24 mechanical data

Figure 40. PowerSSO-24 package dimensions

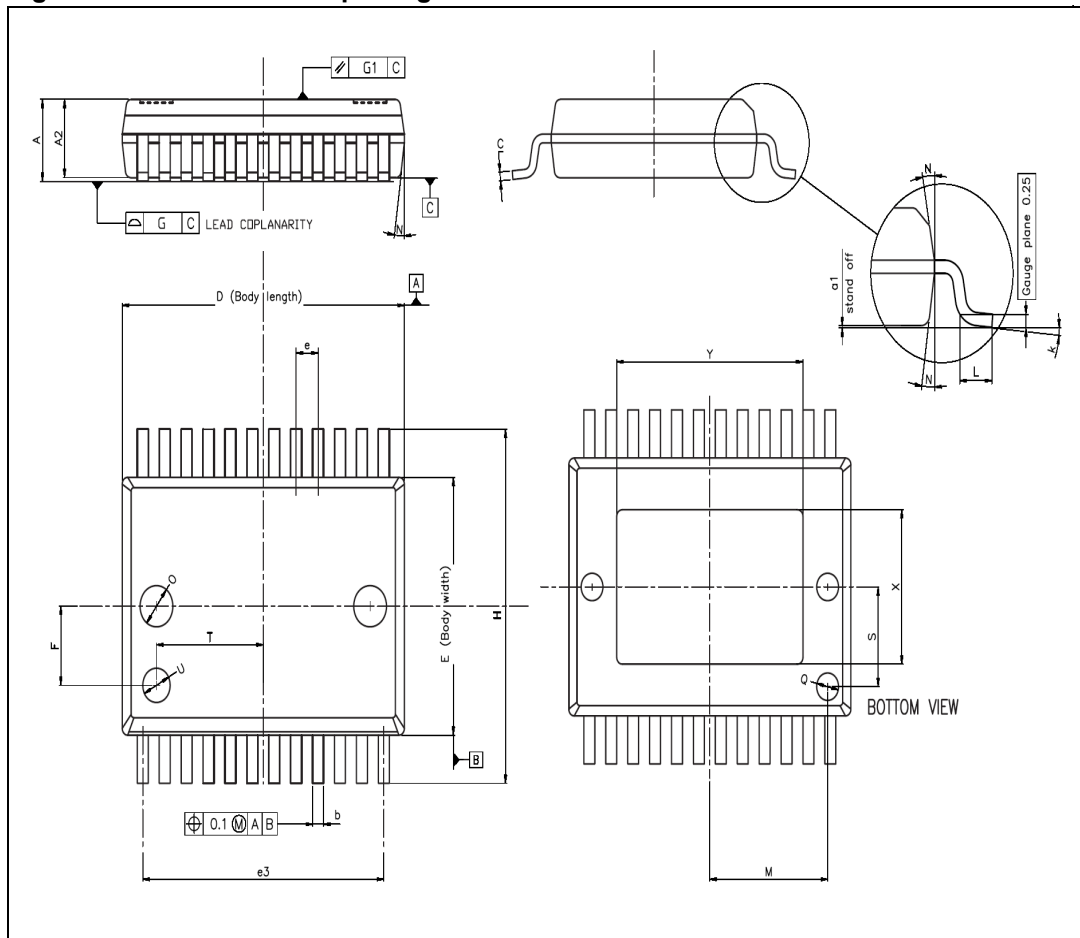


Table 12. PowerSSO-24 mechanical data⁽¹⁾⁽²⁾

Symbol	Millimeters		
	Min.	Typ.	Max.
A			2.45
A2	2.15		2.35
a1	0		0.10
b	0.33		0.51
c	0.23		0.32
D ⁽³⁾	10.10		10.50
E ⁽³⁾	7.40		7.60
e		0.8	
e3		8.8	
F		2.3	
G			0.1
G1			0.06
H	10.1		10.5
h			0.4
k	0°		8°
L	0.55		0.85
O		1.2	
Q		0.8	
S		2.9	
T		3.65	
U		1	
N			10°
X	4.1		4.7
Y	6.5 4.9 ⁽⁴⁾		7.1 5.5 ⁽⁴⁾

1. No intrusion allowed inwards the leads.
2. Flash or bleeds on exposed die pad shall not exceed 0.4 mm per side
3. "D and E" do not include mold Flash or protusions.
Mold Flash or protusions shall not exceed 0.15 mm.
4. Variations for small window leadframe option.

5.3 PowerSSO-12 packing information

Figure 41. PowerSSO-12 tube shipment (no suffix)

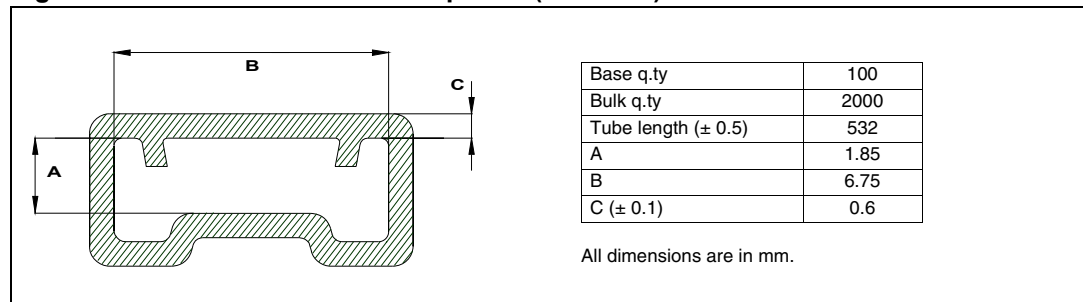
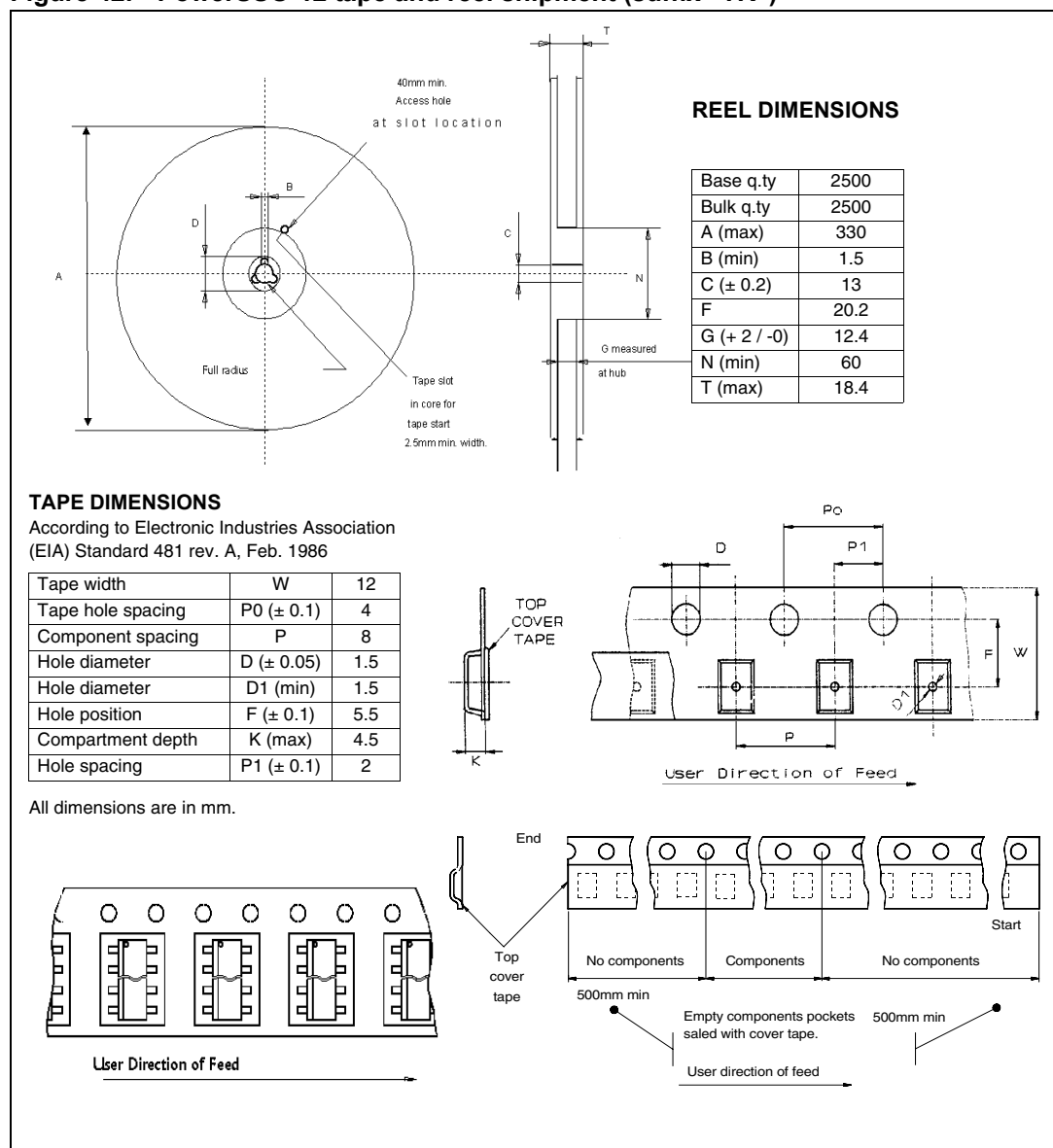


Figure 42. PowerSSO-12 tape and reel shipment (suffix "TR")



5.4 PowerSSO-24 packing information

Figure 43. PowerSSO-24 tube shipment (no suffix)

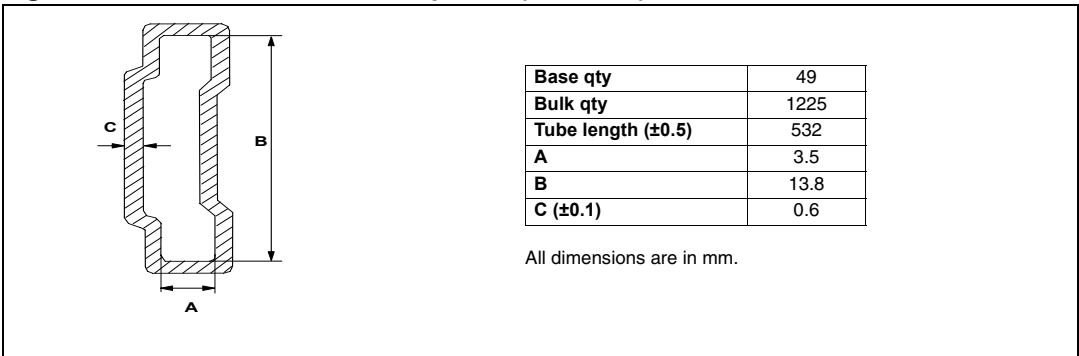
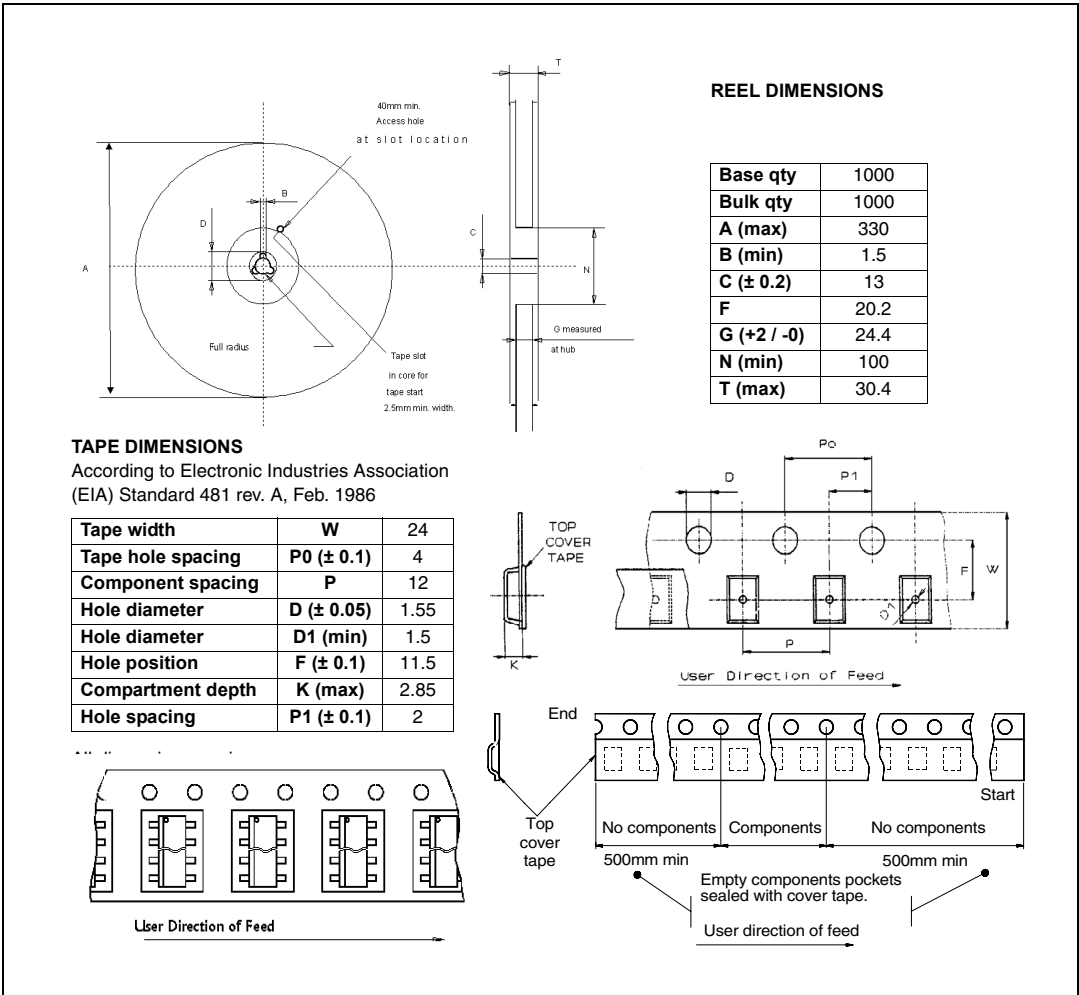


Figure 44. PowerSSO-24 tape and reel shipment (suffix “TR”)



6 Revision history

Table 13. Document revision history

Date	Revision	Changes
26-May-2006	1	Initial release.
05-Jan-2007	2	L4995A and L4995R versions added: Features section updated and table added. Table 1 updated. Table 5: General, Watchdog Iwi entry updated. Figure 2: Block diagram of L4995A and Figure 3: Block diagram of L4995R added. Table 2: Pins descriptions updated. Table 4: Thermal data updated. List of tables and List of figures added. Packaging information provided in new format. Table 11: PowerSSO-12 mechanical data X and Y values updated. Some sections reformatted for clarity. New disclaimer added.
18-May-2007	3	Updated Table 2: Pins descriptions. Updated Figure 4: Pins configurations (L4995). Table 1: Device summary changed title.
09-Jul-2007	4	Updated Table 2: Pins descriptions .
09-Aug-2007	5	Updated Table 2: Pins descriptions. Updated Table 12: PowerSSO-24 mechanical data.

Table 13. Document revision history (continued)

Date	Revision	Changes
07-Dec-2007	6	Updated Section 2.2: Thermal data: – corrected note changing single layer with double layer. Updated Table 5: General: – changed I_{short} typ. value from 750 to 800 mA – added I_{short} max. value – changed I_{lim} typ. value from 820 to 900 mA – added I_{lim} max. value – added I_{lim} note – added V_{dp} note – changed I_{qn_1} typ. value from 110 to 90 μA – added I_{qn_1} max. value – added I_{qn_50} max. value – added I_{qn_150} max. value – changed I_{qn_250} typ. value from 1.2 to 1 mA – added I_{qn_250} max. value – changed I_{qn_500} typ. value from 2.4 to 2.1 mA – added I_{qn_500} max. value Updated Table 6: Reset: – changed V_{Rlth} parameter definition from “Reset timing low” to “Reset delay circuit low threshold” – changed V_{Rhth} parameter definition from “Reset timing high” to “Reset delay circuit high threshold” – added T_{rd} min. and max. values Updated Table 7: Watchdog: – added I_{wi} max value Updated Table 8: Enable: – changed Pull down current symbol from R_{En} to I_{En} – changed I_{En} typ. value from 2.5 to 10 μA – added I_{En} max. value Added Section 2.4: Electrical characteristics curves. Added Section 2.5: Test circuit and waveforms plot. Added Section 4: Package and PCB thermal data
03-Oct-2008	7	Updated PowerSSO-24 information: – changed Figure 40: PowerSSO-24 package dimensions – changed Table 12: PowerSSO-24 mechanical data.
19-Mar-2009	8	Updated Table 4: Thermal data
19-May-2009	9	Updated Table 2: Pins descriptions. Updated Figure 4: Pins configurations (L4995) – Changed GND to substrate

Table 13. Document revision history (continued)

Date	Revision	Changes
24-Jun-2009	10	<i>Table 12: PowerSSO-24 mechanical data:</i> – Deleted A (min) value – Changed A (max) value from 2.50 to 2.45 – Changed A2 (max) value from 2.40 to 2.35 – Updated K row – Changed L (min) value from 0.6 to 0.55 – Changed L (max) value from 1 to 0.85
12-Jul-2010	11	Added <i>Figure 27: Stability region⁽¹⁾</i> .

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER'S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2010 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com