L6728

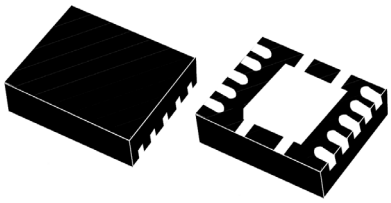
Single phase PWM controller with Power Good

Features

- Flexible power supply from 5 V to 12 V
- Power conversion input as low as 1.5 V
- 0.8 V internal reference
- 0.8 % output voltage accuracy
- High-current integrated drivers
- Power Good output
- Sensorless and programmable OCP across low-side $R_{DS(on)}$
- OV / UV protections
- VSEN disconnection protection
- Oscillator internally fixed at 300 kHz
- LSless to manage pre-bias start-up
- Adjustable output voltage
- Disable function
- Internal soft-start
- DFN10 package

Applications

- Memory and termination supply
- Subsystem power supply (MCH, IOCH, PCI...)
- CPU and DSP power supply
- Distributed power supply
- General DC-DC converters



DFN10

Description

L6728 is a single-phase step-down controller with integrated high-current drivers that provides complete control logic and protection to realize in a simple way general DC-DC converters by using a compact DFN10 package.

Device flexibility allows managing conversions with power input V_{IN} as low as 1.5 V and device supply voltage ranging from 5 V to 12 V.

L6728 provides simple control loop with voltage mode EA. The integrated 0.8 V reference allows regulating output voltages with ±0.8 % accuracy over line and temperature variations. Oscillator is internally fixed to 300 kHz.

L6728 provides programmable dual level over current protection as well as over and under voltage protection. Current information is monitored across the low-side MOSFET $R_{DS(on)}$ saving the use of expensive and space-consuming sense resistors.

PGOOD output easily provides real-time information on output voltage status, through VSEN dedicated output monitor.

Table 1. Device summary

Order codes	Package	Packaging
L6728	DFN10	Tube
L6728TR		Tape and reel

Table 2. Pins description (continued)

Pin #	Name	Function
9	VSEN	Regulated voltage sense pin for OVP and UVP protections and PGOOD. Connect to the output regulated voltage, or to the output resistor divider if the regulated voltage is higher than the reference.
10	PGOOD	Open drain output set free after SS has finished and pulled low when VSEN is outside the relative window. Pull up to a voltage equal or lower than VCC. If not used it can be left floating.

3 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{th(JA)}$	Thermal resistance junction to ambient (Device soldered on 2s2p, 67 mm x 69 mm board)	45	°C/W
$R_{th(JC)}$	Thermal resistance junction to case	5	°C/W
T_{MAX}	Maximum junction temperature	150	°C
T_{STG}	Storage temperature range	-40 to 150	°C
T_J	Junction temperature range	-40 to 125	°C
P_{TOT}	Maximum power dissipation at T_A = 25 °C	2.25	W

4 Electrical specifications

4.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
VCC	to GND	-0.3 to 15	V
V_{BOOT}, V_{UGATE}	to PHASE to GND to GND; t < 200 ns	15 33 45	V
V_{PHASE}	to GND to GND; t < 200 ns	-5 to 18 -8 to 30	V
V_{LGATE}	to GND	-0.3 to VCC+0.3	V
	FB, COMP, VSEN to GND	-0.3 to 3.6	V
	PGOOD to GND	-0.3 to VCC+0.3	V

4.2 Electrical characteristics

Table 5. Electrical characteristics
(V_{CC} = 5 V to 12 V; T_J = 0 to 70 °C unless otherwise specified)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Supply current and power-ON						
I_{CC}	VCC supply current	UGATE and LGATE = OPEN		6		mA
I_{BOOT}	BOOT supply current	UGATE = OPEN; PHASE to GND		0.7		mA
UVLO	VCC Turn-ON	VCC rising			4.1	V
	Hysteresis			0.2		V
Oscillator						
F_{SW}	Main oscillator accuracy		270	300	330	kHz
ΔV_{OSC}	PWM ramp amplitude			1.4		V
d_{MAX}	Maximum duty cycle		80			%
Reference and error amplifier						
	Output voltage accuracy		-0.8	-	0.8	%
A_0	DC gain (1)			120		dB
GBWP	Gain-bandwidth product (1)			15		MHz
SR	Slew-rate (1)			8		V/µs
DIS	Disable threshold	COMP falling	0.70		0.85	V

Table 5. Electrical characteristics (continued)
(V_{CC} = 5 V to 12 V; T_J = 0 to 70 °C unless otherwise specified)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Gate drivers						
I_{UGATE}	HS source current	BOOT - PHASE = 5 V		1.5		A
R_{UGATE}	HS sink resistance	BOOT - PHASE = 5 V		1.1		Ω
I_{LGATE}	LS source current	VCC = 5 V		1.5		A
R_{LGATE}	LS sink resistance	VCC = 5 V		0.65		Ω
Over-current protection						
I_{OCSET}	OCSET current source	Sourced from LGATE pin, during OC setting phase.	9	10	11	µA
V_{OC_SW}	OC switch-over threshold	$V_{LGATE/OC}$ rising		600		mV
Over and under-voltage protections						
OVP	OVP threshold	VSEN rising	0.970	1.000	1.030	V
		un-latch, VSEN falling	0.35	0.40	0.45	V
UVP	UVP threshold	VSEN falling	0.570	0.600	0.630	V
VSEN	VSEN bias current	Sourced from VSEN		100		nA
PGOOD						
PGOOD	Upper threshold	VSEN rising	0.860	0.890	0.920	V
	Lower threshold	VSEN falling	0.680	0.710	0.740	V
V_{PGOODL}	PGOOD voltage low	I_{PGOOD} = -4 mA			0.4	V

1. Guaranteed by design, not subject to test.

14 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at

Table 8. DFN10 mechanical data

Dim.	mm			mils		
	Min	Typ	Max	Min	Typ	Max
A	0.80	0.90	1.00	31.5	35.4	39.4
A1		0.02	0.05		0.8	2.0
A2		0.70			27.6	
A3		0.20			7.9	
b	0.18	0.23	0.30	7.1	9.1	11.8
D		3.00			118.1	
D2	2.21	2.26	2.31	87.0	89.0	90.9
E		3.00			118.1	
E2	1.49	1.64	1.74	58.7	64.6	68.5
e		0.50			19.7	
L	0.3	0.4	0.5	11.8	15.7	19.7
M		0.75			29.5	
m		0.25			9.8	

Figure 19. Package dimensions