UM2255
User manual

SPC58NG-DISP user manual

Introduction

The SPC58NG-DISP Discovery board is the hardware platform to evaluate and to develop applications with SPC58NG84E7 microcontroller at budget price.

This document describes the hardware architecture of the board and how it is possible to enable specific functions.

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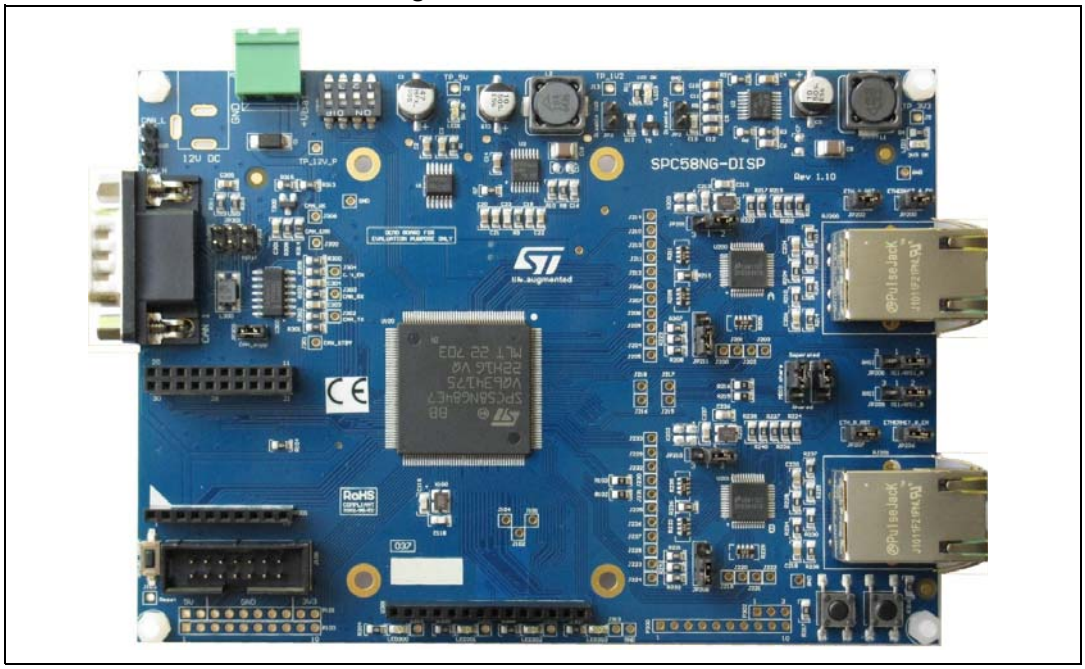
Figure 1. SPC58NG-DISP



The SPC58NG-DISP discovery board is based on the microcontroller SPC58NG84E7, a high performance e200z4d triple core 32-bit Power Architecture® technology CPU, 6 MB Flash with HSM cryptography in an eTQFP176 package.

The several interfaces including GPI/O's, peripherals such as DSPI, LINFlexD (LIN and UART), FlexRay, M_CAN ISO CAN-FD and two Ethernet ports make the SPC570S-DISP an excellent starter kit for the customer to quickly evaluate the microcontroller as well as to develop and debug application.

Free ready-to-run application firmware examples are available inside SPC5Studio (www.st.com/spc5studio) to support quick evaluation and development.

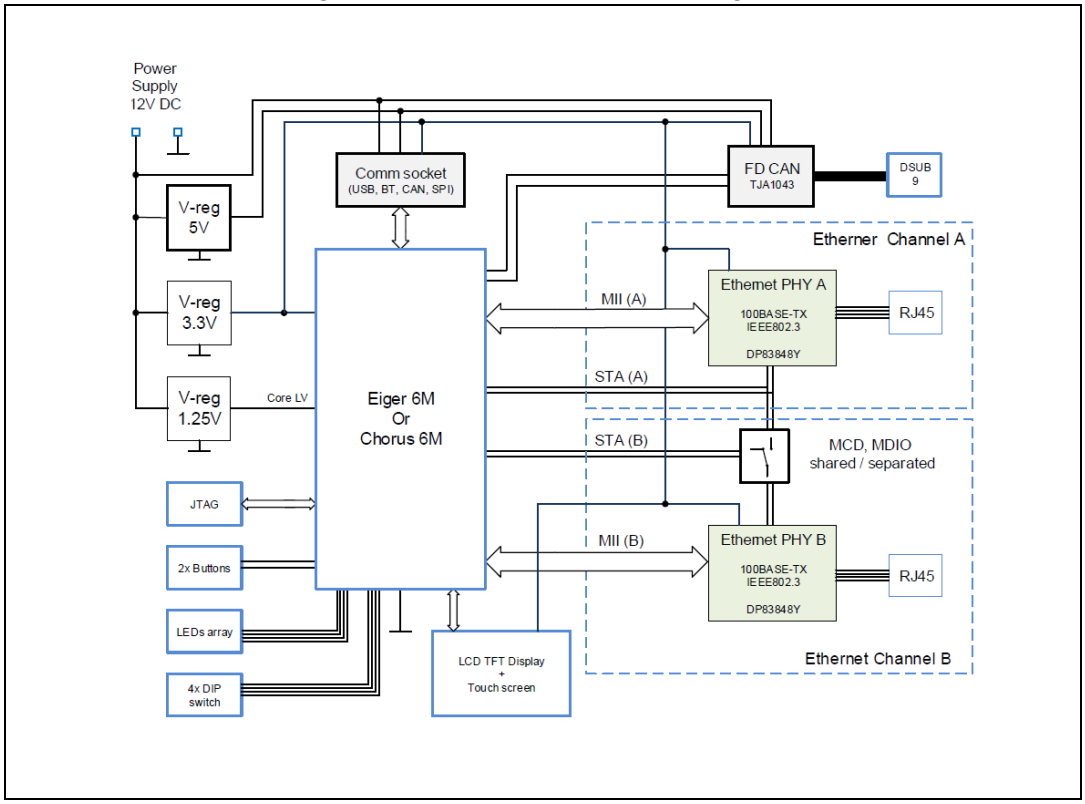
The PCB, the components and all HW parts assembled in this board meet requirements of the applicable RoHS directives.

1.1 I/O interface and connectors

- 2 Ethernet ports 100BASE-TX
- 1 CAN FD port with DB9 connector
- 1 CAN + 1 LIN/UART +1 SPI
- 2 FlexRay channels
- JTAG (Header 2 x 7 pin)
- 4 LED’s User
- 4 DIP switches
- 2 User push buttons
- 12VDC power supply (external PSU)
- RESET push button
- 40MHz crystal
- Option: LCD TFT display (320 x 240) with touch screen

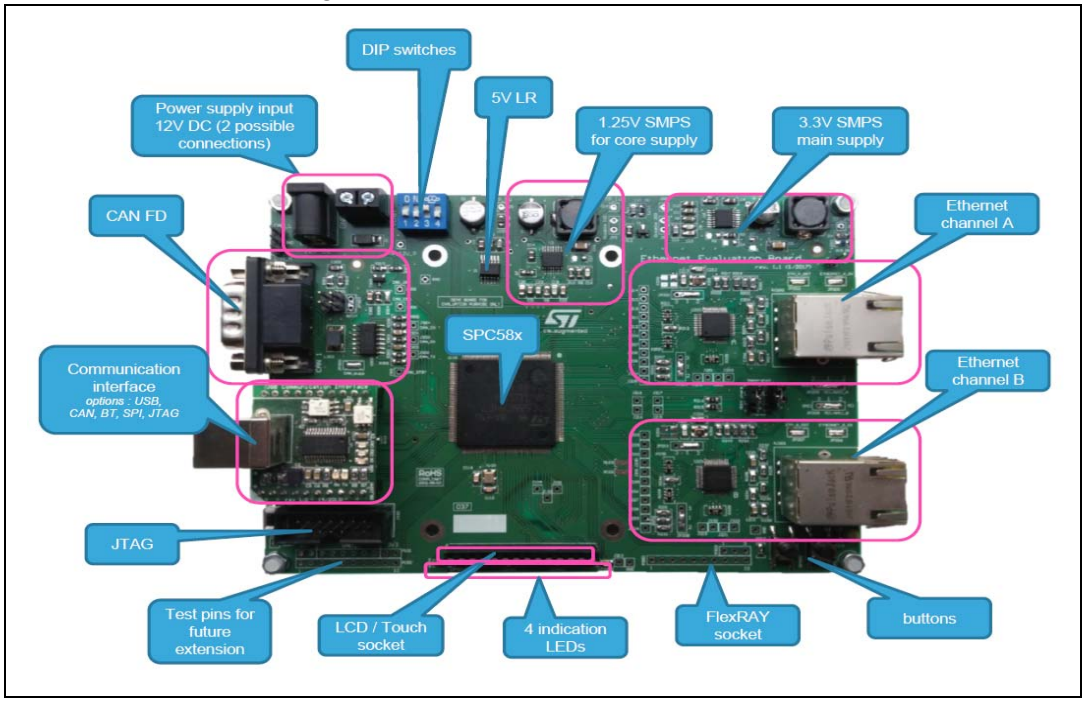
2 SPC58NG-DISP block diagram

Figure 2. SPC58NG-DISP block diagram



3 Hardware overview

Figure 3. SPC58NG-DISP: HW overview



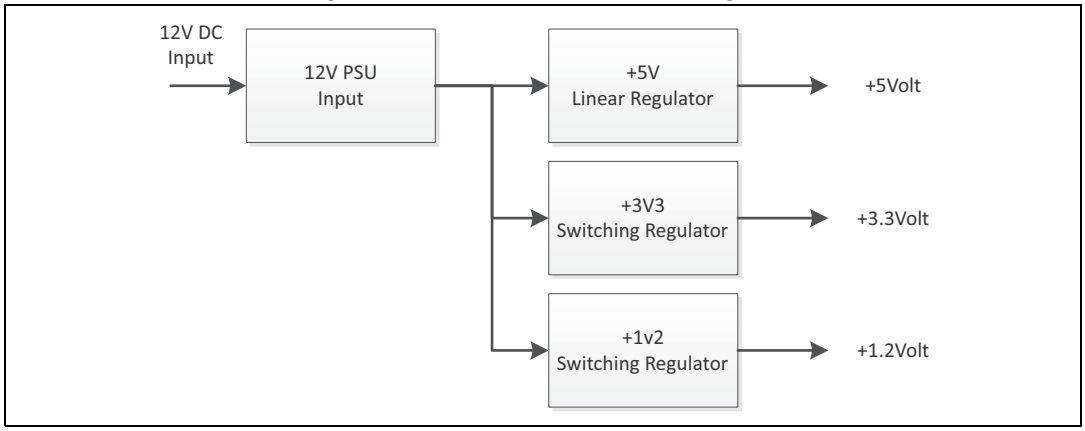
3.1 Power supply section

Figure 4 shows the PSU block diagram.

The DC input source is 12 V and three voltage regulators generate +5 V, 3.3 V and 1.2 V supply voltages.

The LEDs D1, D2 and D3 are used to monitor the output of each voltage regulator as well as the test points J2, J3, J5 and J13 to allow measuring the voltage levels 12 V, 5 V, 3.3 V and 1.2 V respectively.

Figure 4. PSU section – Block diagram

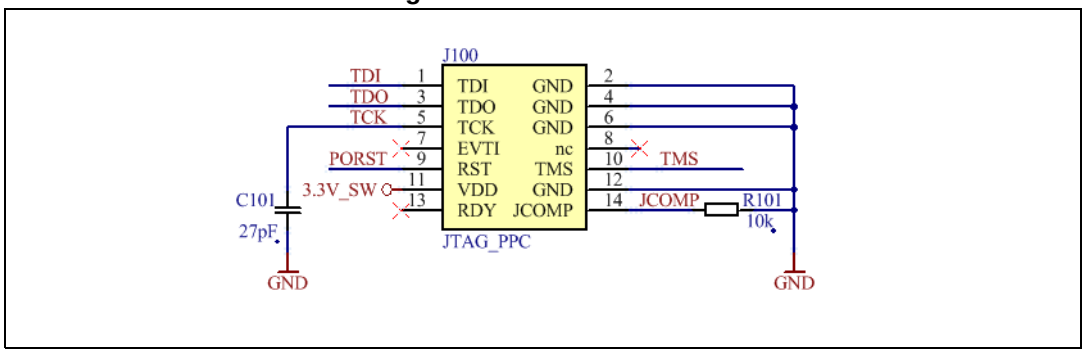


3.2 Microcontroller section

3.2.1 Programmer/debugger JTAG port

A standard 14 pin JTAG port is available for programming and debugging (*Figure 5*).

Figure 5. JTAG connector



3.3 User LEDs and user buttons

In the board, the following functions are available:

- 4 LEDs (*Figure 6*)
- 2 pushbuttons (*Figure 7*)
- 4 DIP switches (*Figure 8*)

Figure 6. User LEDs

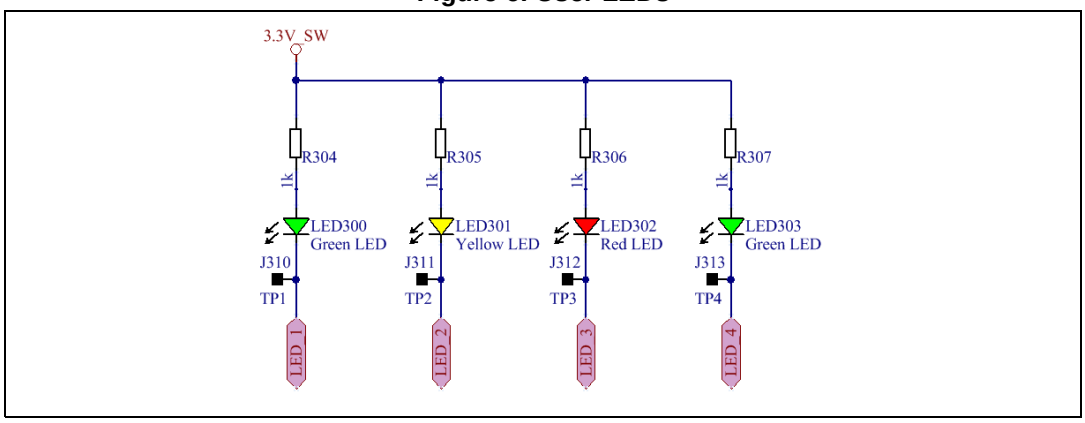


Figure 7. User push buttons

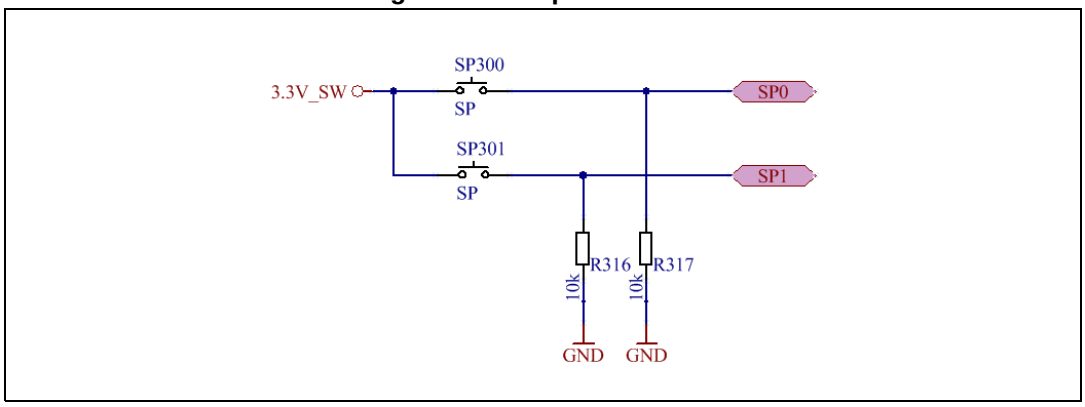
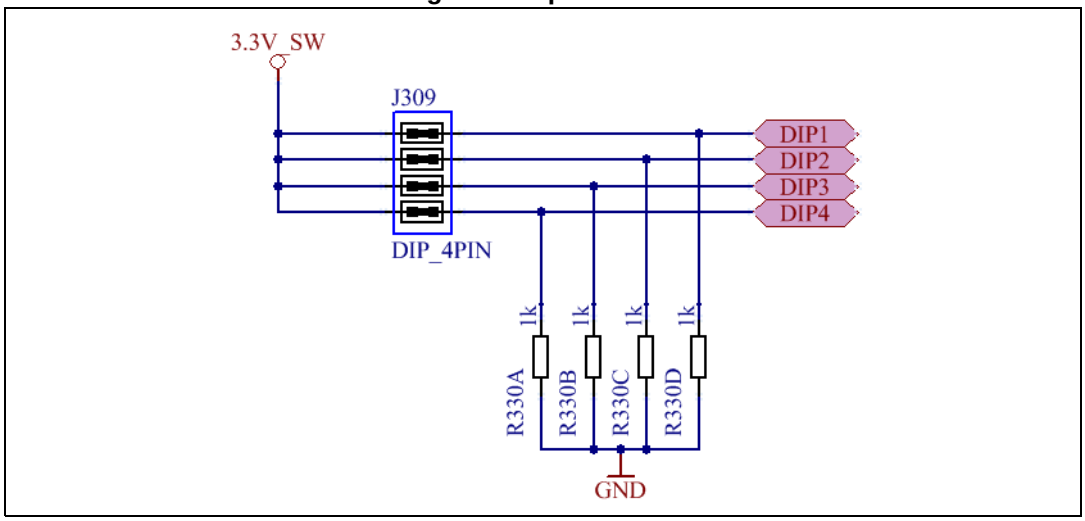
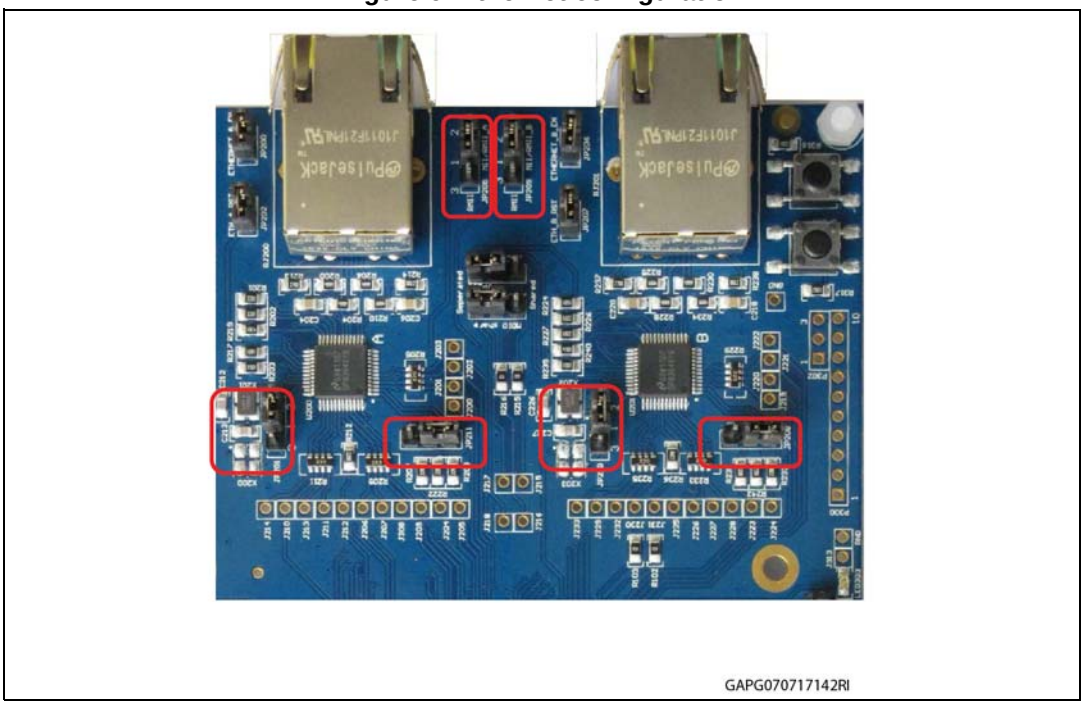


Figure 8. Dip switches



3.4 Ethernet configuration

Figure 9. Ethernet configuration



3.4.1 Ethernet MII / RMII configuration

Table 1. Ethernet MII jumper configuration

Default Configuration - MII	
Jumper	**Jumper setting**
JP205	1-2
JP201	1-2
JP211	1-2
JP209	1-2
JP210	1-2
JP208	1-2

Table 2. Ethernet RMII jumper configuration

Default Configuration - MII	
Jumper	Jumper Setting
JP205	1-3
JP201	1-3
JP211	1-3

Table 2. Ethernet RMII jumper configuration (continued)

Default Configuration - MII	
JP209	1-3
JP210	1-3
JP208	1-3
X200	Assembled
X203	Assembled

3.4.2 Ethernet PHY Serial Management

Table 3. Ethernet - Configuration for separated management

Configuration for separated management	
MDC0, MDIO0 linked to ETH0	
MDC1, MDIO1 linked to ETH1	
JP203	1-2
JP204	1-2

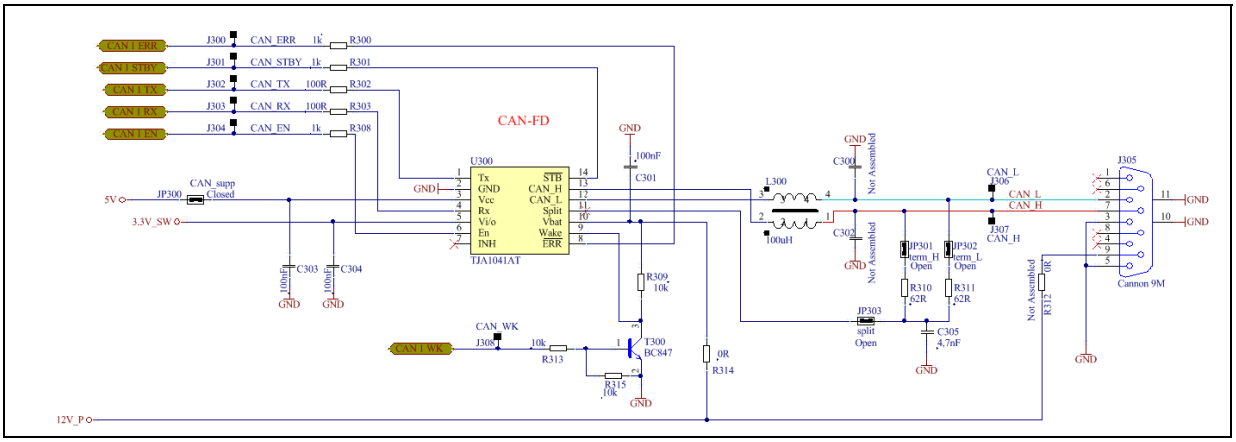
Table 4. Ethernet - Configuration for share management

Configuration for shared management	
MDC0, MDIO0 linked to ETH0 and ETH1	
ETH0 = address 1	
ETH1 = address 3	
JP203	1-3
JP204	1-3

3.5 CAN-FD

Figure 10 shows the CAN-FD section with transceiver and the DB9 connector.

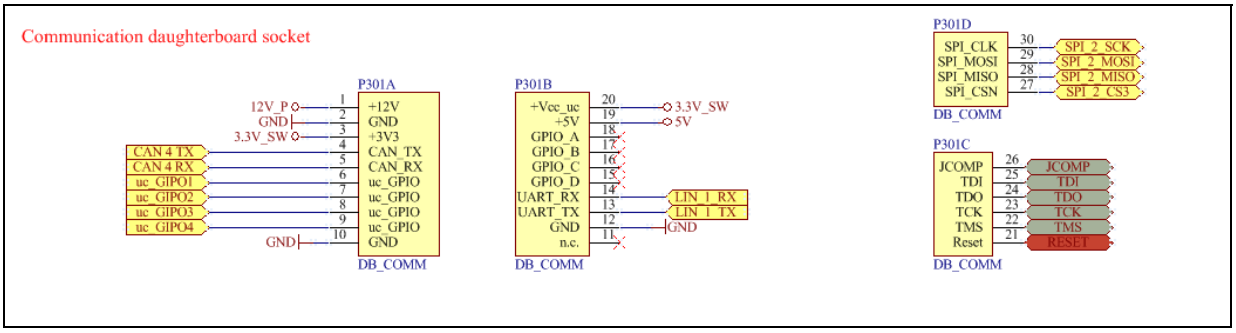
Figure 10. CAN-FD



3.6 Communication daughter board socket

The functionality of SPC58NG-DISP increases plugging some additional daughter boards in the connectors P301, P301B, P301C and P301D (see *Figure 11*).

Figure 11. Communication daughter board socket



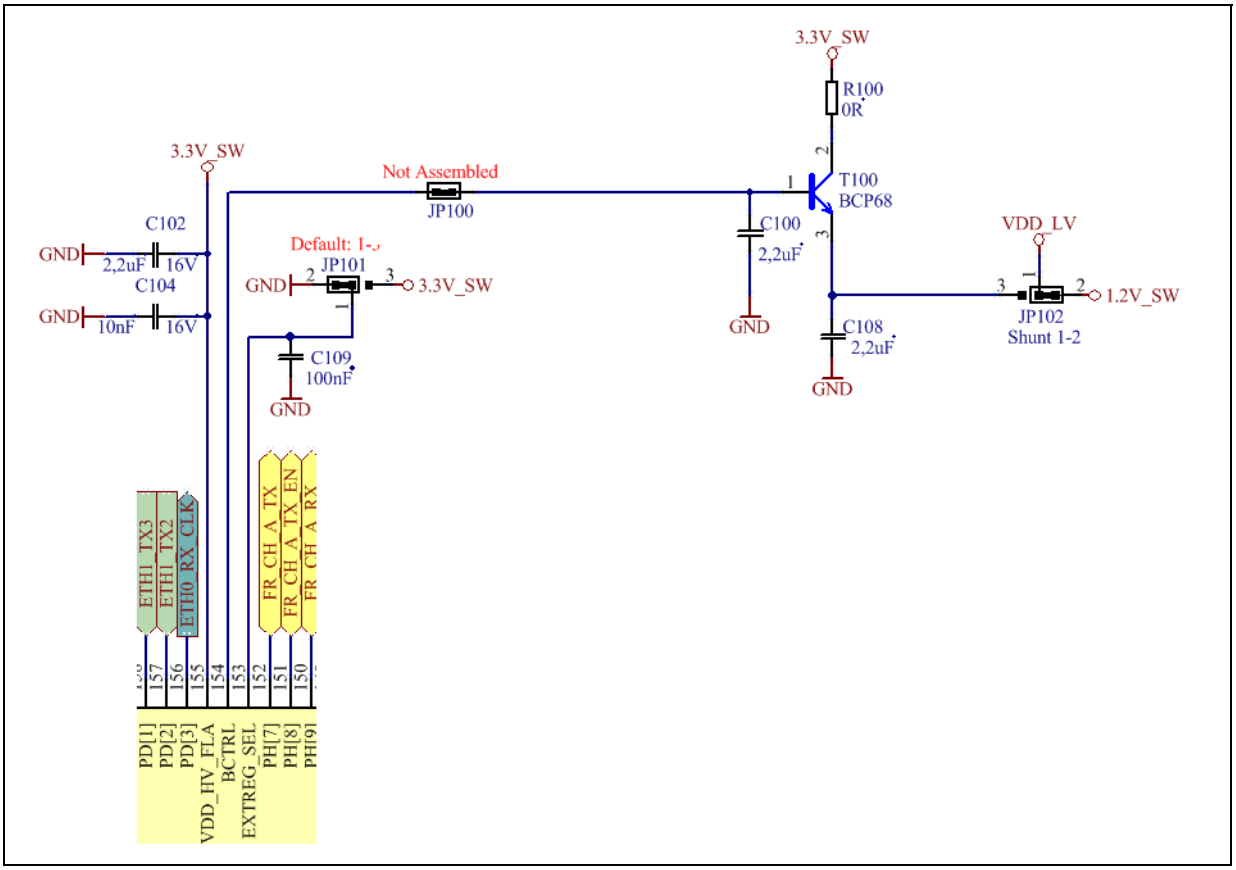
3.6.1 Power supply configuration - Jumper configuration

The default configuration enabled the supply from an external supply source (1.2_SW). The jumper configuration is reported in *Table 5*.

Table 5. Power supply configuration - Jumper configuration

	Configuration	Note
JP102	1-2	VDD_LV from 1.2 V SW
JP101	1-3	
JP100	open	
R100	Not assembled	Recommended
R102	Not assembled	
R103	Not assembled	

Figure 12. Microcontroller Power Supply configuration



4 Revision history

Table 6. Document revision history

Date	Revision	Changes
31-Jul-2017	1	Initial release.
03-Sep-2018	2	Updated *Introduction*. Minor text changes.