



STD70NS04ZL

N-channel clamped 9.5 mΩ 70 A DPAK
fully protected SAFeFET™ Power MOSFET

Features

Type	V _{DSS}	R _{DS(on)} max	I _D
STD70NS04ZL	Clamped	< 10.5 mΩ	70 A

- Low capacitance and gate charge
- 100% avalanche tested
- 175 °C maximum junction temperature

Applications

- Switching applications
 - ABS, solenoid drivers
 - Motor control
 - DC-DC converters

Description

This fully clamped Power MOSFET is produced by using the latest advanced company's Mesh OVERLAY process which is based on a novel strip layout. The inherent benefits of the new technology coupled with the extra clamping capabilities make this product particularly suitable for the harshest operation conditions such as those encountered in the automotive environment. Any other application requiring extra ruggedness is also recommended.

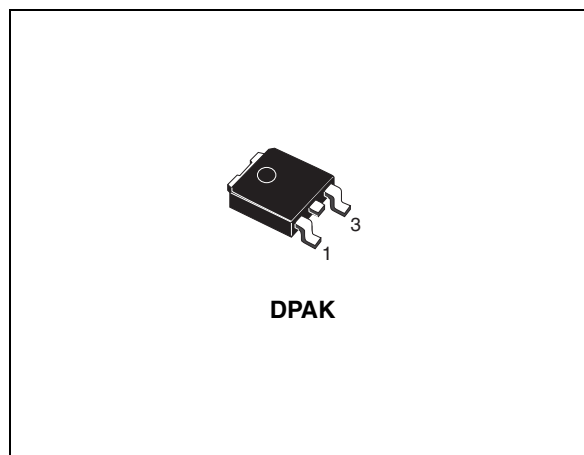


Figure 1. Internal schematic diagram

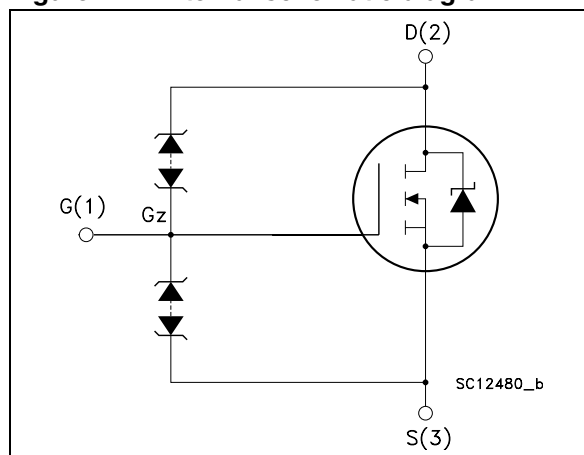


Table 1. Device summary

Order codes	Marking	Package	Packaging
STD70NS04ZL	70NS04ZL	DPAK	Tape and reel

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	33 ⁽¹⁾	V
V_{DG}	drain-gate voltage	33 ⁽¹⁾	V
V_{GS}	Gate-source voltage	± 20 ⁽¹⁾	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	70	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	50	A
I_{DG}	Drain gate current (continuous)	± 50	mA
I_{GS}	Gate-source current (continuous)	± 50	mA
I_{DM} ⁽²⁾	Drain current (pulsed)	280	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	110	W
	Derating factor	0.73	W/ $^{\circ}\text{C}$
$V_{ESD(G-S)}$	Gate-source ESD (HBM-C=100 pF, R=1.5 k Ω)	± 8	kV
$V_{ESD(G-D)}$	Gate-drain ESD (HBM-C=100 pF, R=1.5 k Ω)	± 8	kV
$V_{ESD(D-S)}$	Drain-source ESD (HBM-C=100 pF, R=1.5 k Ω)	± 8	kV
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 175	$^{\circ}\text{C}$

1. Voltage is limited by zener diodes

2. Pulse width limited by safe operating area

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	1.36	$^{\circ}\text{C}/\text{W}$
$R_{thj-pcb}$ ⁽¹⁾	Thermal resistance junction-pcb max	50	$^{\circ}\text{C}/\text{W}$

1. When mounted on 1 inch² 2 oz. FR4 Cu.

Table 4. Avalanche data

Symbol	Parameter	Value	Unit
I_{AS}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	30	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AS}$, $V_{DD} = 21\text{ V}$) (see Figure 17, Figure 18)	650	mJ

2 Electrical characteristics

($T_{CASE}=25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DG}$	Clamped voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$ $-40 < T_j < 175\text{ }^{\circ}\text{C}$	33		41	V
$V_{DSR(CL)}$	Drain-source clamping voltage (DC)	$I_{GD(CL)} = -2\text{ mA}$, $I_D = 1\text{ A}$		40		V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 16\text{ V}$ $V_{DS} = 16\text{ V}$, $T_j = 150\text{ }^{\circ}\text{C}$ $V_{DS} = 16\text{ V}$, $T_j = 175\text{ }^{\circ}\text{C}$			1 50 100	μA μA μA
$I_{GSS}^{(1)}$	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 10\text{ V}$ $V_{GS} = \pm 10\text{ V}$, $T_j = 175\text{ }^{\circ}\text{C}$ $V_{GS} = \pm 15\text{ V}$, $T_j = 175\text{ }^{\circ}\text{C}$			2 50 150	μA μA μA
V_{GSS}	Gate-source breakdown voltage	$I_{GS} = \pm 100\text{ }\mu\text{A}$	15			V
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 1\text{ mA}$	1		3	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 5\text{ V}$, $I_D = 30\text{ A}$ $V_{GS} = 10\text{ V}$, $I_D = 30\text{ A}$		9.5 7.5	12.5 10.5	$\text{m}\Omega$ $\text{m}\Omega$

1. Gate Oxide, without zener diodes, tested at wafer sorting ($I_{GSS} < \pm 100\text{ nA}$ @ $\pm 20\text{ V}$ $T_j=25^{\circ}$) (see [Figure 17](#)) for electrical schematics

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS}=15\text{ V}$, $I_D = 30\text{ A}$	-	50	-	S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS}=25\text{ V}$, $f=1\text{ MHz}$, $V_{GS}=0$	-	1800 625 220	-	pF pF pF
$t_{r(Voff)}$ t_f t_c	Off voltage rise time Fall time Cross-over time	$V_{CLAMP}=32\text{ V}$, $I_D=60\text{ A}$, $V_{GS}=10\text{ V}$, $R_G=4.7\text{ }\Omega$ (see Figure 16)	-	70 95 185	-	ns ns ns
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD}=32\text{ V}$, $I_D = 60\text{ A}$ $V_{GS}=5\text{ V}$ (see Figure 15)	-	32 12 17	-	nC nC nC

1. Pulsed: pulse duration=300 μs , duty cycle 1.5%

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM}^{(1)}$	Source-drain current Source-drain current (pulsed)		-		70 280	A A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=60\text{ A}$, $V_{GS}=0$	-		1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=60\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD}=25\text{ V}$, $T_j=150\text{ }^{\circ}\text{C}$ (see Figure 16)	-	40 40 2.3		ns nC A

1. Pulse width limited by safe operating area

2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

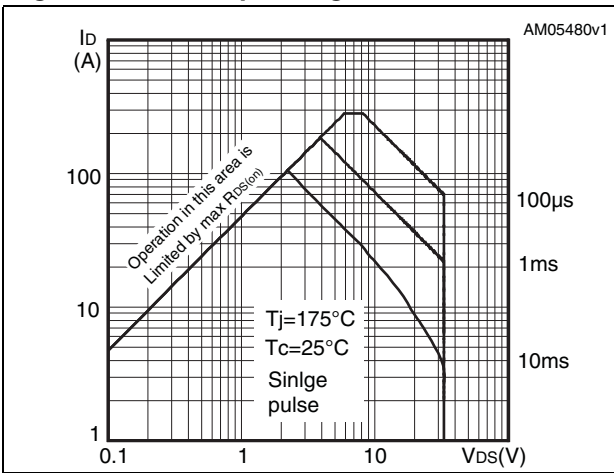


Figure 3. Thermal impedance

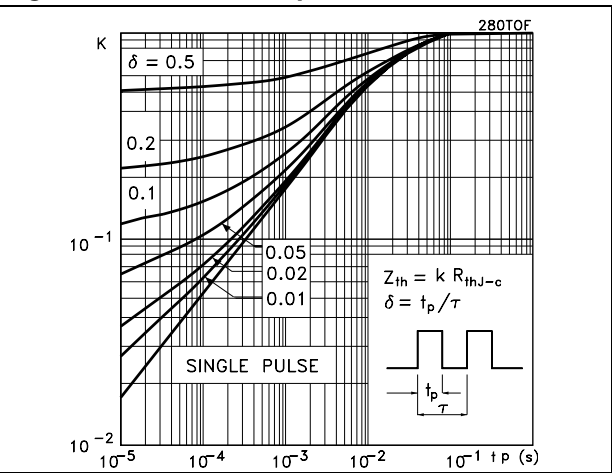


Figure 4. Output characteristics

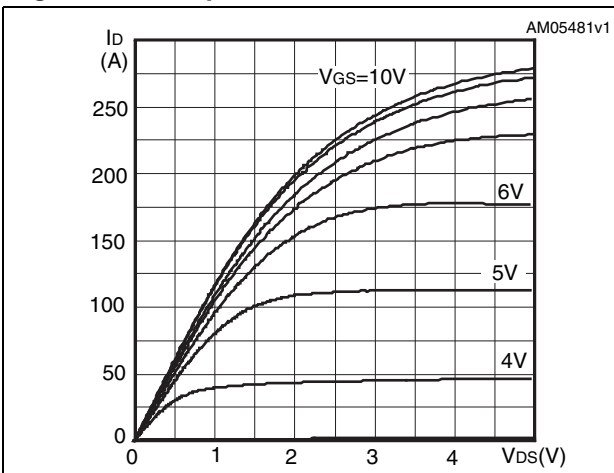


Figure 5. Transfer characteristics

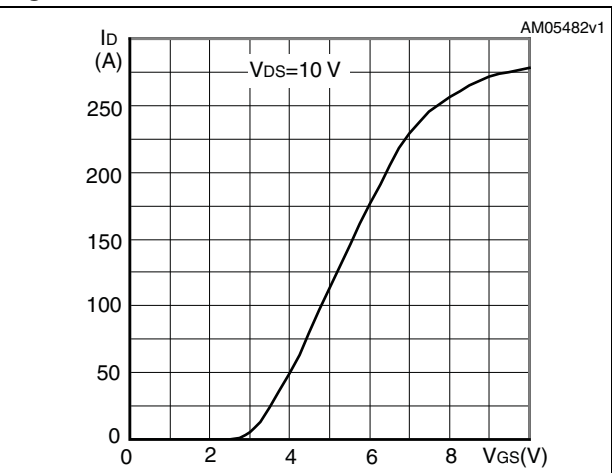


Figure 6. Normalized BVDS vs temperature

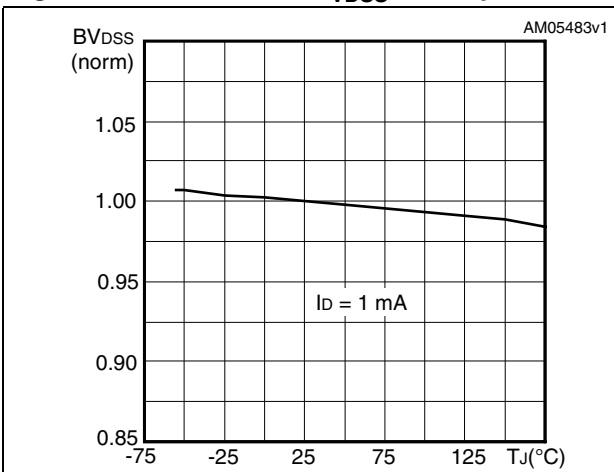


Figure 7. Static drain-source on resistance

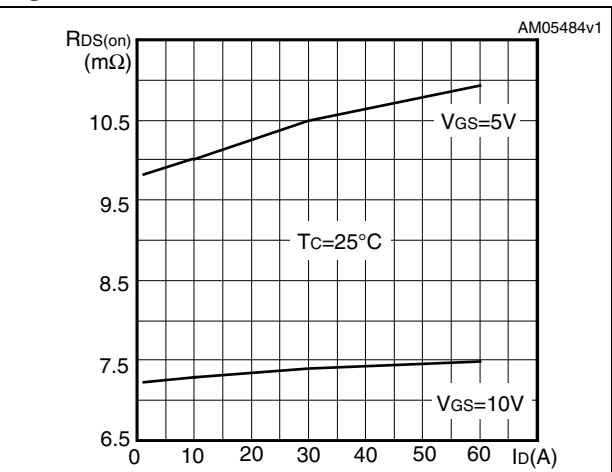


Figure 8. Gate charge vs gate-source voltage

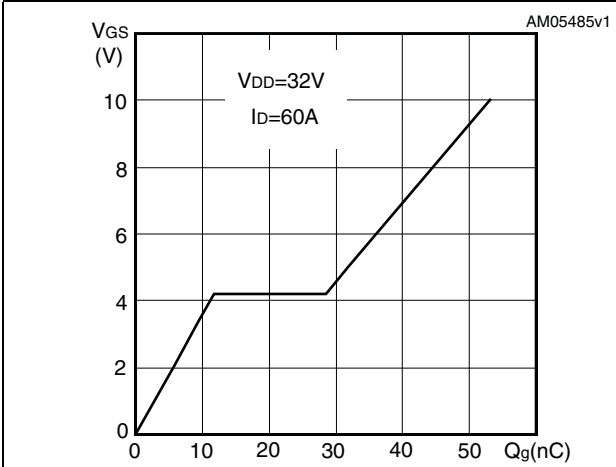


Figure 9. Capacitance variations

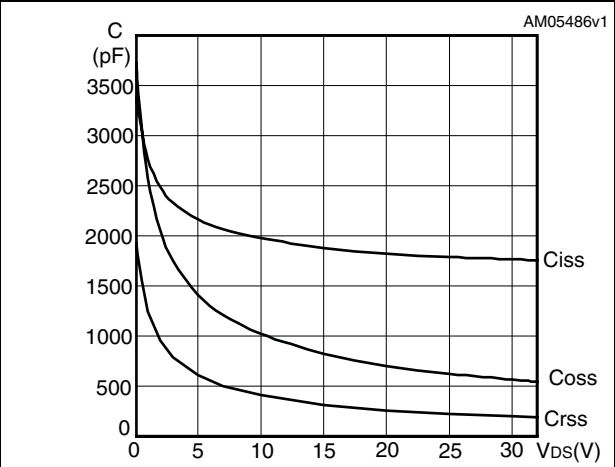


Figure 10. Normalized gate threshold voltage vs temperature

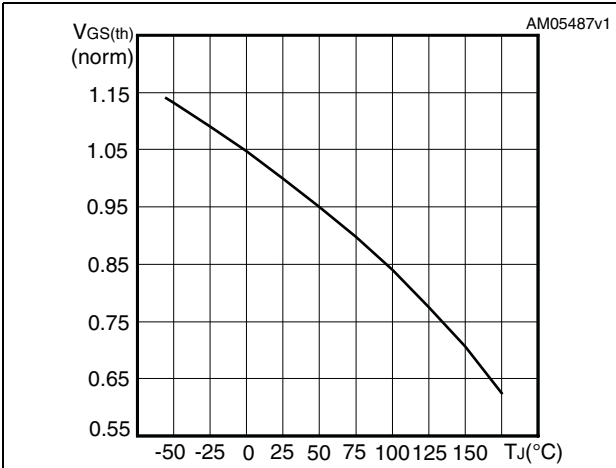


Figure 11. Normalized on resistance vs temperature

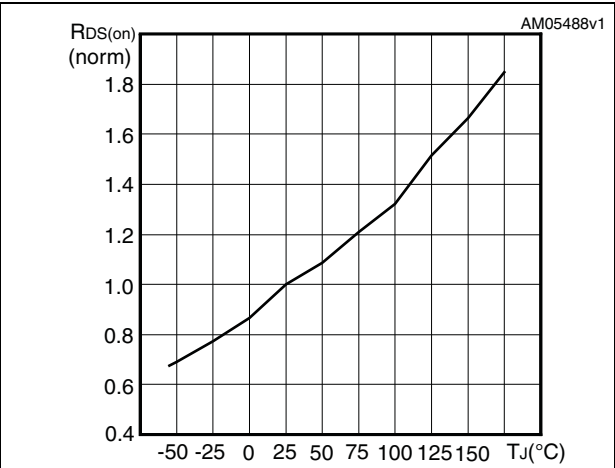
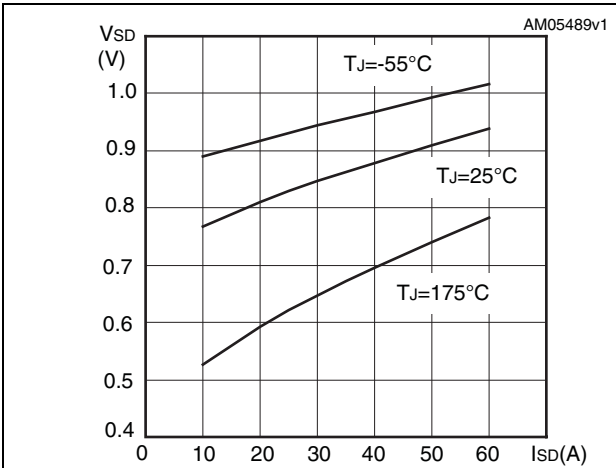


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

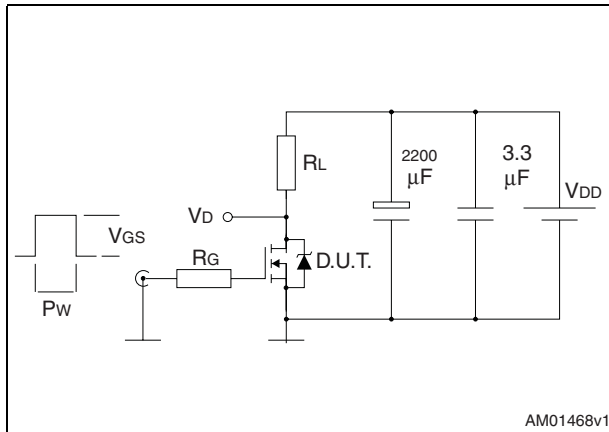


Figure 14. Gate charge test circuit

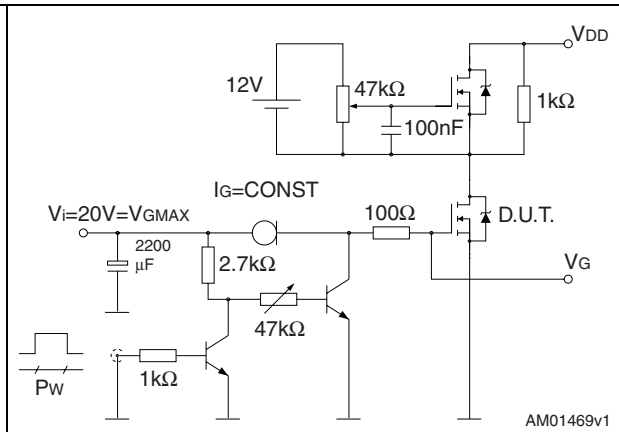


Figure 15. Test circuit for inductive load switching and diode recovery times

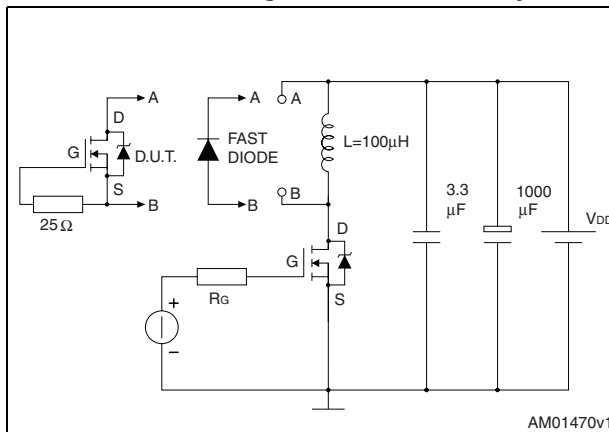


Figure 16. Unclamped inductive load test circuit

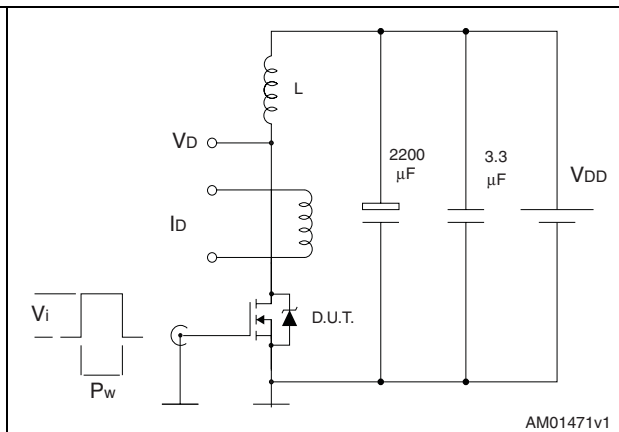


Figure 17. Unclamped inductive waveform

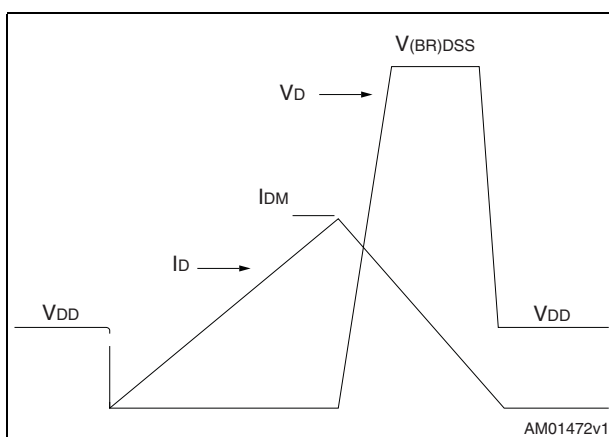
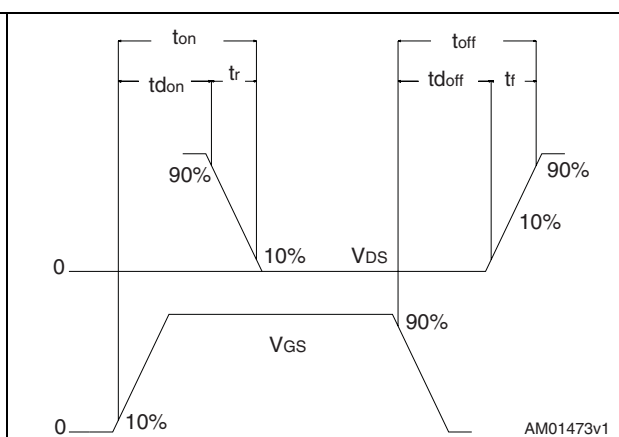


Figure 18. Switching time waveform

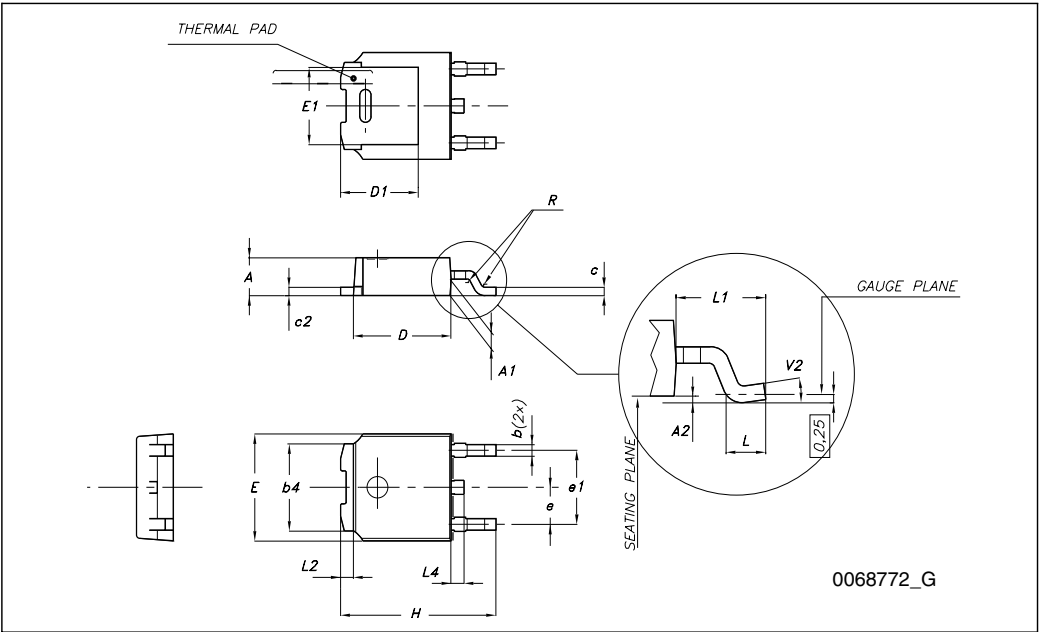


4 Package mechanical data

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TO-252 (DPAK) mechanical data

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0 °		8 °



6 Revision history

Table 8. Document revision history

Date	Revision	Changes
01-Oct-2009	1	First release

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