



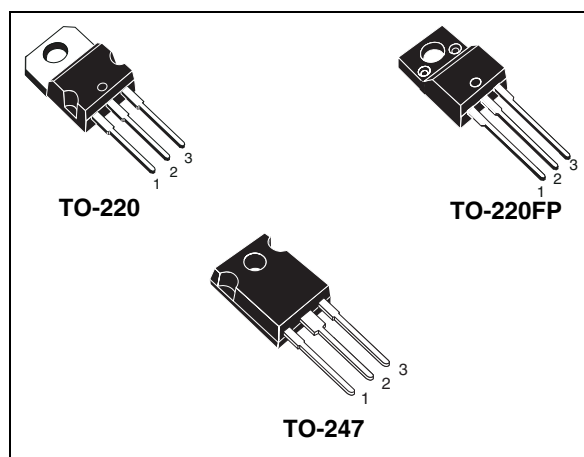
STF13N95K3 STP13N95K3, STW13N95K3

N-channel 950 V, 0.68 Ω , 10 A TO-220, TO-220FP, TO-247
Zener-protected SuperMESH3™ Power MOSFET

Features

Order codes	V _{DSS}	R _{DS(on)} max	I _D	P _W
STF13N95K3	950 V	< 0.85 Ω	10 A	40 W
STP13N95K3				190 W
STW13N95K3				

- Gate charge minimized
- Extremely large avalanche performance
- 100% avalanche tested
- Very low intrinsic capacitance
- Zener-protected



Application

Switching applications

Description

These devices are made using the SuperMESH3™ Power MOSFET technology that is obtained via improvements applied to STMicroelectronics' SuperMESH™ technology combined with a new optimized vertical structure. The resulting product has an extremely low on resistance, superior dynamic performance and high avalanche capability, making it especially suitable for the most demanding applications.

Figure 1. Internal schematic diagram

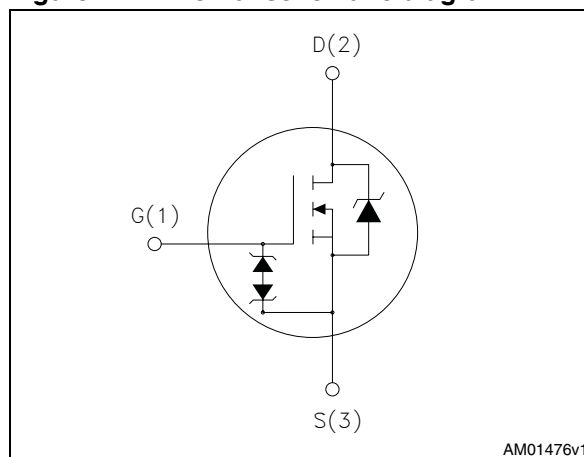


Table 1. Device summary

Order codes	Marking	Package	Packaging
STF13N95K3	13N95K3	TO-220FP	Tube
STP13N95K3		TO-220	
STW13N95K3		TO-247	

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220, TO-247	TO-220FP	
V_{DS}	Drain source voltage	950		V
V_{GS}	Gate- source voltage	± 30		V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	10	10 ⁽¹⁾	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	6	6 ⁽¹⁾	A
I_{DM} ⁽²⁾	Drain current (pulsed)	40	40 ⁽¹⁾	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	190	40	W
I_{AR}	Max current during repetitive or single pulse avalanche (pulse width limited by T_{jmax})	13		A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AS}$, $V_{DD} = 50\text{ V}$)	400		mJ
dv/dt ⁽³⁾	Peak diode recovery voltage slope	9		V/ns
T_j T_{stg}	Operating junction temperature Storage temperature	- 55 to 150		$^{\circ}\text{C}$

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area.
3. $I_{SD} \leq 10\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{Peak} \leq V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value			Unit
		TO-220	TO-247	TO-220FP	
$R_{thj-case}$	Thermal resistance junction-case max	0.66		3.13	$^{\circ}\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-amb max	62.5	50	62.5	$^{\circ}\text{C}/\text{W}$
T_l	Maximum lead temperature for soldering purpose	300			$^{\circ}\text{C}$

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	950			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{max rating}$, $V_{DS} = \text{max rating}$, $T_c = 125\text{ °C}$			1 50	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 100\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$, $I_D = 5\text{ A}$		0.68	0.85	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	1620	-	pF
C_{oss}	Output capacitance			117		pF
C_{rss}	Reverse transfer capacitance			1.2		pF
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{GS} = 0$, $V_{DS} = 0\text{ to }760\text{ V}$	-	115	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related		-	131	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	2.3	-	Ω
Q_g	Total gate charge	$V_{DD} = 760\text{ V}$, $I_D = 10\text{ A}$	-	51	-	nC
Q_{gs}	Gate-source charge	$V_{GS} = 10\text{ V}$		10		nC
Q_{gd}	Gate-drain charge	(see Figure 20)		30		nC

1. Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
2. energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 475\text{ V}$, $I_D = 5\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 22)	-	18	-	ns
t_r	Rise time			16		ns
$t_{d(off)}$	Turn-off delay time			50		ns
t_f	Fall time			21		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		10	mA
I_{SDM}	Source-drain current (pulsed)				40	A
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 10\text{ A}$, $V_{GS} = 0$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 10\text{ A}$, $V_{DD} = 60\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$, (see Figure 21)	-	500		ns
Q_{rr}	Reverse recovery charge			9		μC
I_{RRM}	Reverse recovery current			36		A
t_{rr}	Reverse recovery time	$I_{SD} = 10\text{ A}$, $V_{DD} = 60\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$, $T_J = 150\text{ }^\circ\text{C}$ (see Figure 21)	-	624		ns
Q_{rr}	Reverse recovery charge			11		μC
I_{RRM}	Reverse recovery current			37		A

1. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
BV_{GSO}	Gate-source breakdown voltage	$I_{gs} \pm 1\text{ mA}$, (open drain)	30	-		V

The built-in-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220FP

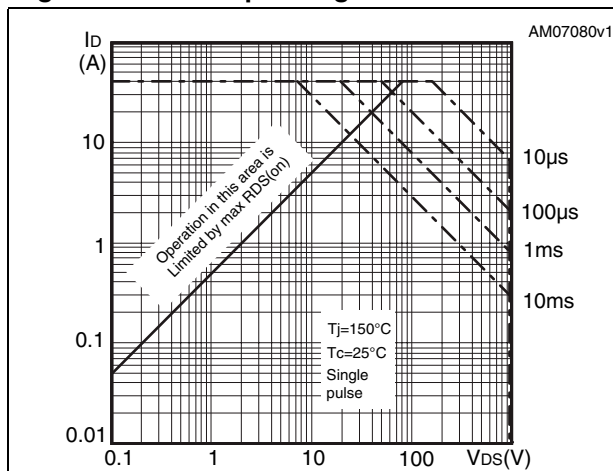


Figure 3. Thermal impedance for TO-220FP

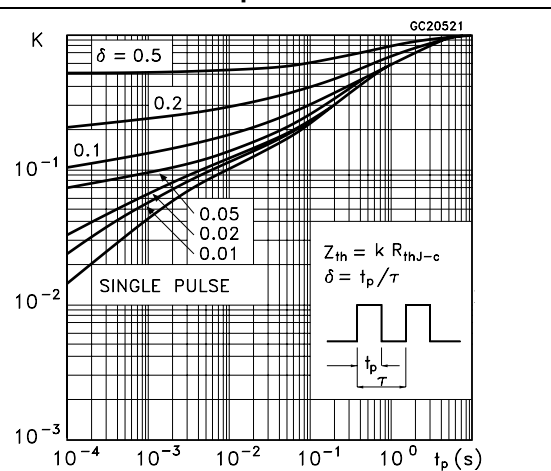


Figure 4. Safe operating area for TO-220

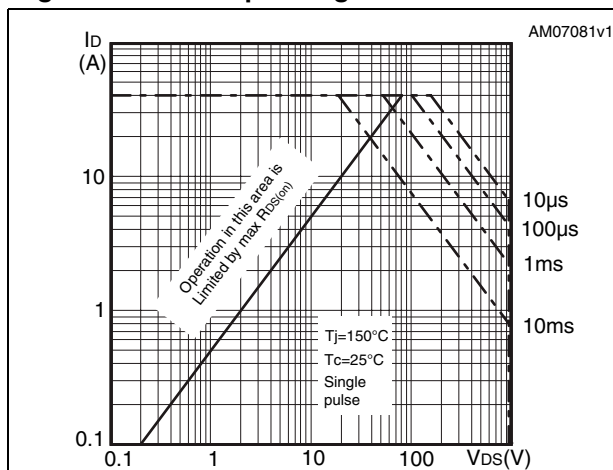


Figure 5. Thermal impedance for TO-220

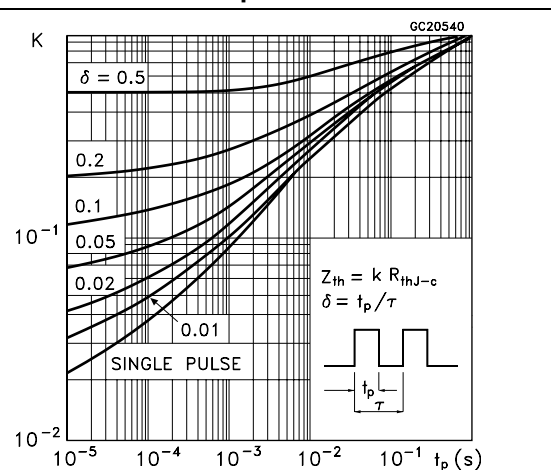


Figure 6. Safe operating area for TO-247

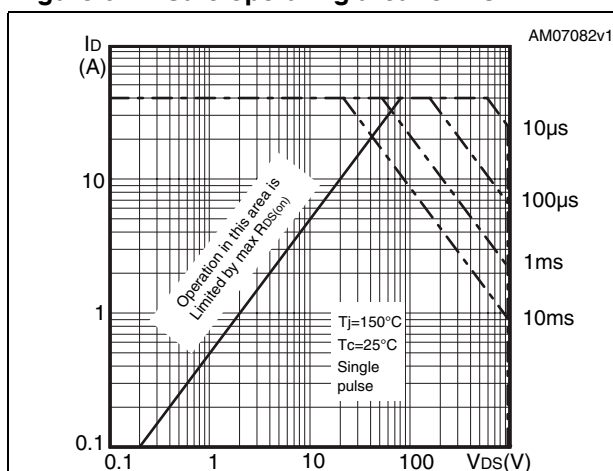


Figure 7. Thermal impedance for TO-247

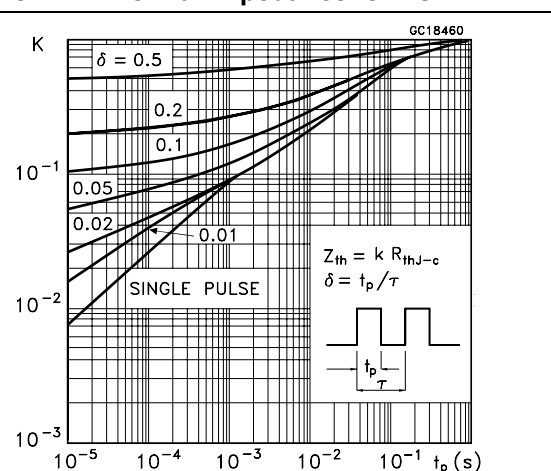


Figure 8. Output characteristics

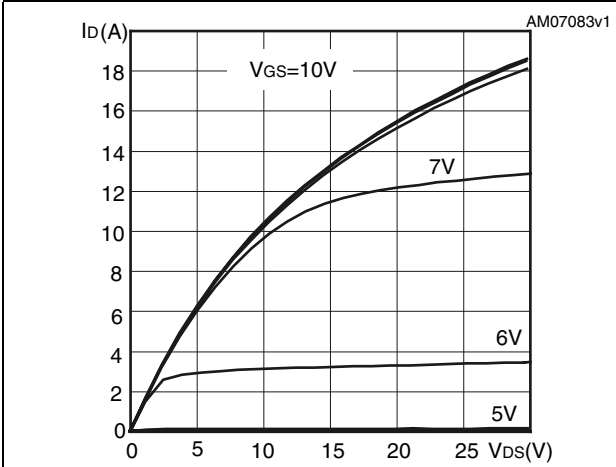


Figure 9. Transfer characteristics

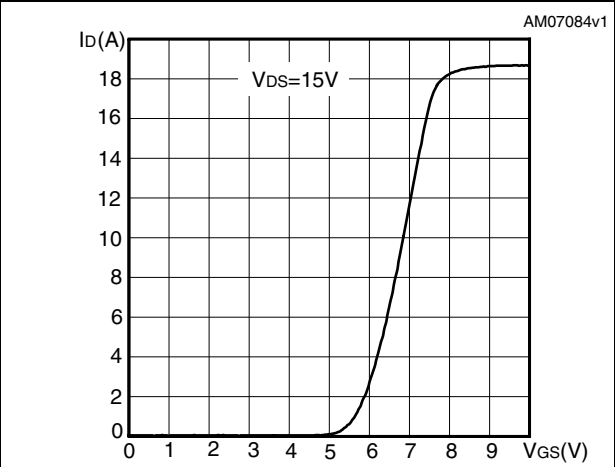


Figure 10. Gate charge vs gate-source voltage

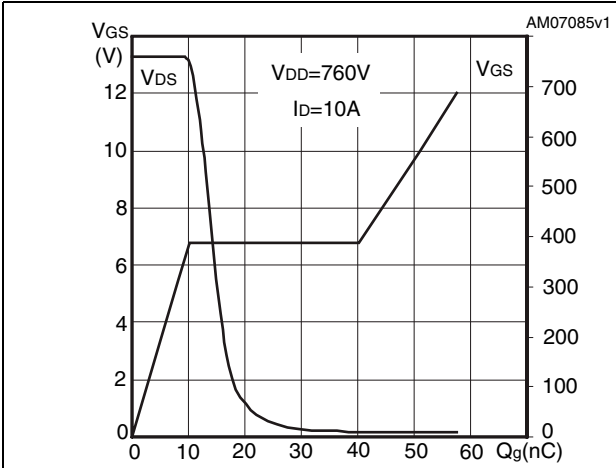


Figure 11. Static drain-source on resistance

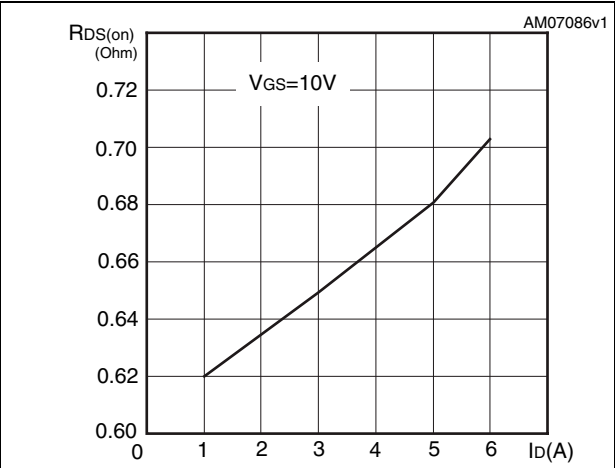


Figure 12. Capacitance variations

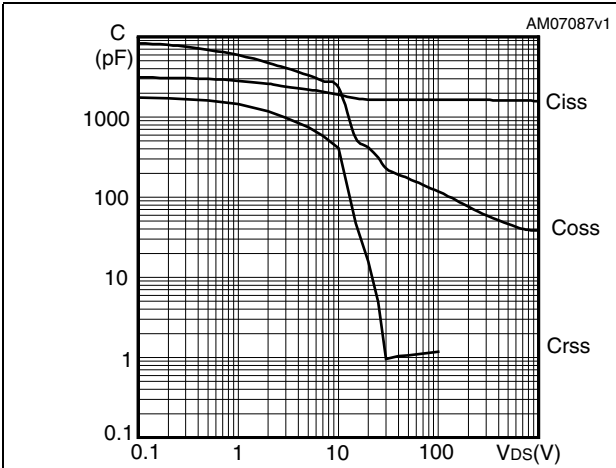


Figure 13. Output capacitance stored energy

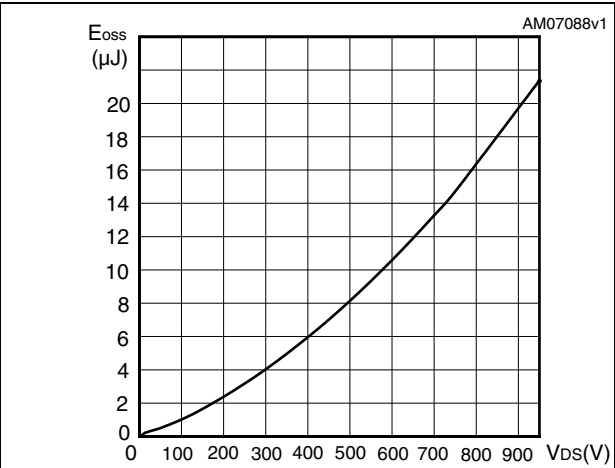


Figure 14. Normalized gate threshold voltage vs temperature

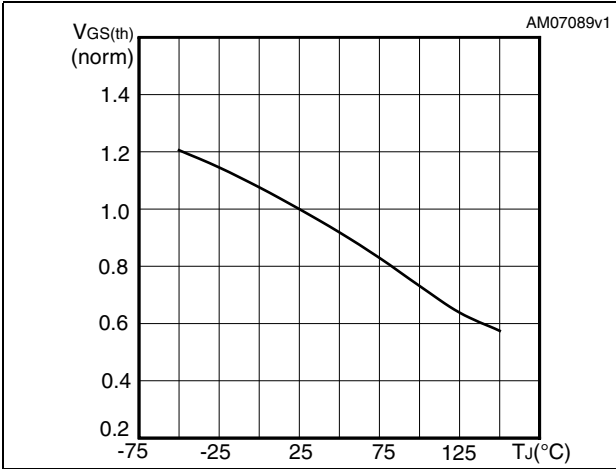


Figure 15. Normalized on resistance vs temperature

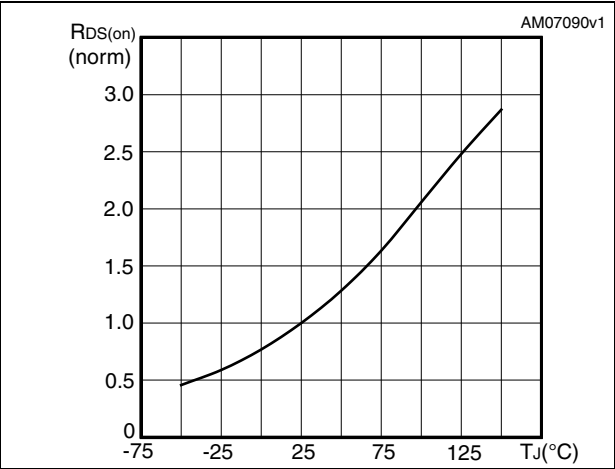


Figure 16. Source-drain diode forward characteristics

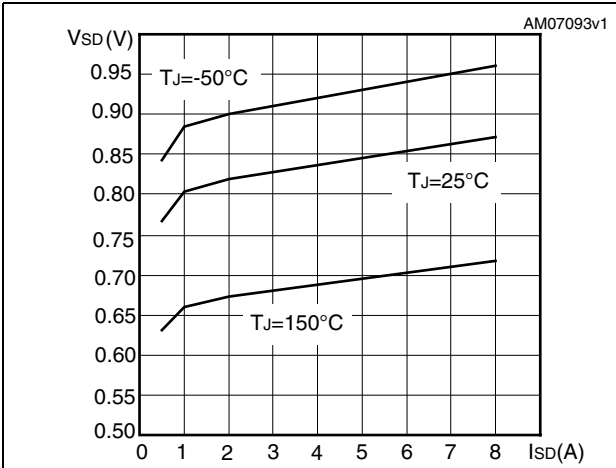


Figure 17. Normalized B_{VDSS} vs temperature

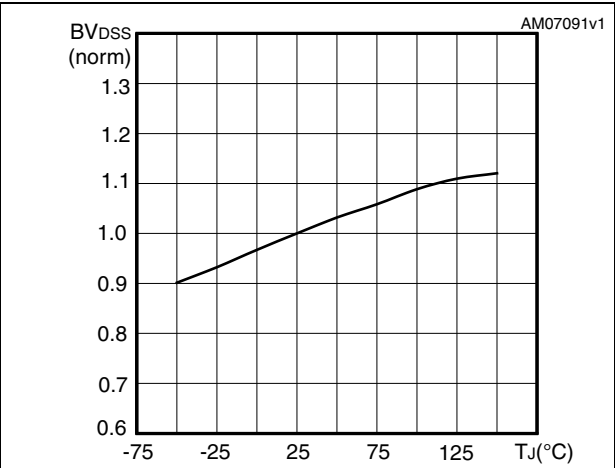
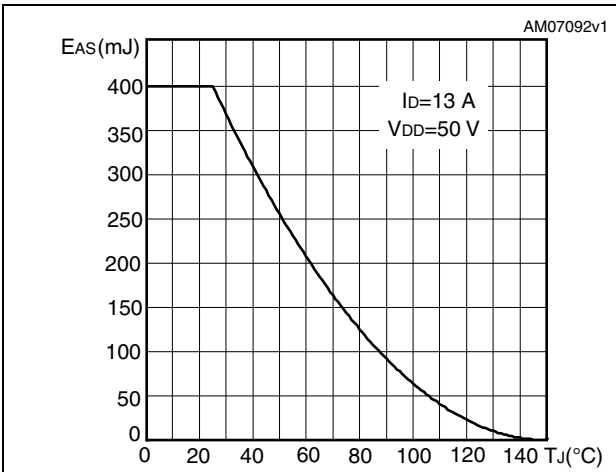


Figure 18. Maximum avalanche energy vs starting T_J



3 Test circuits

Figure 19. Switching times test circuit for resistive load

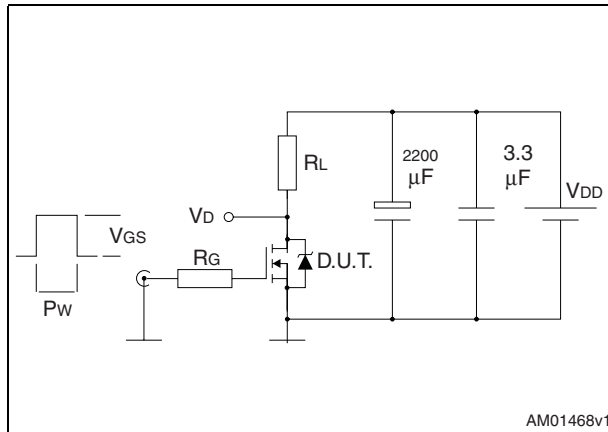


Figure 20. Gate charge test circuit

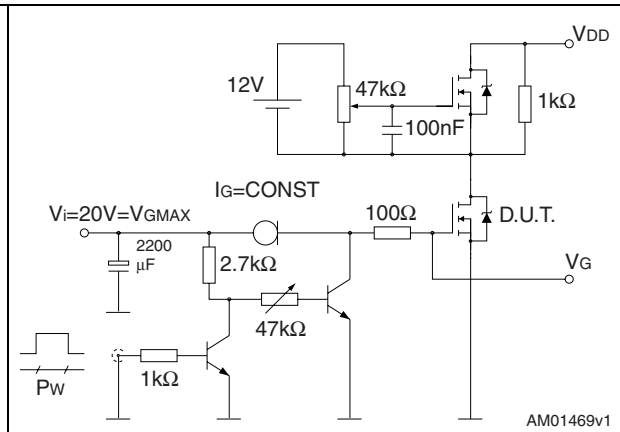


Figure 21. Test circuit for inductive load switching and diode recovery times

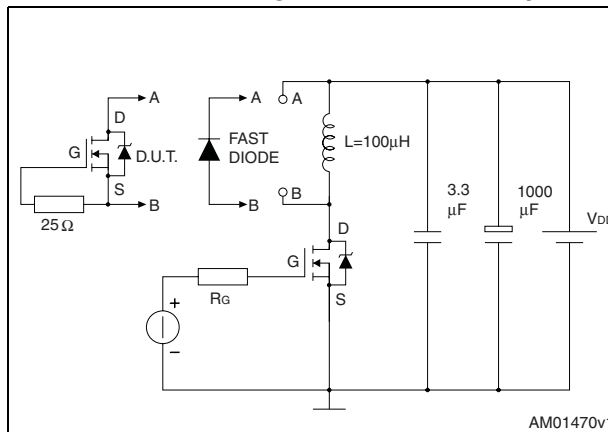


Figure 22. Unclamped inductive load test circuit

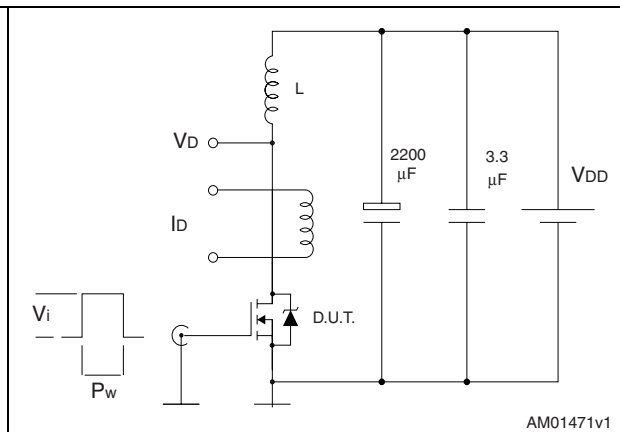


Figure 23. Unclamped inductive waveform

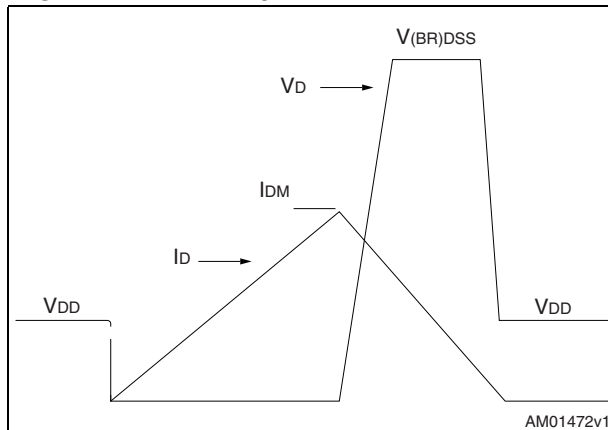
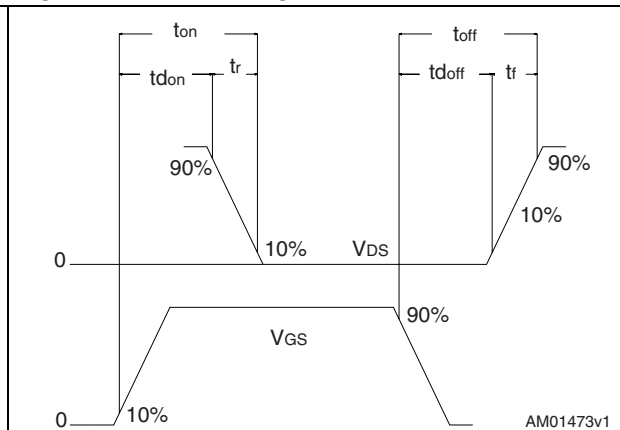


Figure 24. Switching time waveform



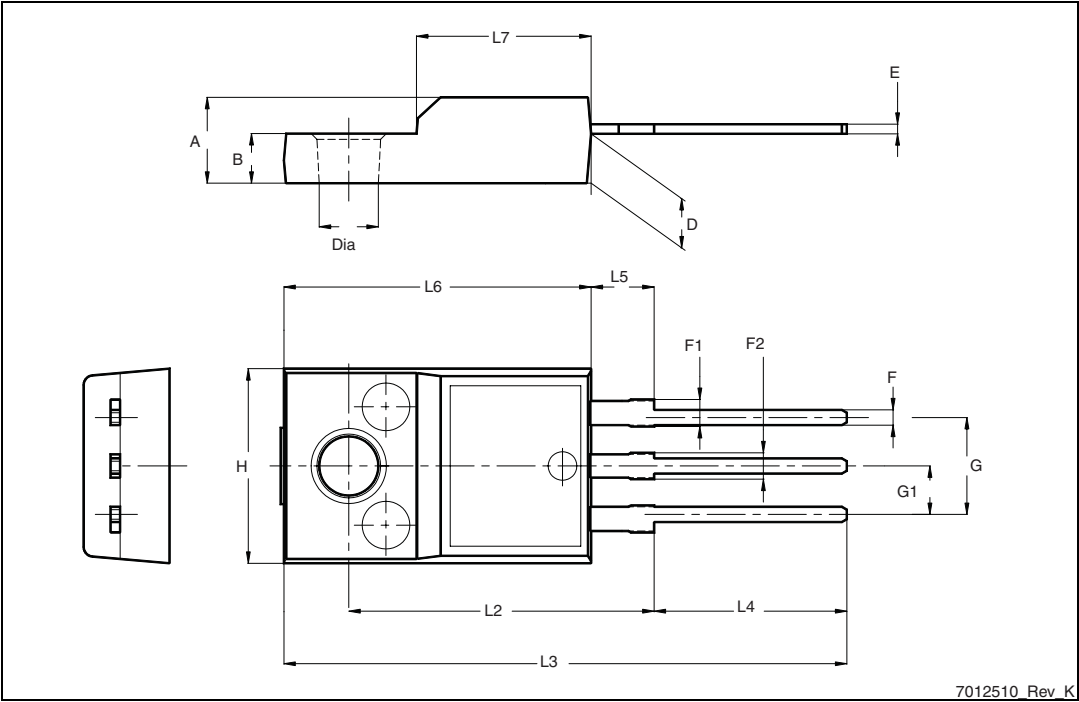
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Table 9. TO-220FP mechanical data

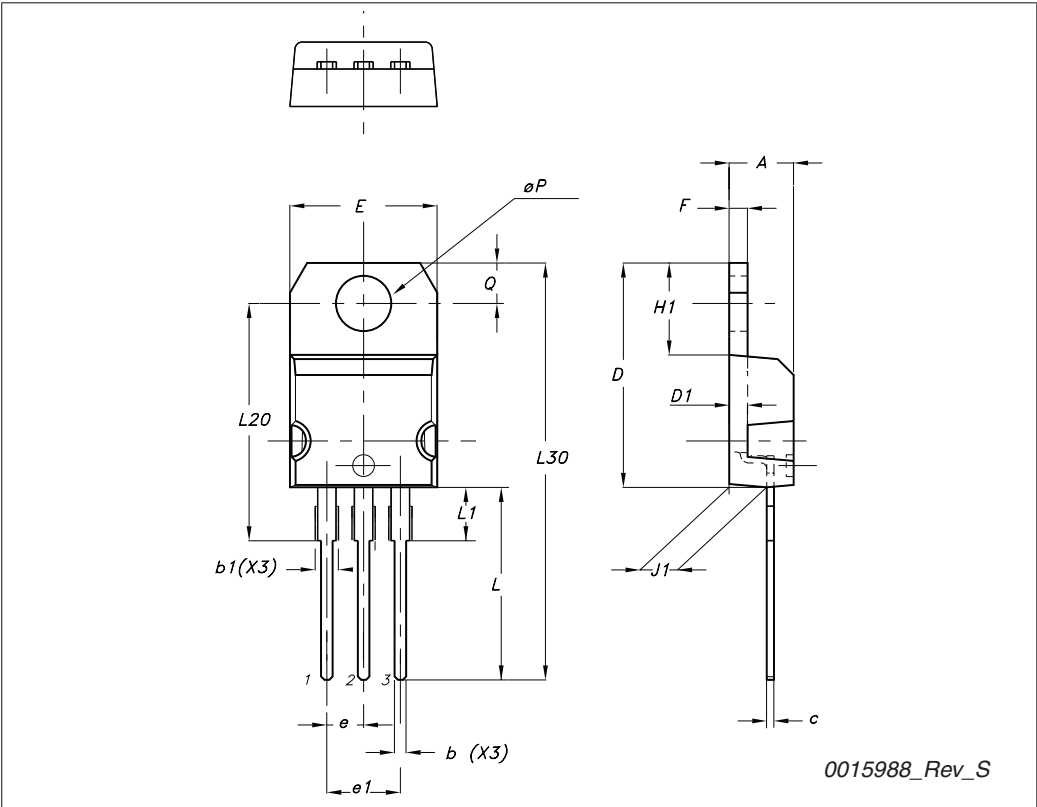
Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

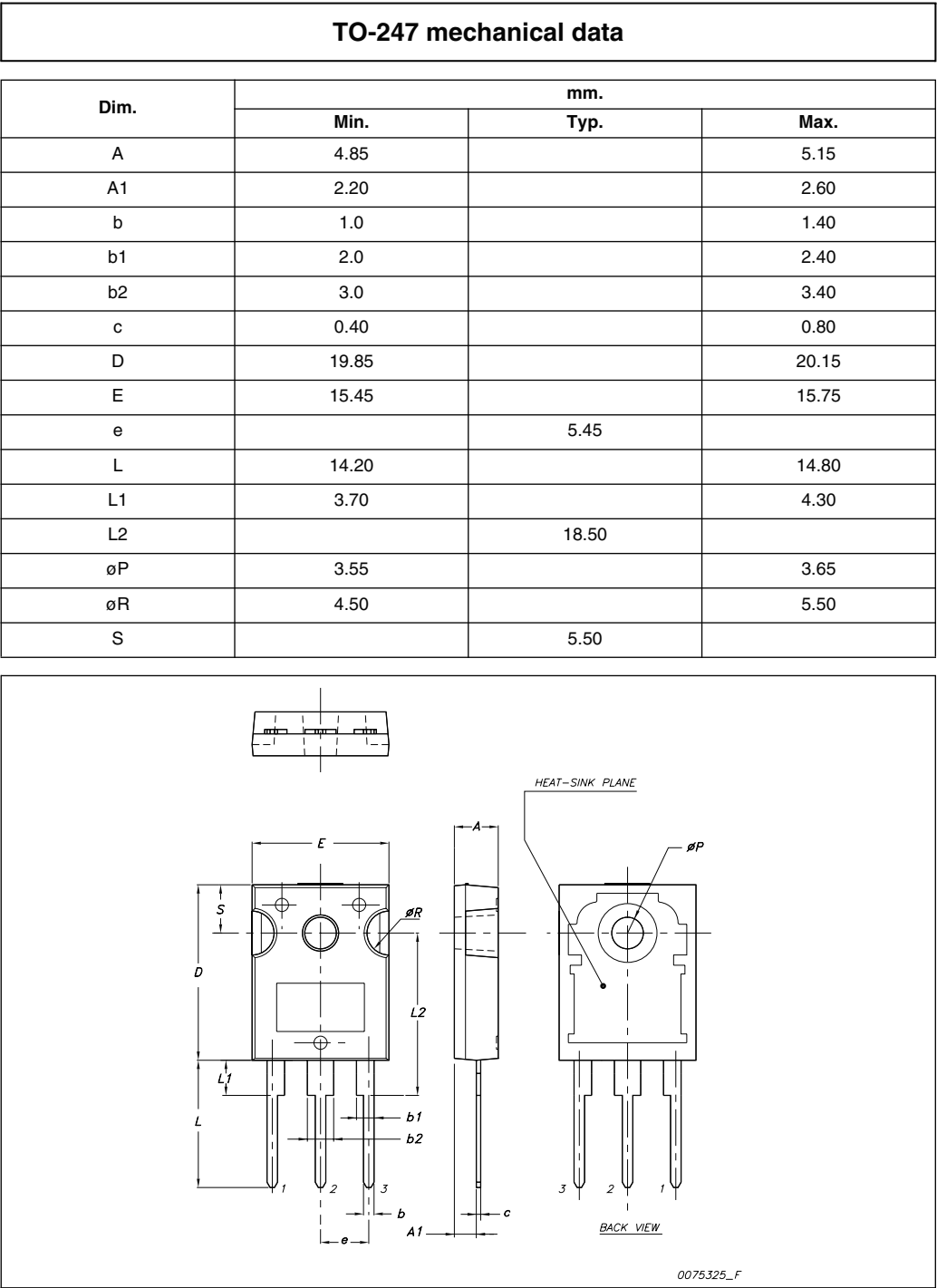
Figure 25. TO-220FP drawing



TO-220 type A mechanical data

Dim	mm		
	Min	Typ	Max
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95





5 Revision history

Table 10. Document revision history

Date	Revision	Changes
15-May-2009	1	First release.
02-Sep-2010	2	Document status promoted from preliminary data to datasheet.

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