



# STW45N65M5, STWA45N65M5

N-channel 650 V, 0.067  $\Omega$  typ., 35 A MDmesh™ V Power MOSFET  
in TO-247 and TO-247 long leads packages

Datasheet — production data

## Features

Order code	V <sub>DSS</sub> @ T <sub>Jmax</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
STW45N65M5	710 V	< 0.078 $\Omega$	35 A
STWA45N65M5			

- Worldwide best R<sub>DS(on)</sub> \* area
- Higher V<sub>DSS</sub> rating and high dv/dt capability
- Excellent switching performance
- 100% avalanche tested

## Applications

- Switching applications

## Description

These devices are N-channel MDmesh™ V Power MOSFETs based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

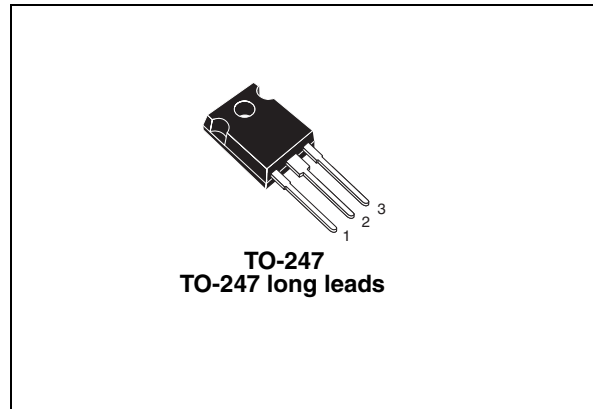


Figure 1. Internal schematic diagram

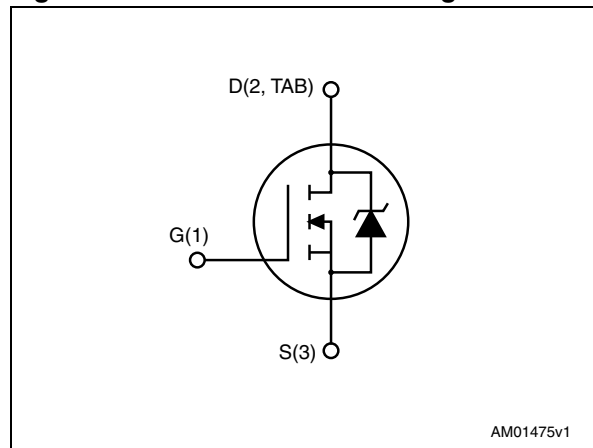


Table 1. Device summary

Order code	Marking	Package	Packaging
STW45N65M5	45N65M5	TO-247	Tube
STWA45N65M5		TO-247 long leads	

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	35	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	22	A
$I_{DM}^{(1)}$	Drain current (pulsed)	140	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	210	W
$dv/dt^{(1)}$	Peak diode recovery voltage slope	15	V/ns
$T_{stg}$	Storage temperature	- 55 to 150	$^\circ\text{C}$
$T_j$	Max. operating junction temperature	150	$^\circ\text{C}$

1.  $I_{SD} \leq 35\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{DS(Peak)} < V_{(BR)DSS}$ ,  $V_{DD} = 400\text{ V}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.60	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	50	$^\circ\text{C}/\text{W}$

**Table 4. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not repetitive (pulse width limited by $T_{jmax}$ )	9	A
$E_{AS}$	Single pulse avalanche energy (starting $t_j=25\text{ }^\circ\text{C}$ , $I_d=I_{AR}$ ; $V_{dd}=50$ )	810	mJ

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 5. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$ , $V_{GS} = 0$	650			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 650\text{ V}$ $V_{DS} = 650\text{ V}$ , $T_C = 125\text{ °C}$			1 100	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 25\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 17.5\text{ A}$		0.067	0.078	$\Omega$

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$	-	3470 82 7	-	pF pF pF
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{DS} = 0\text{ to }520\text{ V}$ , $V_{GS} = 0$	-	280	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related		-	79	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	2	-	$\Omega$
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 520\text{ V}$ , $I_D = 17.5\text{ A}$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 16</a> )	-	82 18.5 35	-	nC nC nC

1. Time related is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$
2. Energy related is defined as a constant equivalent capacitance giving the same stored energy as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 7. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_d$ (v)	Voltage delay time	$V_{DD} = 400$ V, $I_D = 23$ A,		79.5		ns
$t_r$ (v)	Voltage rise time	$R_G = 4.7$ $\Omega$ , $V_{GS} = 10$ V		11		ns
$t_f$ (i)	Current fall time	(see <a href="#">Figure 17</a> and	-	9.3	-	ns
$t_c$ (off)	Crossing time	<a href="#">Figure 20</a> )		16		ns

**Table 8. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current				35	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		140	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 35$ A, $V_{GS} = 0$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 35$ A, $di/dt = 100$ A/ $\mu$ s		392		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 100$ V (see <a href="#">Figure 17</a> )	-	7.4		$\mu$ C
$I_{RRM}$	Reverse recovery current			38		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 35$ A, $di/dt = 100$ A/ $\mu$ s		468		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 100$ V, $T_j = 150$ °C	-	9.7		$\mu$ C
$I_{RRM}$	Reverse recovery current	(see <a href="#">Figure 17</a> )		42		A

1. Pulse width limited by safe operating area.

2. Pulsed: pulse duration = 300  $\mu$ s, duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

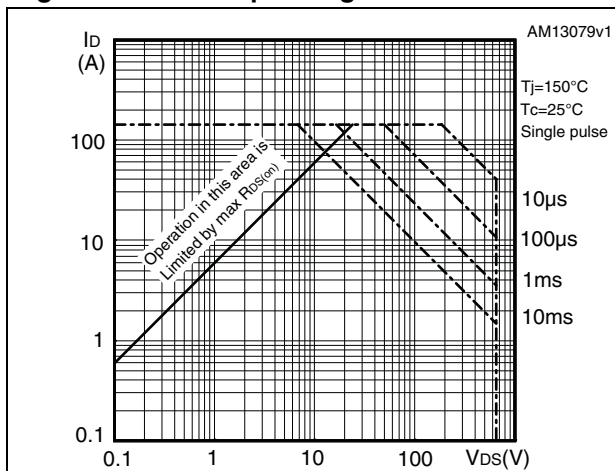


Figure 3. Thermal impedance

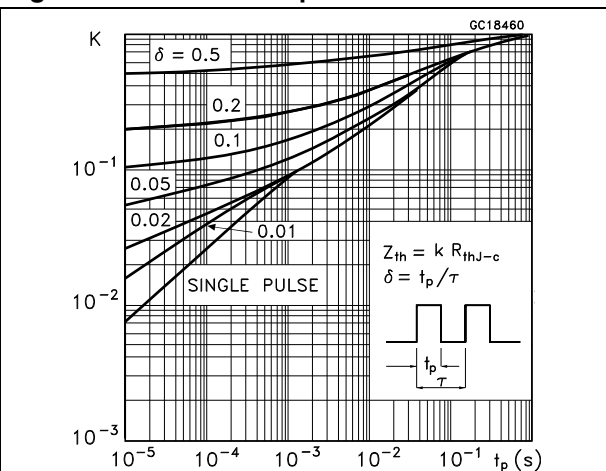


Figure 4. Output characteristics

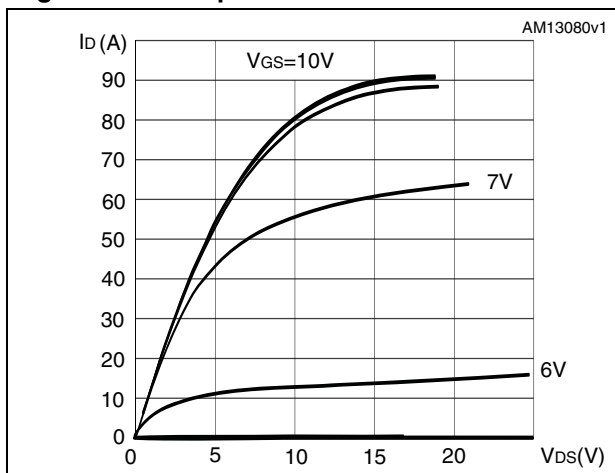


Figure 5. Transfer characteristics

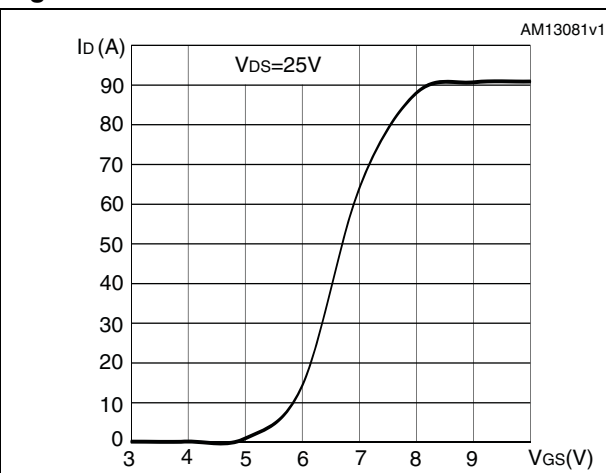


Figure 6. Gate charge vs gate-source voltage

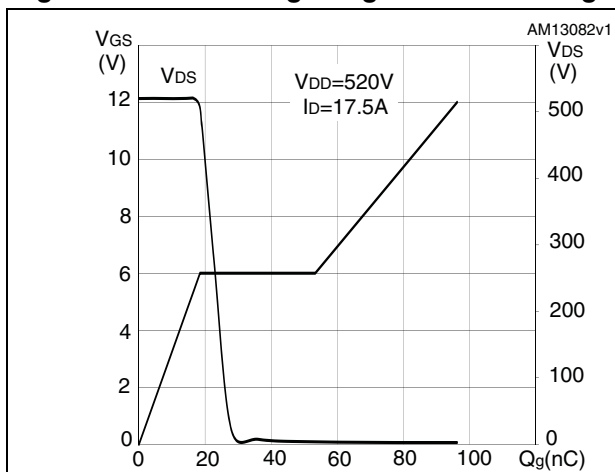


Figure 7. Static drain-source on-resistance

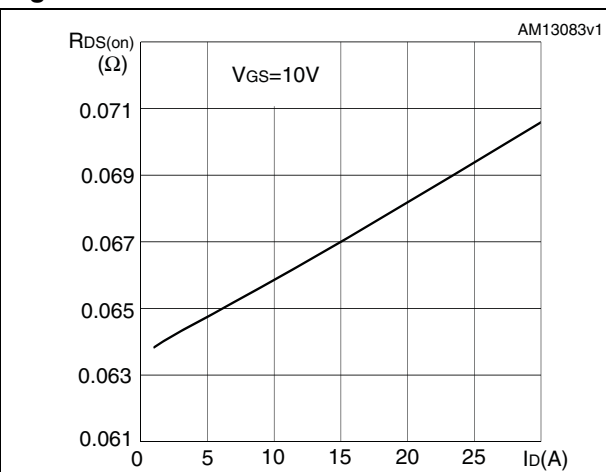


Figure 8. Capacitance variations

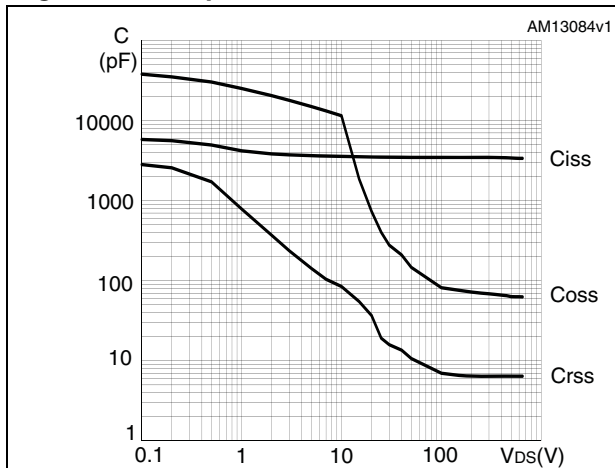


Figure 9. Output capacitance stored energy

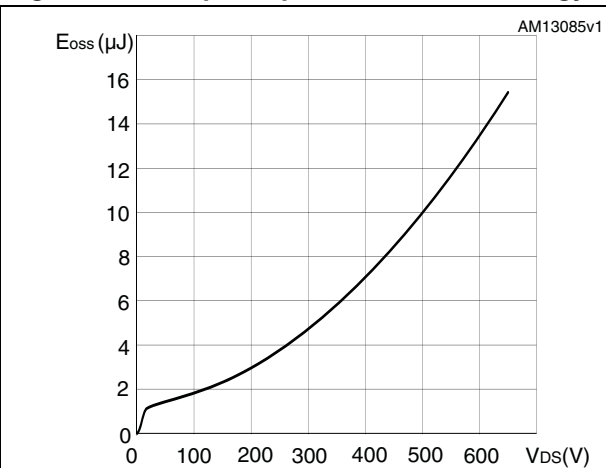


Figure 10. Normalized gate threshold voltage vs. temperature

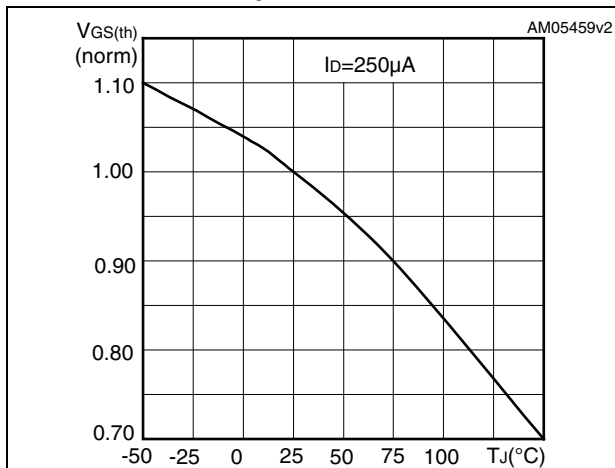


Figure 11. Normalized on resistance vs. temperature

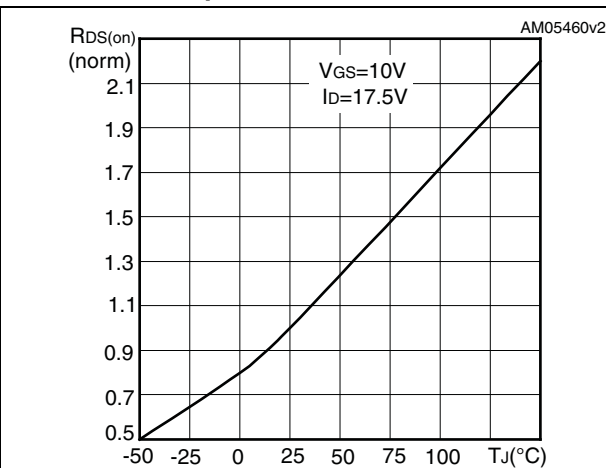


Figure 12. Drain-source diode forward characteristics

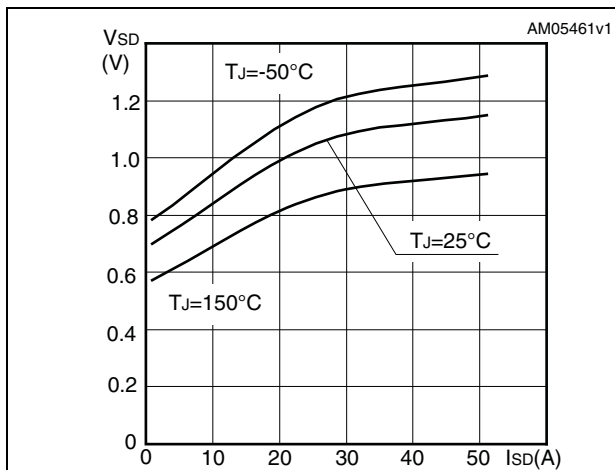


Figure 13. Normalized VDS vs. temperature

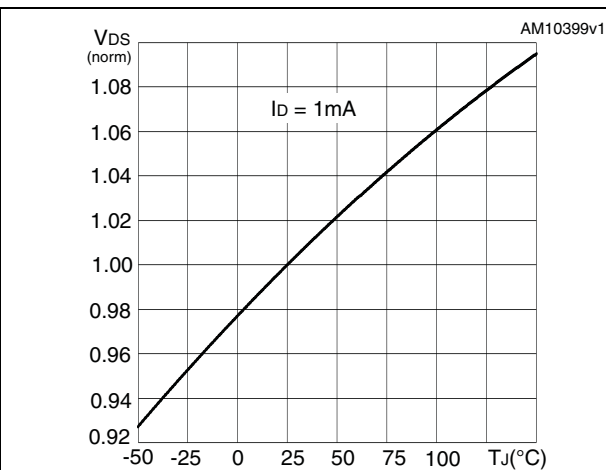
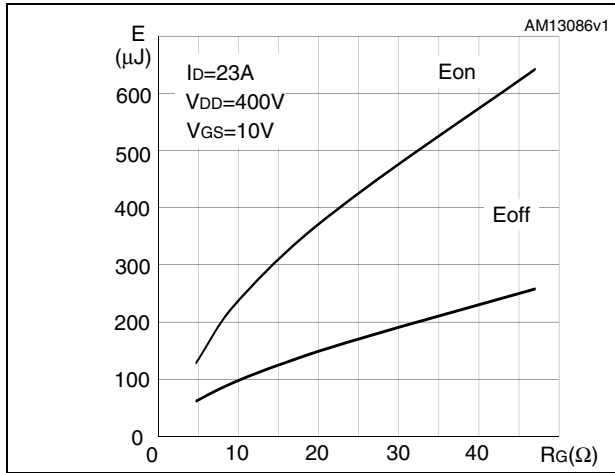


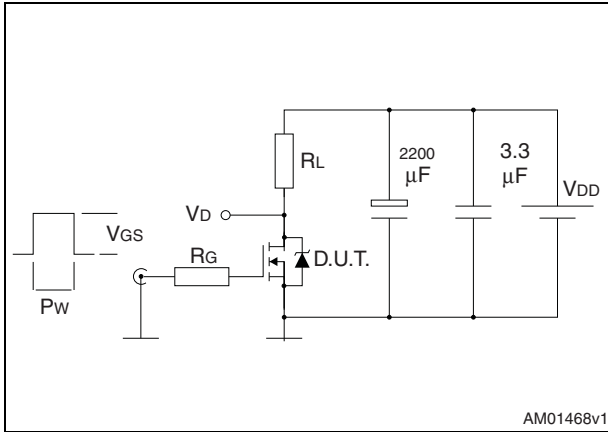
Figure 14. Switching losses vs. gate resistance (1)



1.  $E_{on}$  including reverse recovery of a SiC diode

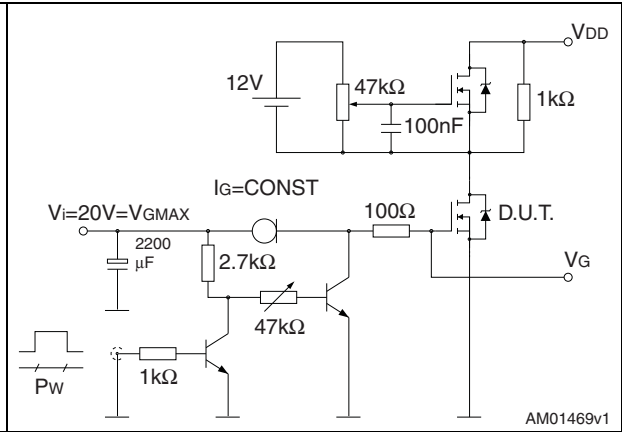
### 3 Test circuits

**Figure 15. Switching times test circuit for resistive load**



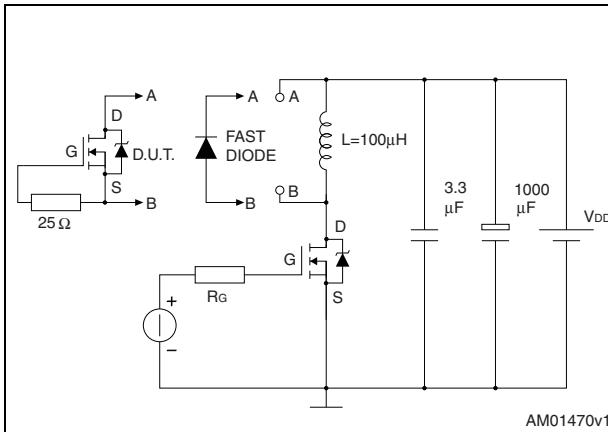
AM01468v1

**Figure 16. Gate charge test circuit**



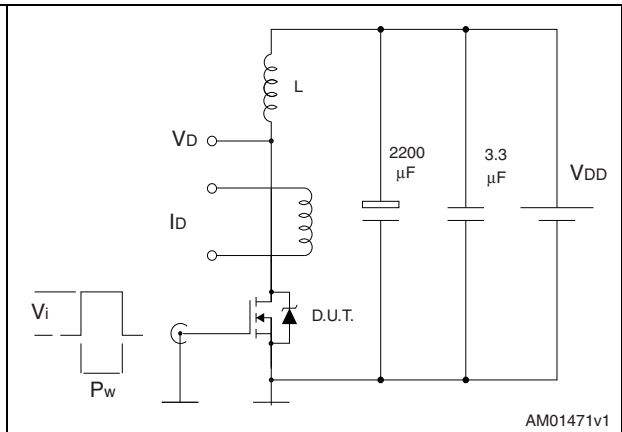
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**Figure 17. Test circuit for inductive load switching and diode recovery times**



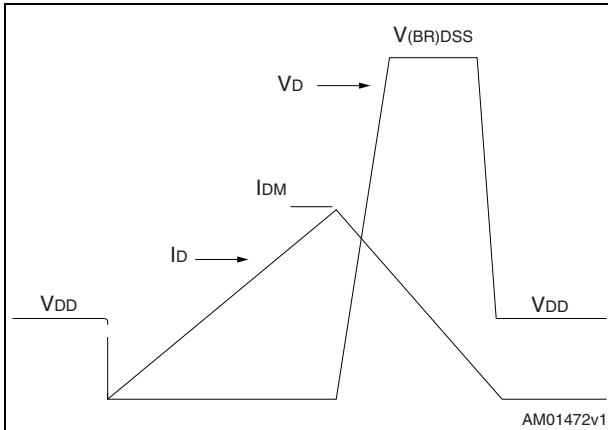
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**Figure 18. Unclamped inductive load test circuit**



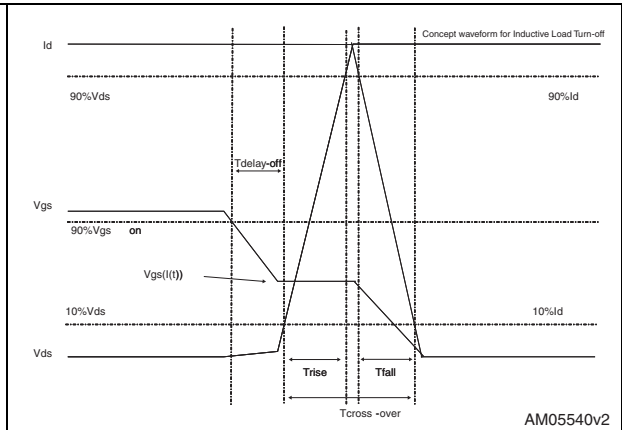
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**Figure 19. Unclamped inductive waveform**



AM01472v1

**Figure 20. Switching time waveform**



AM05540v2

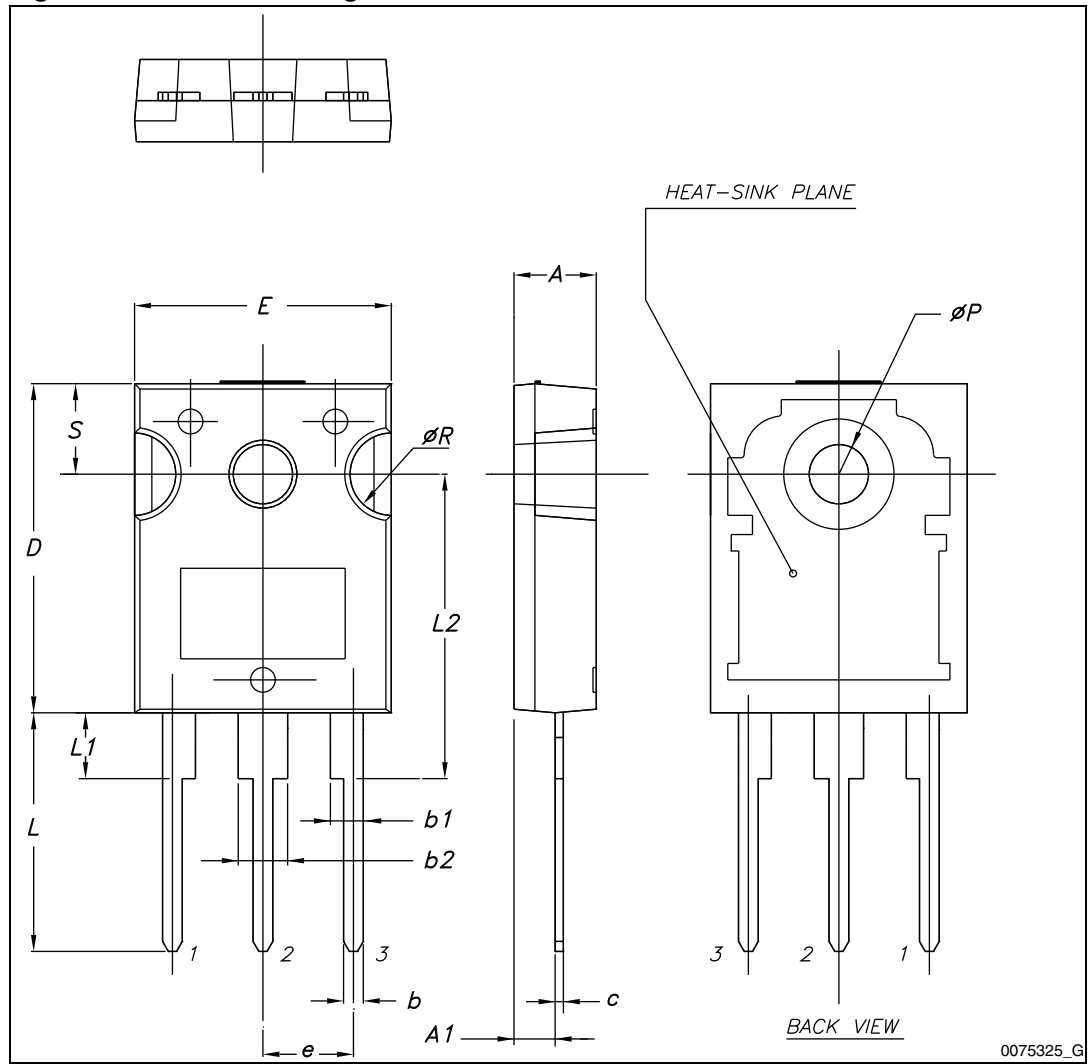
## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

Table 9. TO-247 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

Figure 21. TO-247 drawing

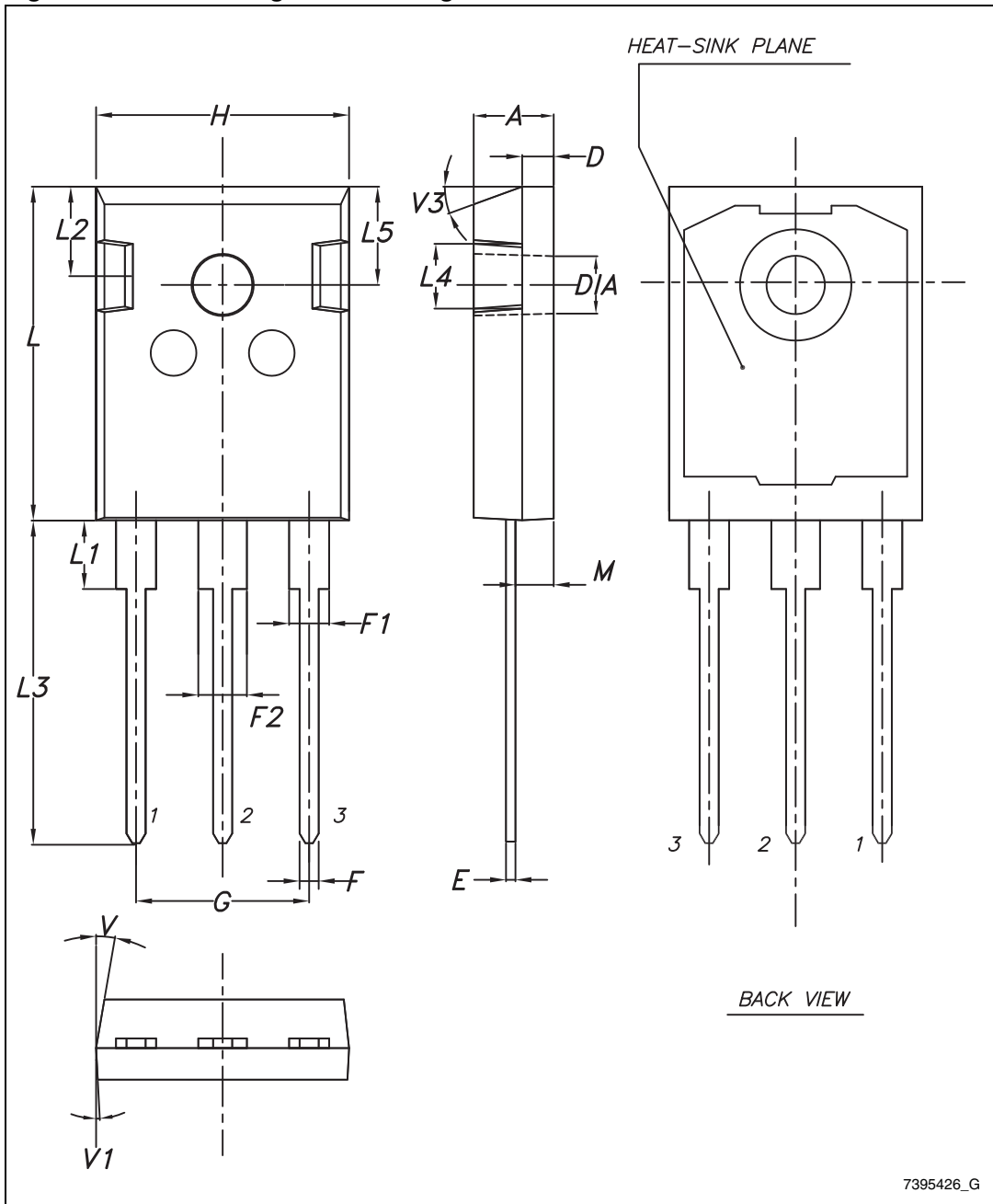


0075325\_G

Table 10. TO-247 long leads mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.90		5.15
D	1.85		2.10
E	0.55		0.67
F	1.07		1.32
F1	1.90		2.38
F2	2.87		3.38
G	10.90 BSC		
H	15.77		16.02
L	20.82		21.07
L1	4.16		4.47
L2	5.49		5.74
L3	20.05		20.30
L4	3.68		3.93
L5	6.04		6.29
M	2.25		2.55
V		10°	
V1		3°	
V3		20°	
Dia.	3.55		3.66

Figure 22. TO-247 long leads drawing



7395426\_G

## 5 Revision history

Table 11. Document revision history

Date	Revision	Changes
11-Dec-2012	1	First release.

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