

N-channel 600 V, 0.184 Ω typ., 16 A MDmesh™ M2 EP Power MOSFET in a PowerFLAT™ 8x8 HV package

Datasheet - production data

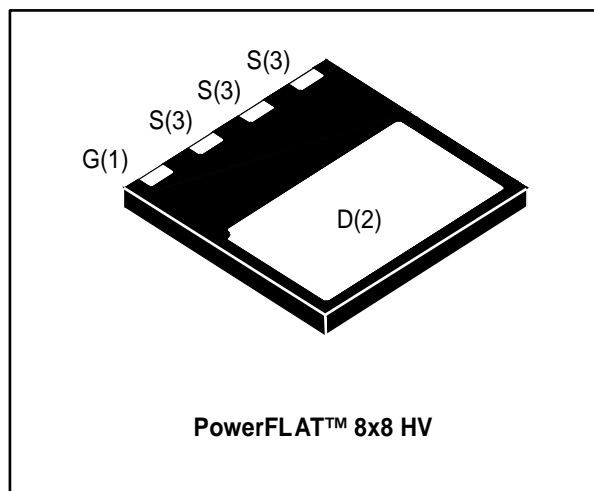
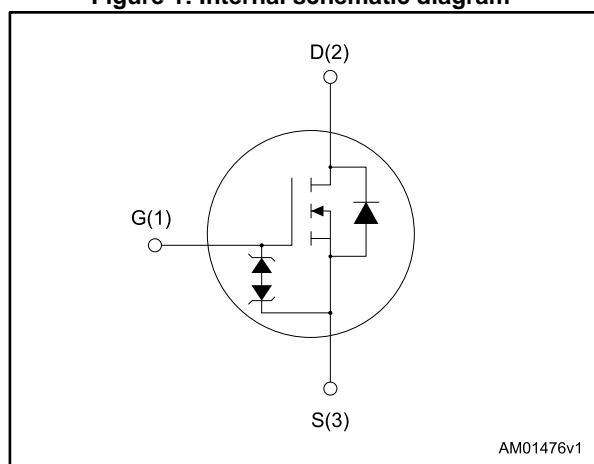


Figure 1: Internal schematic diagram



Features

Order code	V_{DS} @ T_{Jmax}	$R_{DS(on)}$ max.	I_D
STL25N60M2-EP	650 V	0.206 Ω	16 A

- Extremely low gate charge
- Excellent output capacitance (C_{OSS}) profile
- Very low turn-off switching losses
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications
- Tailored for Very High Frequency Converters ($f > 150$ kHz)

Description

This device is an N-channel Power MOSFET developed using MDmesh™ M2 EP enhanced performance technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance, optimized switching characteristics with very low turn-off switching losses, rendering it suitable for the most demanding very high frequency converters.

Table 1: Device summary

Order code	Marking	Package	Packaging
STL25N60M2-EP	25N60M2EP	PowerFLAT™ 8x8 HV	Tape and reel

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	16 ⁽¹⁾	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	10 ⁽¹⁾	A
I_{DM} ⁽²⁾	Drain current (pulsed)	64 ⁽¹⁾	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	125	W
dv/dt ⁽³⁾	Peak diode recovery voltage slope	15	V/ns
dv/dt ⁽⁴⁾	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature	- 55 to 150	$^\circ\text{C}$
T_j	Max. operating junction temperature		

Notes:

⁽¹⁾The value is limited by package.

⁽²⁾Pulse width limited by safe operating area.

⁽³⁾ $I_{SD} \leq 16\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$; $V_{DS(\text{peak})} < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$.

⁽⁴⁾ $V_{DS} \leq 480\text{ V}$

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-case}}$	Thermal resistance junction-case max	1	$^\circ\text{C}/\text{W}$
$R_{thj\text{-pcb}}$ ⁽¹⁾	Thermal resistance junction-pcb max	45	$^\circ\text{C}/\text{W}$

Notes:

⁽¹⁾When mounted on FR-4 board of inch^2 , 2oz Cu.

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by $T_{j\text{max}}$)	3.5	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$; $V_{DD} = 50\text{ V}$)	180	mJ

2 Electrical characteristics

$T_C = 25\text{ °C}$ unless otherwise specified

Table 5: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	600			V
I_{DSS}	Zero gate voltage Drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$, $T_C = 125\text{ °C}$			100	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 25\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 8\text{ A}$		0.184	0.205	Ω

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	1090	-	pF
C_{oss}	Output capacitance		-	56	-	pF
C_{rss}	Reverse transfer capacitance		-	1.6	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }480\text{ V}$, $V_{GS} = 0\text{ V}$	-	255	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$, $I_D = 0\text{ A}$	-	7	-	Ω
Q_g	Total gate charge	$V_{DD} = 480\text{ V}$, $I_D = 18\text{ A}$, $V_{GS} = 10\text{ V}$ (see Figure 16: "Gate charge test circuit")	-	29	-	nC
Q_{gs}	Gate-source charge		-	6	-	nC
Q_{gd}	Gate-drain charge		-	12	-	nC

Notes:

⁽¹⁾ $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7: Switching Energy

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$E_{(off)}$	Turn-off energy (from 90% V_{GS} to 0% I_D)	$V_{DD} = 400\text{ V}$, $I_D = 2\text{ A}$ $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	7	-	μJ
		$V_{DD} = 400\text{ V}$, $I_D = 4\text{ A}$ $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	8	-	μJ

Table 8: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 9\text{ A}$ $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 15: "Switching times test circuit for resistive load" and Figure 20: "Switching time waveform")	-	15	-	ns
t_r	Rise time		-	10	-	ns
$t_{d(off)}$	Turn-off-delay time		-	61	-	ns
t_f	Fall time		-	16	-	ns

Table 9: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}^{(1)}$	Source-drain current		-		16	A
$I_{SDM}^{(1), (2)}$	Source-drain current (pulsed)		-		64	A
$V_{SD}^{(3)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 16\text{ A}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 18\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 100\text{ V}$ (see Figure 17: "Test circuit for inductive load switching and diode recovery times")	-	360		ns
Q_{rr}	Reverse recovery charge		-	5		μC
I_{RRM}	Reverse recovery current		-	28		A
t_{rr}	Reverse recovery time	$I_{SD} = 18\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 100\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 17: "Test circuit for inductive load switching and diode recovery times")	-	445		ns
Q_{rr}	Reverse recovery charge		-	6.5		μC
I_{RRM}	Reverse recovery current		-	29		A

Notes:

- (1) The value is rated according to $R_{thj-case}$ and limited by package.
(2) Pulse width is limited by safe operating area
(3) Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.2 Electrical characteristics (curves)

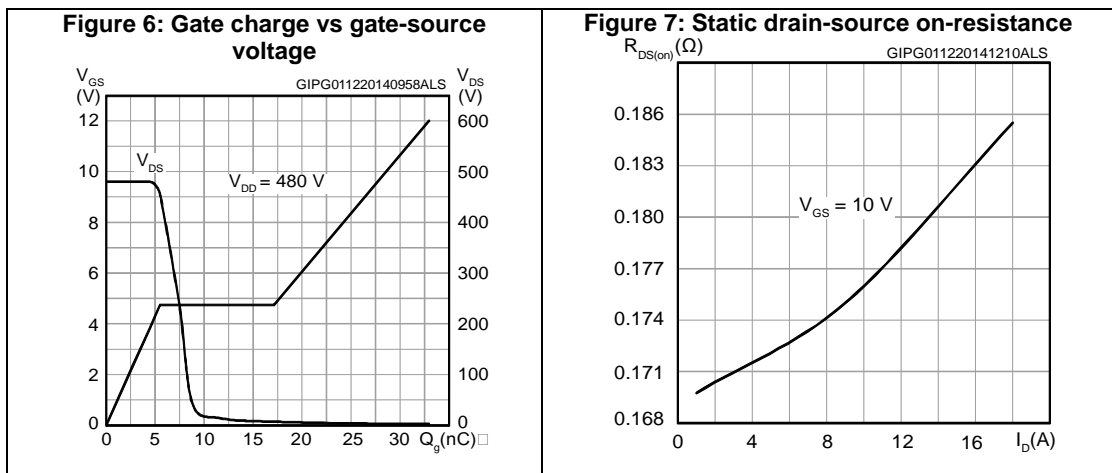
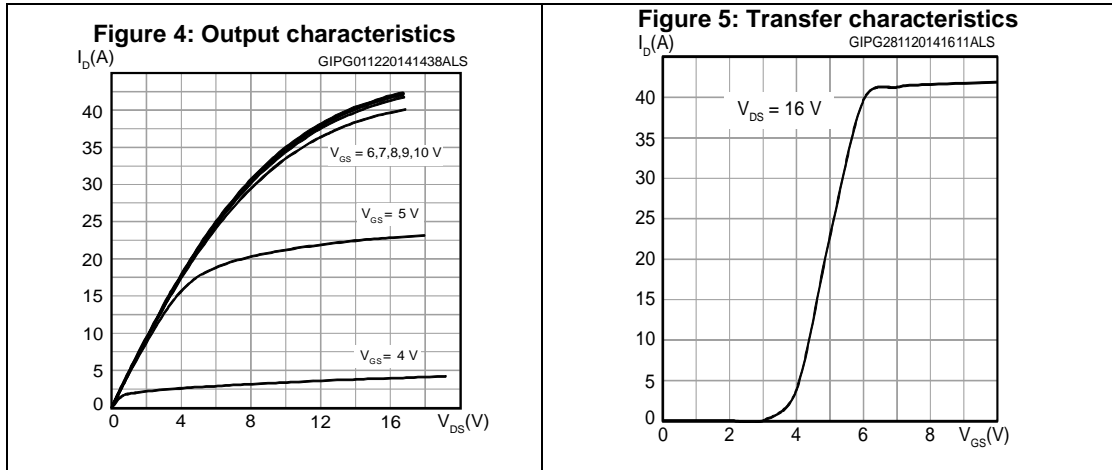
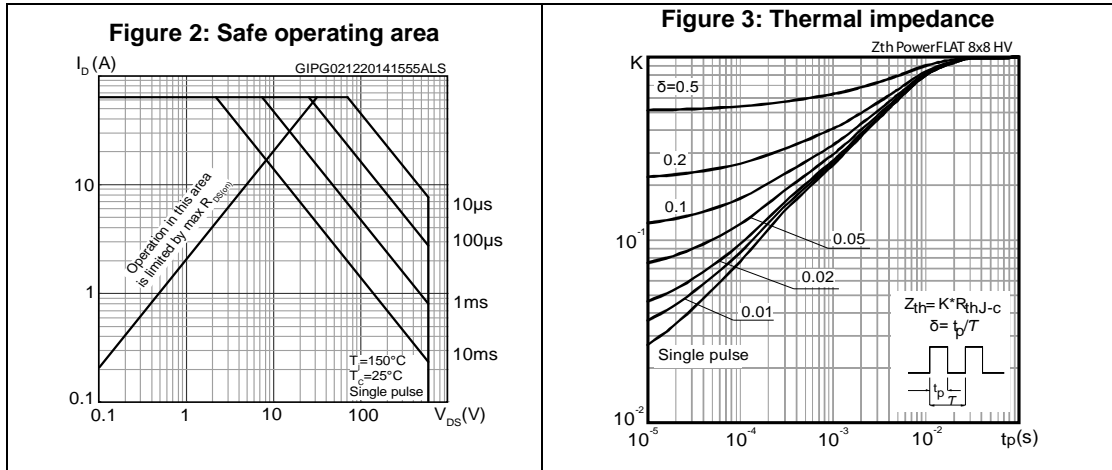


Figure 8: Capacitance variations

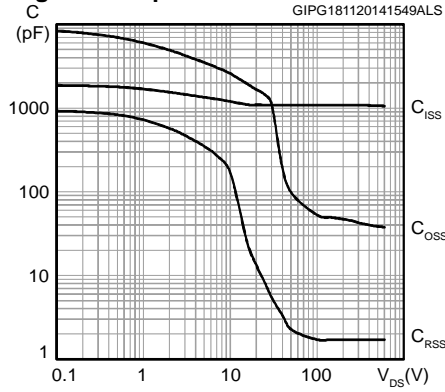


Figure 9: Output capacitance stored energy

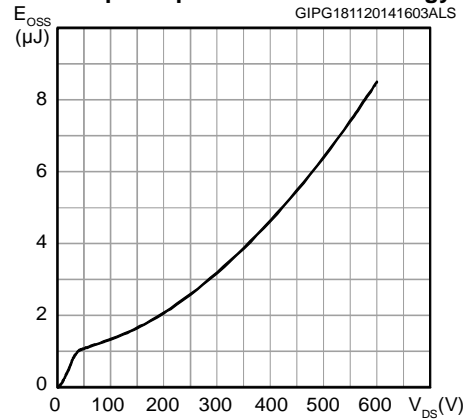


Figure 10: Turn-off switching loss vs drain current

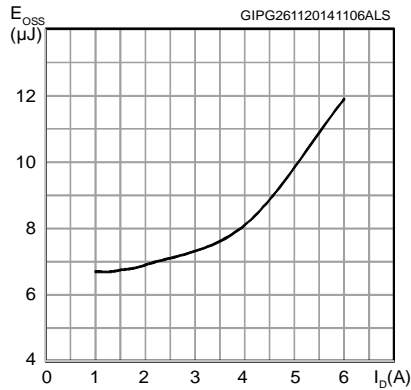


Figure 11: Normalized gate threshold voltage vs temperature

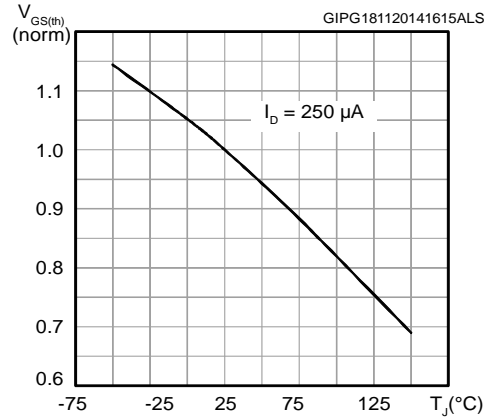


Figure 12: Normalized on-resistance vs temperature

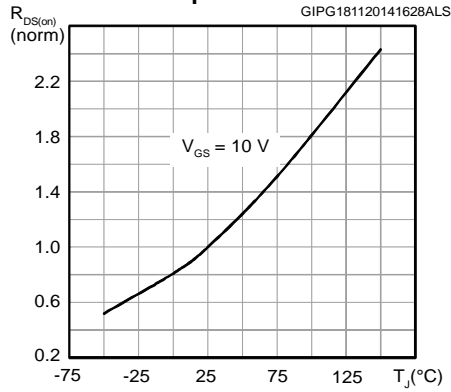


Figure 13: Source-drain diode forward characteristics

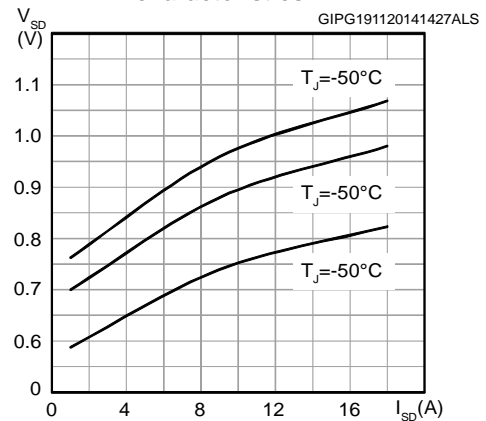
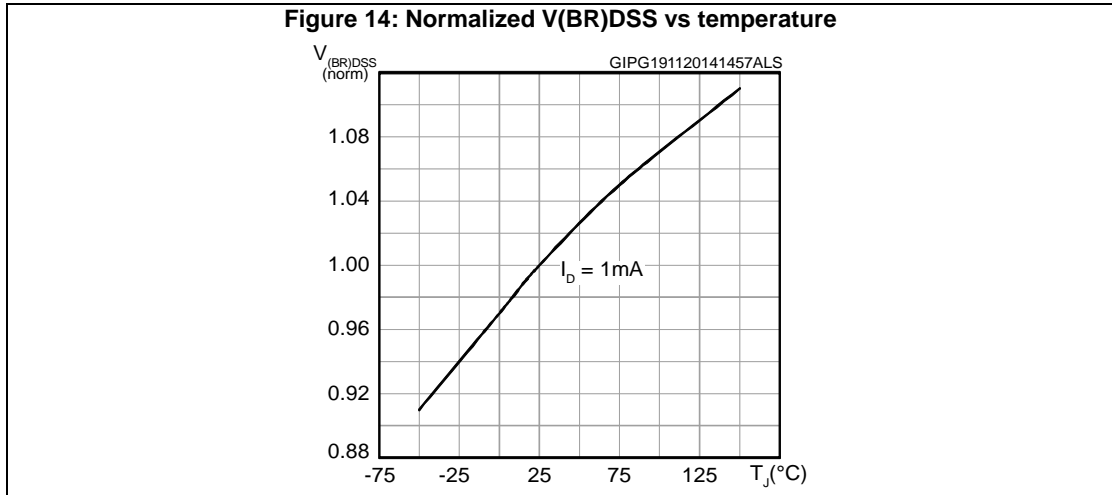
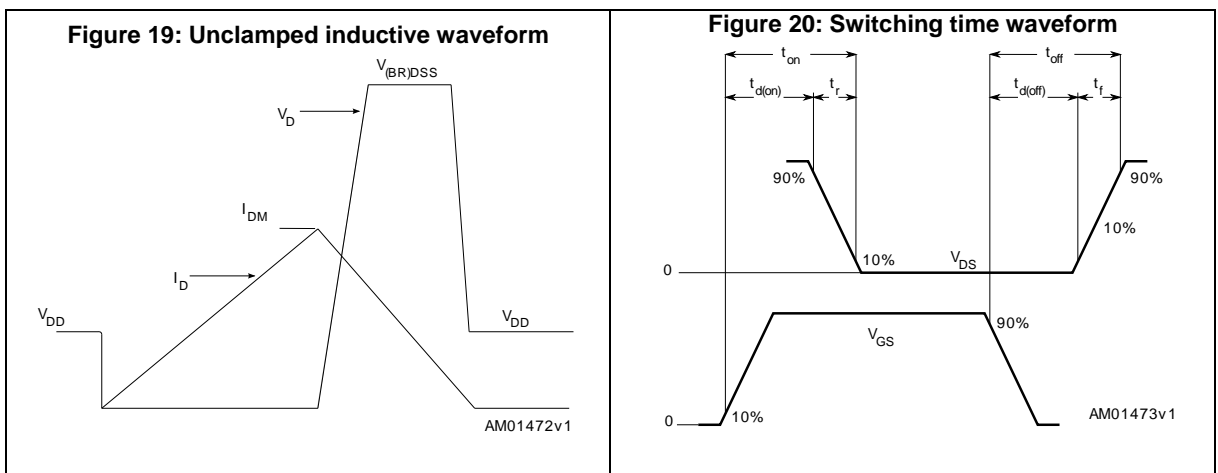
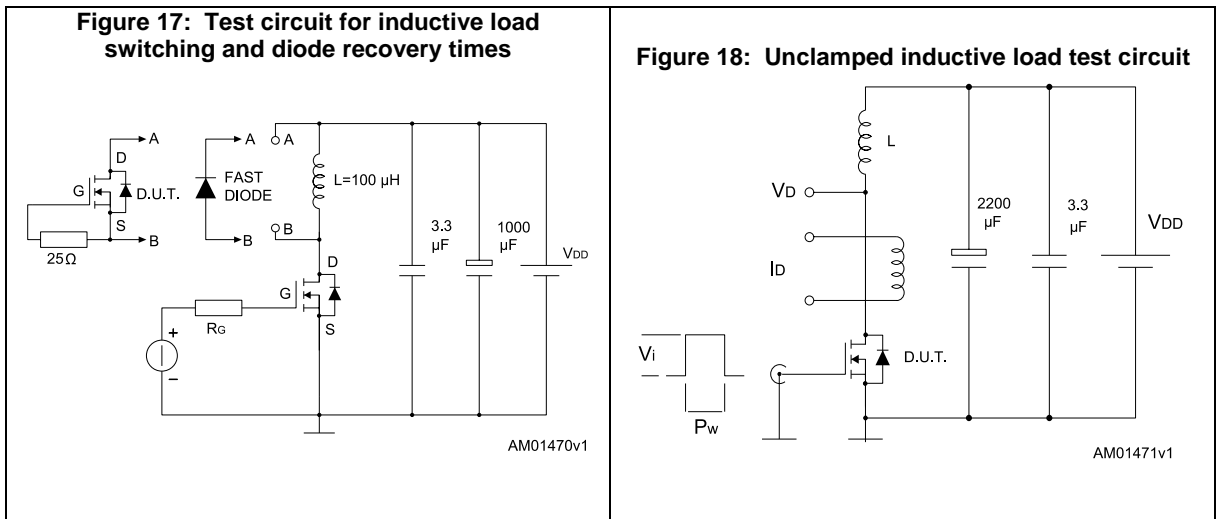
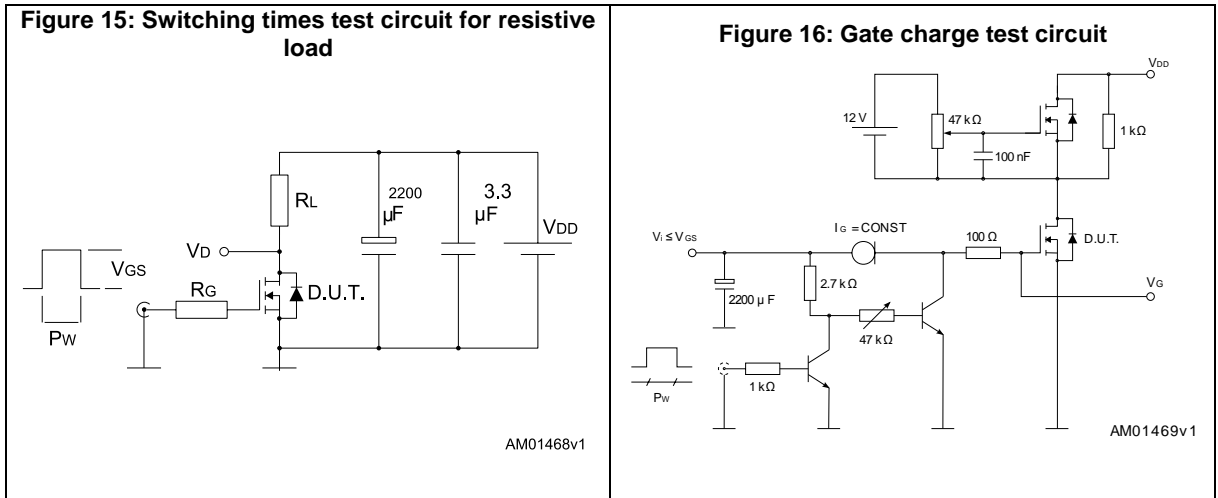


Figure 14: Normalized V(BR)DSS vs temperature



3 Test circuits



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

4.1 PowerFLAT 8x8 HV package information

Figure 21: PowerFLAT™ 8x8 HV drawing

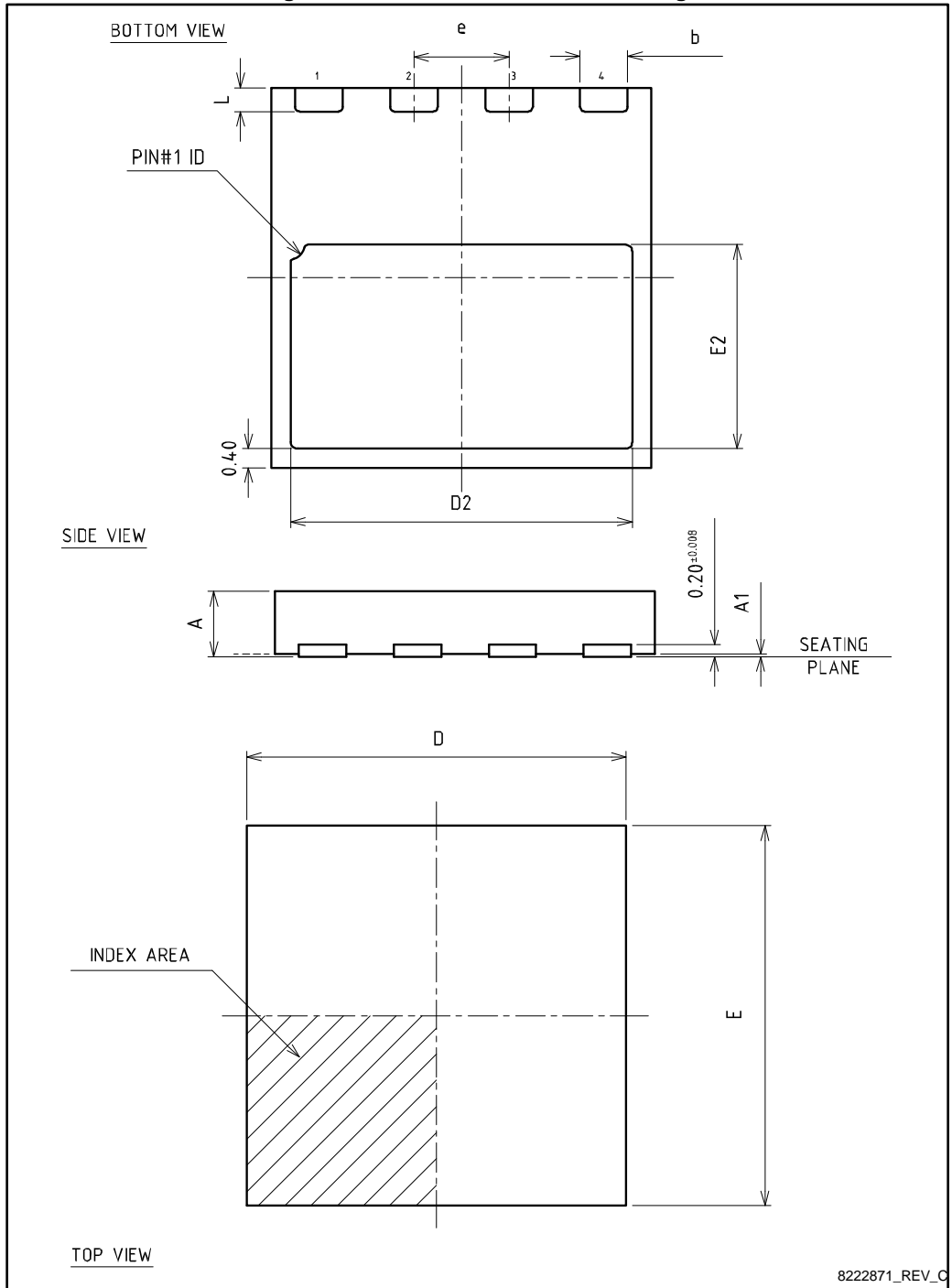
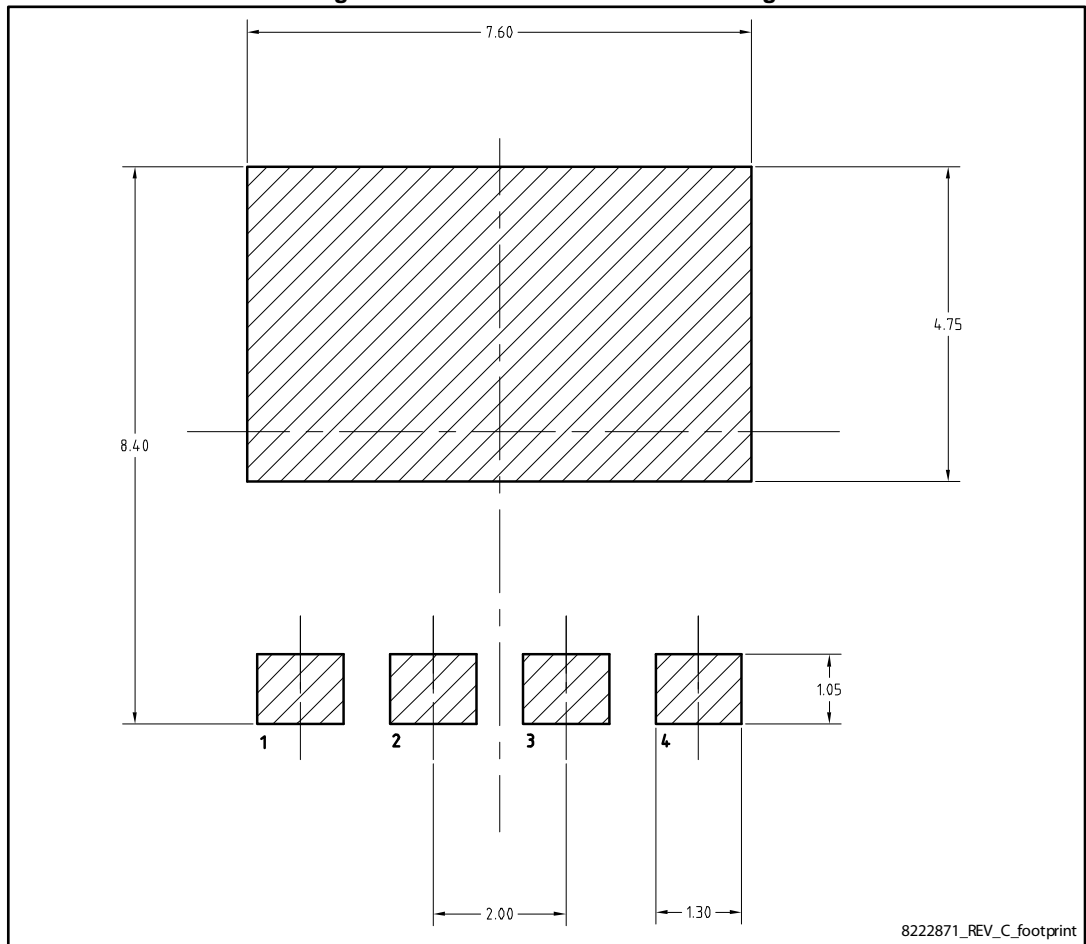


Table 10: PowerFLAT™ 8x8 HV mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
b	0.95	1.00	1.05
D		8.00	
E		8.00	
D2	7.05	7.20	7.30
E2	4.155	4.30	4.40
e		2.00	
L	0.40	0.50	0.60

Figure 22: PowerFLAT™ 8x8 HV drawing



All the dimensions are in millimeters.

5 Packaging mechanical data

Figure 23: PowerFLAT™ 8x8 HV tape

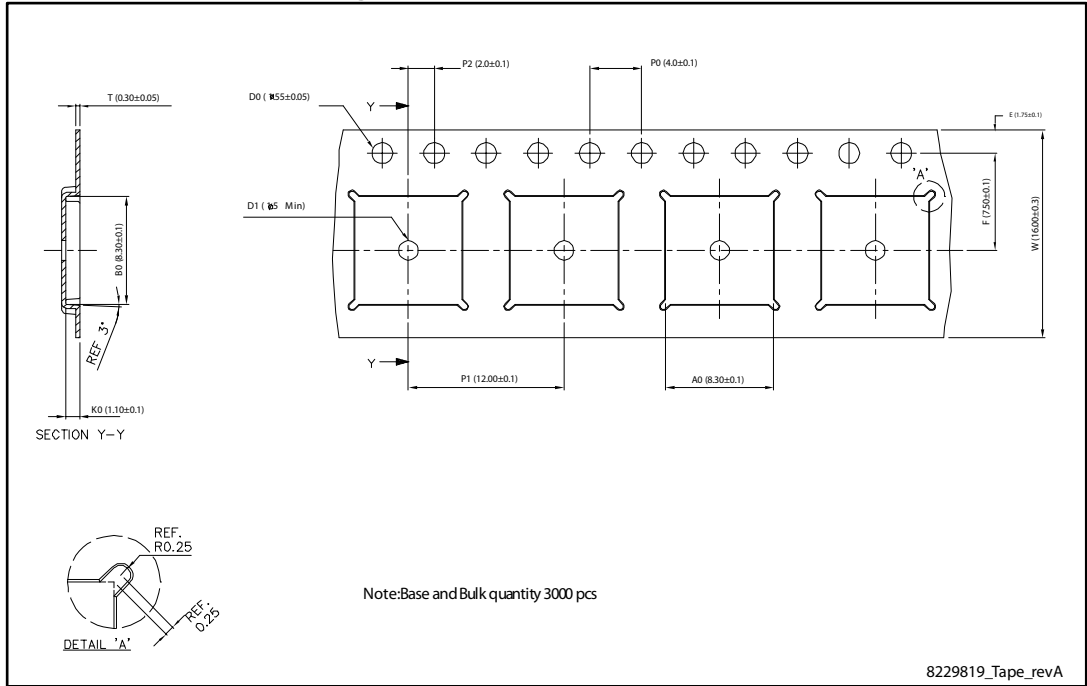
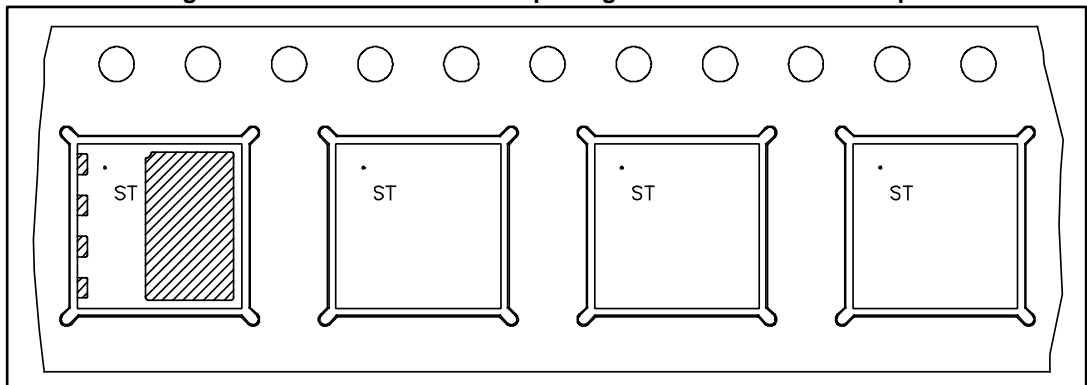


Figure 24: PowerFLAT™ 8x8 HV package orientation in carrier tape



6 Revision history

Table 11: Document revision history

Date	Revision	Changes
02-Dec-2014	1	First release.
12-Jan-2015	2	Updated product status from "preliminary data" to "production data".

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