



# STL40DN3LLH5

Dual N-channel 30 V, 0.016  $\Omega$  typ., 11 A STripFET™V  
Power MOSFET in a PowerFLAT™ 5x6 double island

Datasheet — production data

## Features

Order code	V <sub>DSS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STL40DN3LLH5	30 V	< 0.018 $\Omega$	11 A <sup>(1)</sup>

1. The value is rated according R<sub>thj-pcb</sub>

- R<sub>DS(on)</sub> \* Q<sub>g</sub> industry benchmark
- Extremely low on-resistance R<sub>DS(on)</sub>
- Very low switching gate charge
- High avalanche ruggedness
- Low gate drive power losses

## Applications

- Switching applications

## Description

This device is an N-channel Power MOSFET developed using STMicroelectronics' STripFET™V technology. The device has been optimized to achieve very low on-state resistance, contributing to a FOM that is among the best in its class.

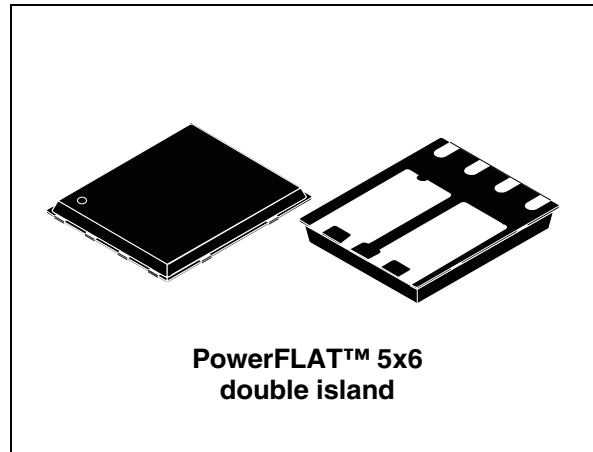


Figure 1. Internal schematic diagram

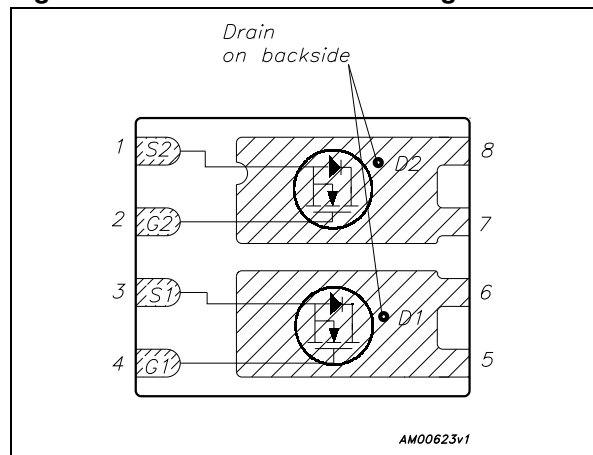


Table 1. Device summary

Order code	Marking	Package	Packaging
STL40DN3LLH5	40DN3LLH5	PowerFLAT™ 5x6 double island	Tape and reel

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	30	V
$V_{GS}$	Gate-source voltage	$\pm 22$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	40	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	26	A
$I_D^{(2)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	11	A
$I_D^{(2)}$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	7	A
$I_{DM}^{(3)}$	Drain current (pulsed)	44	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25^\circ\text{C}$	60	W
$P_{TOT}^{(2)}$	Total dissipation at $T_C = 25^\circ\text{C}$	4	W
	Derating factor	0.03	W/ $^\circ\text{C}$
$T_J$	Operating junction temperature	-55 to 150	$^\circ\text{C}$
$T_{stg}$	Storage temperature		

1. The value is rated according  $R_{thj-c}$
2. The value is rated according  $R_{thj-pcb}$
3. Pulse width limited by safe operating area

**Table 3. Thermal resistance**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case drain, steady state	2.08	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-ambient	32	$^\circ\text{C}/\text{W}$

1. When mounted on FR-4 board of 1inch<sup>2</sup>, 2oz Cu,  $t < 10$  sec

## 2 Electrical characteristics

( $T_{CASE}=25\text{ }^{\circ}\text{C}$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0$	30			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 30\text{ V}$ , $V_{DS} = 30\text{ V @ }125\text{ }^{\circ}\text{C}$			1 10	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 22\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	1	1.5		V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$ , $I_D = 5.5\text{ A}$ $V_{GS} = 4.5\text{ V}$ , $I_D = 5.5\text{ A}$		0.016 0.02	0.018 0.025	$\Omega$ $\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$	-	475	-	pF
$C_{oss}$	Output capacitance		-	97	-	pF
$C_{rss}$	Reverse transfer capacitance		-	19	-	pF
$Q_g$	Total gate charge	$V_{DD} = 15\text{ V}$ , $I_D = 11\text{ A}$	-	4.5	-	nC
$Q_{gs}$	Gate-source charge	$V_{GS} = 4.5\text{ V}$	-	1.7	-	nC
$Q_{gd}$	Gate-drain charge	(see <a href="#">Figure 13</a> )	-	1.9	-	nC

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD}=15\text{ V}$ , $I_D=11\text{ A}$ , $R_G=4.7\ \Omega$ , $V_{GS}=10\text{ V}$ (see <a href="#">Figure 12</a> )		4		ns
$t_r$	Rise time			22		ns
$t_{d(off)}$	Turn-off delay time		-	13	-	ns
$t_f$	Fall time			2.8		ns

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		11	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		44	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=11\text{ A}$ , $V_{GS}=0$	-		1.1	V
$t_{rr}$	Reverse recovery time	$I_{SD}=11\text{ A}$ , $di/dt=100\text{ A}/\mu\text{s}$ , $V_{DD}=25\text{ V}$ , $T_j=150\text{ }^\circ\text{C}$		16.2		ns
$Q_{rr}$	Reverse recovery charge		-	1		nC
$I_{RRM}$	Reverse recovery current			8.1		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

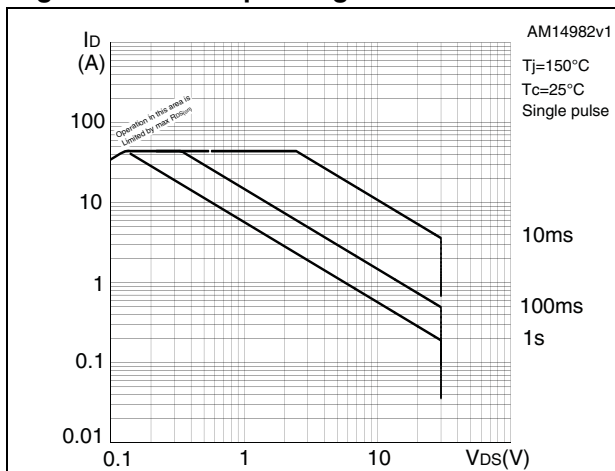


Figure 3. Thermal impedance

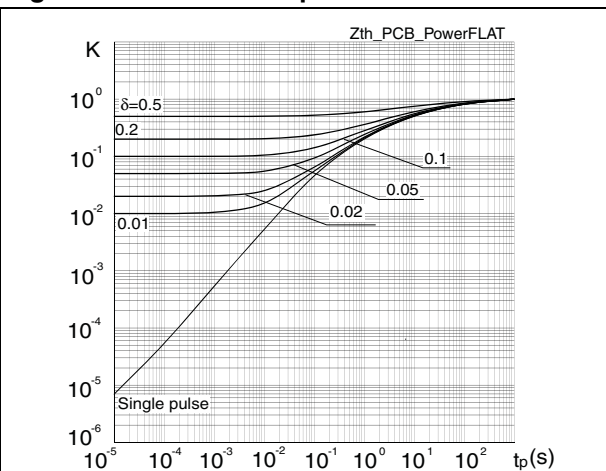


Figure 4. Output characteristics

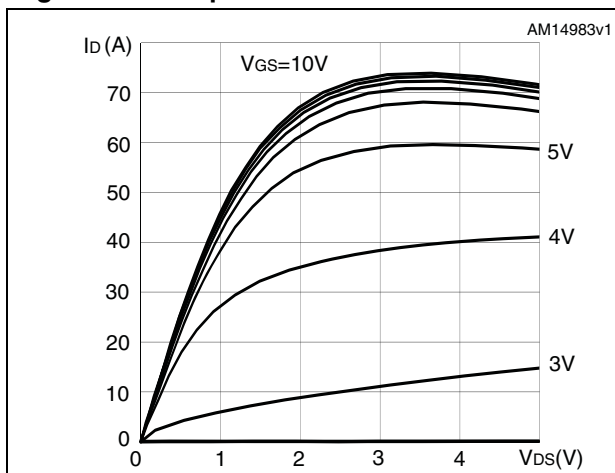


Figure 5. Transfer characteristics

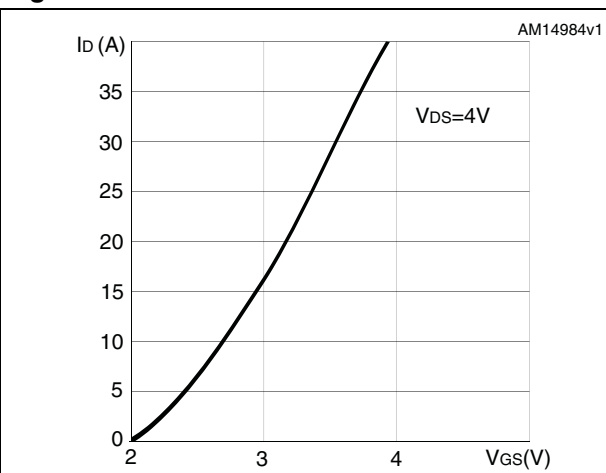


Figure 6. Normalized B<sub>V</sub>D<sub>SS</sub> vs temperature

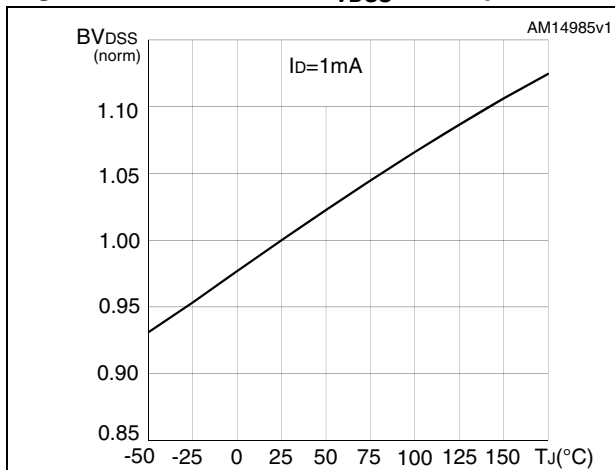


Figure 7. Static drain-source on-resistance

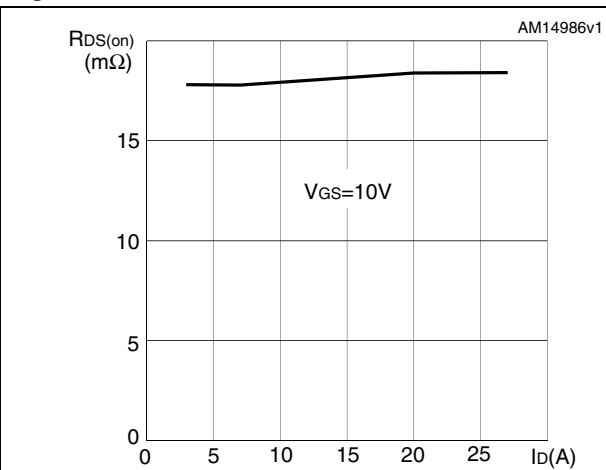


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

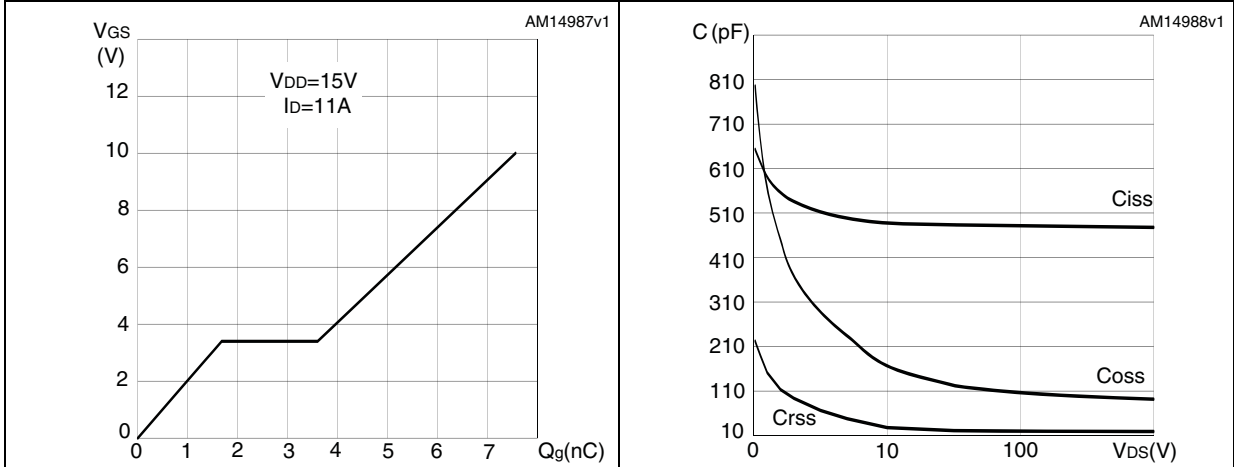
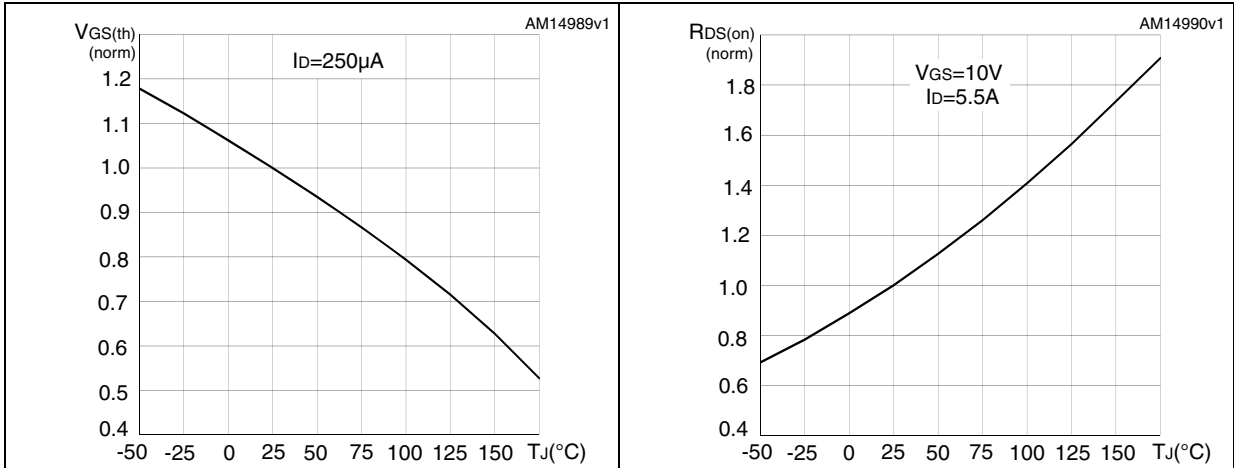
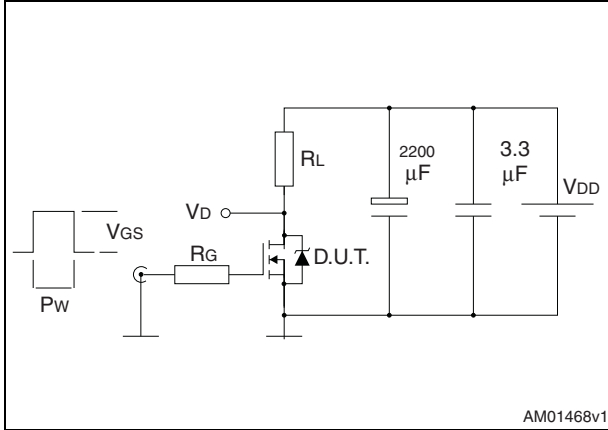


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on-resistance vs temperature

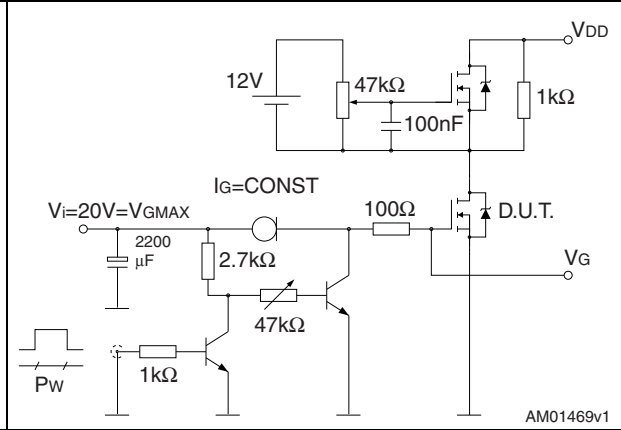


### 3 Test circuits

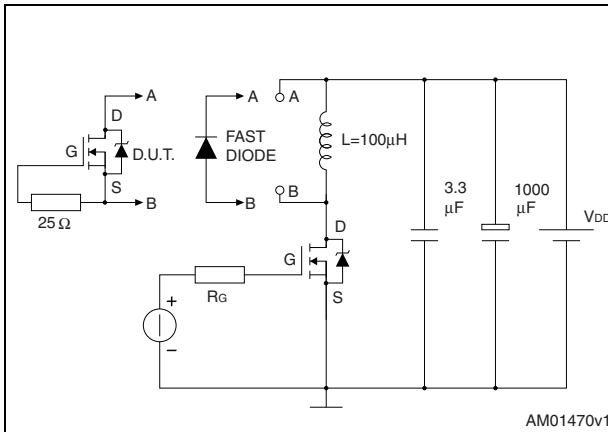
**Figure 12. Switching times test circuit for resistive load**



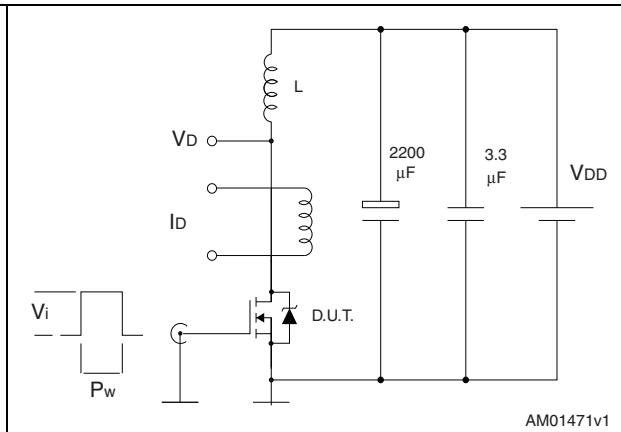
**Figure 13. Gate charge test circuit**



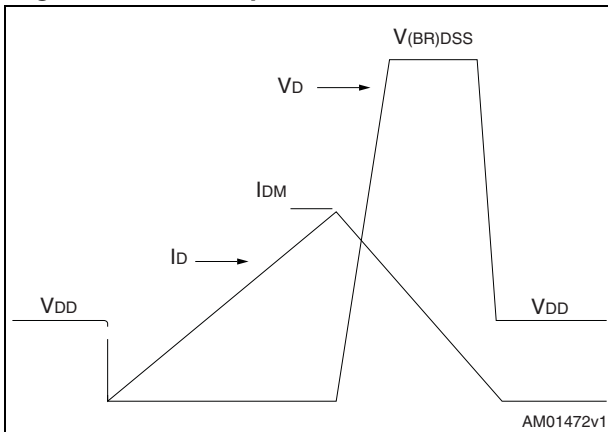
**Figure 14. Test circuit for inductive load switching and diode recovery times**



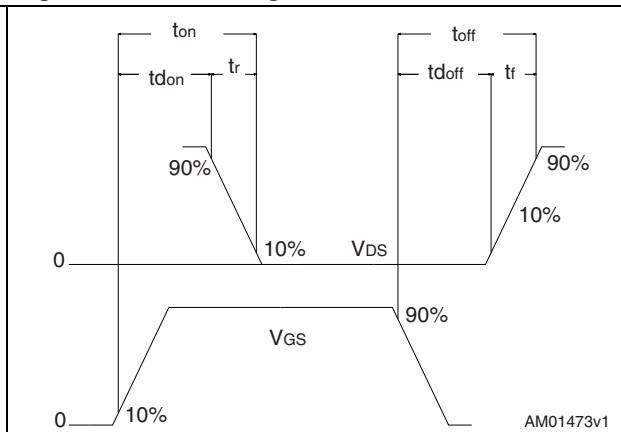
**Figure 15. Unclamped inductive load test circuit**



**Figure 16. Unclamped inductive waveform**



**Figure 17. Switching time waveform**



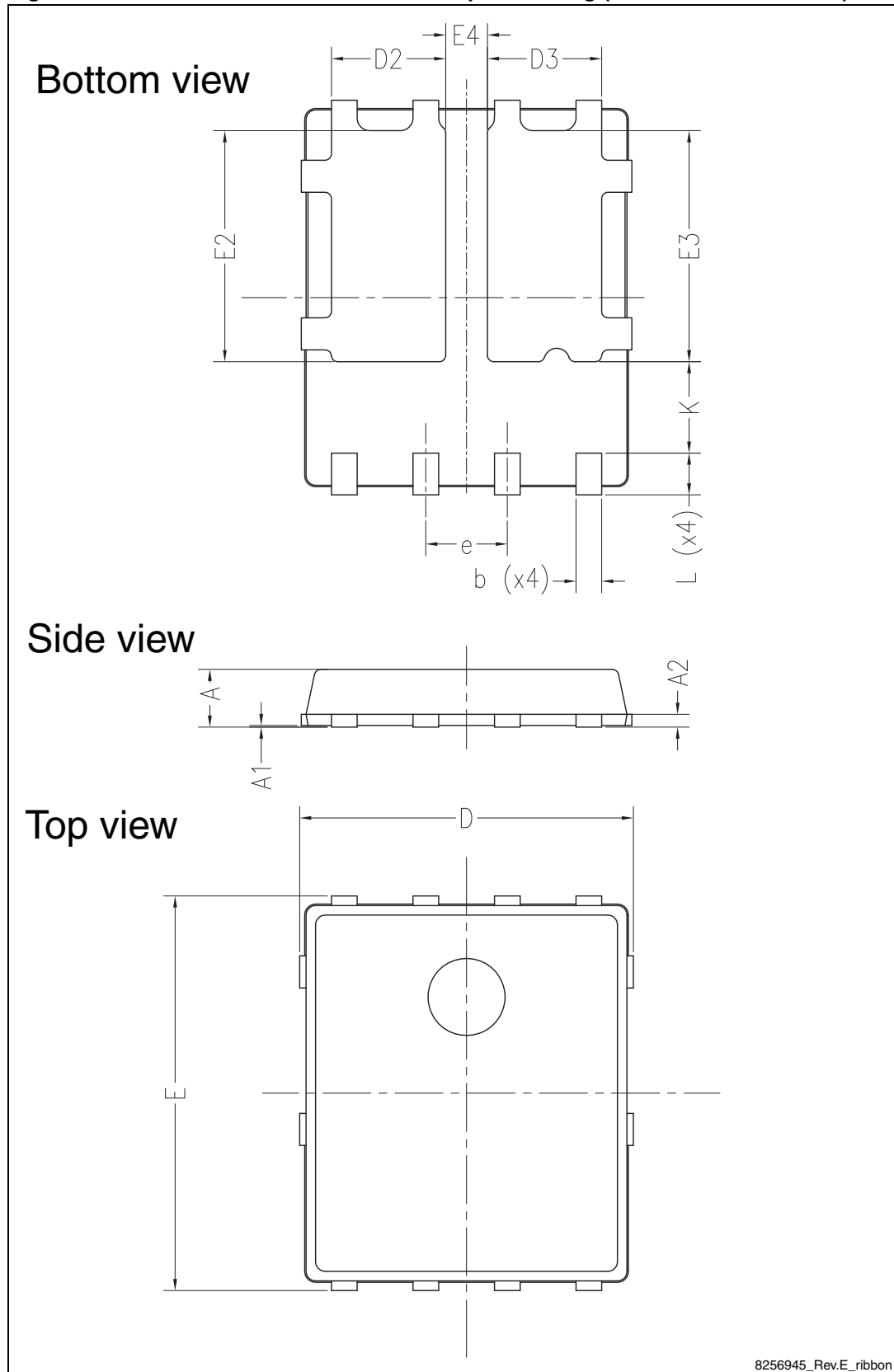
## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

**Table 8. PowerFLAT™ 5x6 - 8 leads dual pad (ribbon) mechanical data**

Ref.	Dimensions (mm)		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D		5.20	
E		6.15	
D2	1.68		1.88
E2	3.50		3.70
D3	1.68		1.88
E3	3.50		3.70
E4	0.55		0.75
e		1.27	
L	0.50		0.80
K	1.275		1.575

Figure 18. PowerFLAT™ 5x6 - 8 leads dual pad drawing (dimensions are in mm)





## 5 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
24-Jan-2011	1	First release.
03-Oct-2012	2	<i>Section 2.1: Electrical characteristics (curves)</i> has been added. Document status promoted from preliminary data to datasheet. Minor text changes.

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