STL42P4LLF6

P-channel 40 V, 0.016 Ω typ., 10 A STripFET™ VI DeepGATE™ Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - target specification

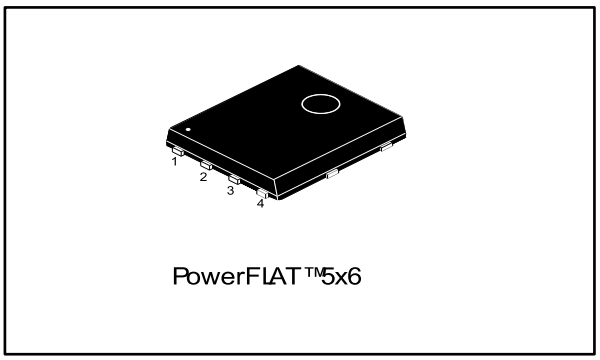
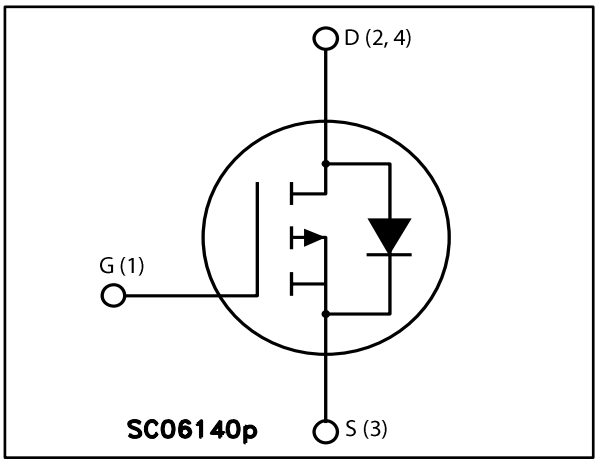


Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$max	I_D	P_{TOT}
STL42P4LLF6	40 V	0.022 Ω	10 A	4.8 W

- $R_{DS(on)}$* $Q_g$industry benchmark
- Extremely low on-resistance $R_{DS(on)}$
- High avalanche ruggedness
- Low gate drive power losses

Applications

- Switching applications

Description

This device is a P-channel Power MOSFET developed using the 6th generation of STripFET™ DeepGATE™ technology, with a new gate structure. The resulting Power MOSFET exhibits the lowest $R_{DS(on)}$ in all packages.

Table 1: Device summary

Order code	Marking	Package	Packaging
STL42P4LLF6	42P4LLF6	PowerFLAT™ 5x6	Tape and reel

For the P-channel Power MOSFETs the actual polarity of the voltages and the current must be reversed.

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	40	V
V_{GS}	Gate-source voltage	± 20	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	42	A
I_D (1)	Drain current (continuous) at T_C = 100 °C	29	
I_D (2)	Drain current (continuous) at T_{pcb} = 25 °C	10	
I_D (2)	Drain current (continuous) at T_{pcb} = 100 °C	7.5	A
I_D (1)(3)	Drain current (pulsed)	168	A
I_{DM} (2)(3)	Drain current (pulsed)	40	A
P_{TOT} (1)	Total dissipation at T_C = 25 °C	75	W
P_{TOT} (2)	Total dissipation at T_{pcb} = 25 °C	4.8	W
	Derating factor	0.03	W/°C
T_{stg}	Storage temperature	- 55 to 175	°C
T_j	Max. operating junction temperature	150	°C

Notes:

(1)The value is rated according to $R_{thj\text{-}c}$

(2)This value is rated according to $R_{thj\text{-}pcb}$

(3)Pulse width is limited by safe operating area

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	2.00	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb, single operation	31.3	°C/W

Notes:

(1)When mounted on FR-4 board of 1 inch², 2oz Cu, steady state

For the P-channel Power MOSFETs the actual polarity of the voltages and the current must be reversed.

2 Electrical characteristics

(T_C= 25 °C unless otherwise specified)

Table 4: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0, I_D = 250 µA	40			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0, V_{DS} = 40 V			1	µA
		V_{DS} = 40 V, T_C = 125 °C			10	
I_{GSS}	Gate-body leakage current	V_{DS} = 0, V_{GS} = ± 20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	1			V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 5 A		0.016	0.022	Ω
		V_{GS} = 4.5 V, I_D = 5 A		0.025	0.035	Ω

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 32 V, f = 1 MHz, V_{GS} = 0	-	2300	-	pF
C_{oss}	Output capacitance		-	325	-	pF
C_{rss}	Reverse transfer capacitance		-	120	-	pF
Q_g	Total gate charge	V_{DD} = 32 V, ID = 10 A, V_{GS} = 4.5 V	-	22	-	nC
Q_{gs}	Gate-source charge		-	TBD	-	nC
Q_{gd}	Gate-drain charge		-	TBD	-	nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 32 V, I_D = 5 A, R_G = 4.7 Ω, V_{GS} = 10 V	-	TBD	-	ns
t_r	Rise time		-	TBD	-	ns
$t_{d(off)}$	Turn-off delay time		-	TBD	-	ns
t_f	Fall time		-	TBD	-	ns

For the P-channel Power MOSFETs the actual polarity of the voltages and the current must be reversed.

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		10	A
I_{SDM} (1)	Source-drain current (pulsed)		-		40	A
V_{SD} (2)	Forward on voltage	I_{SD}= 5 A, V_{GS}= 0	-		1.1	V
t_{rr}	Reverse recovery time	I_{SD}= 5 A, di/dt = 100 A/µs V_{DD}= 16 V, T_j= 150 °C	-	TBD		ns
Q_{rr}	Reverse recovery charge		-	TBD		nC
I_{RRM}	Reverse recovery current		-	TBD		A

Notes:

(1)Pulse width limited by safe operating area

(2)Pulsed: pulse duration = 300 µs, duty cycle 1.5 %

For the P-channel Power MOSFETs the actual polarity of the voltages and the current must be reversed.

3 Test circuits

Figure 2: Switching times test circuit for resistive load

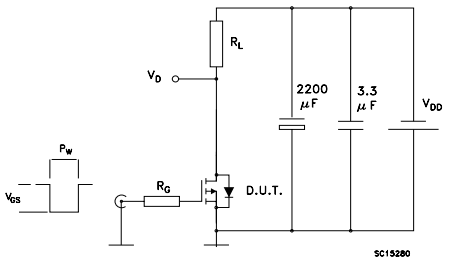


Figure 3: Gate charge test circuit

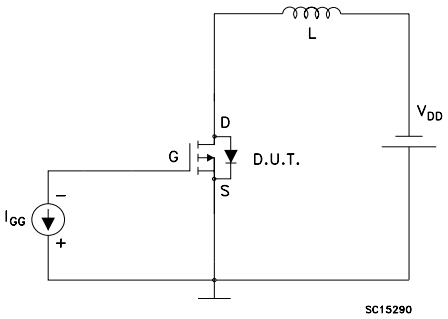
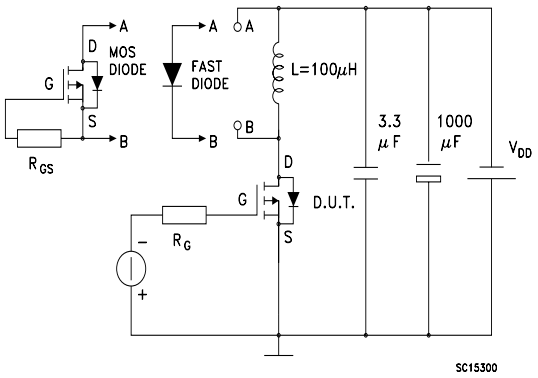


Figure 4: Source-drain diode forward characteristics



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 PowerFLAT 5x6 type S-R package mechanical data

Figure 5: PowerFLAT™ 5x6 type S-R drawing

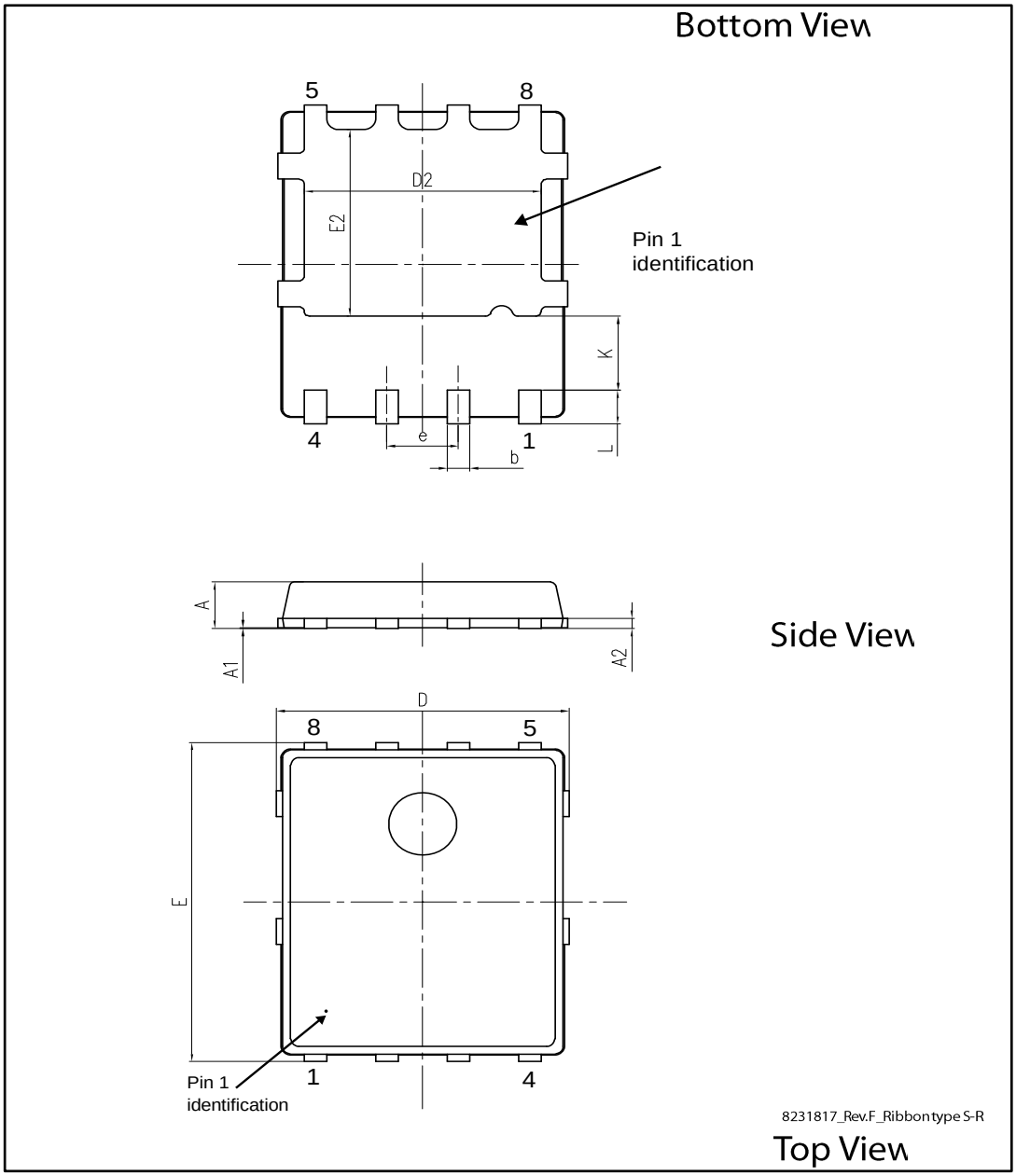
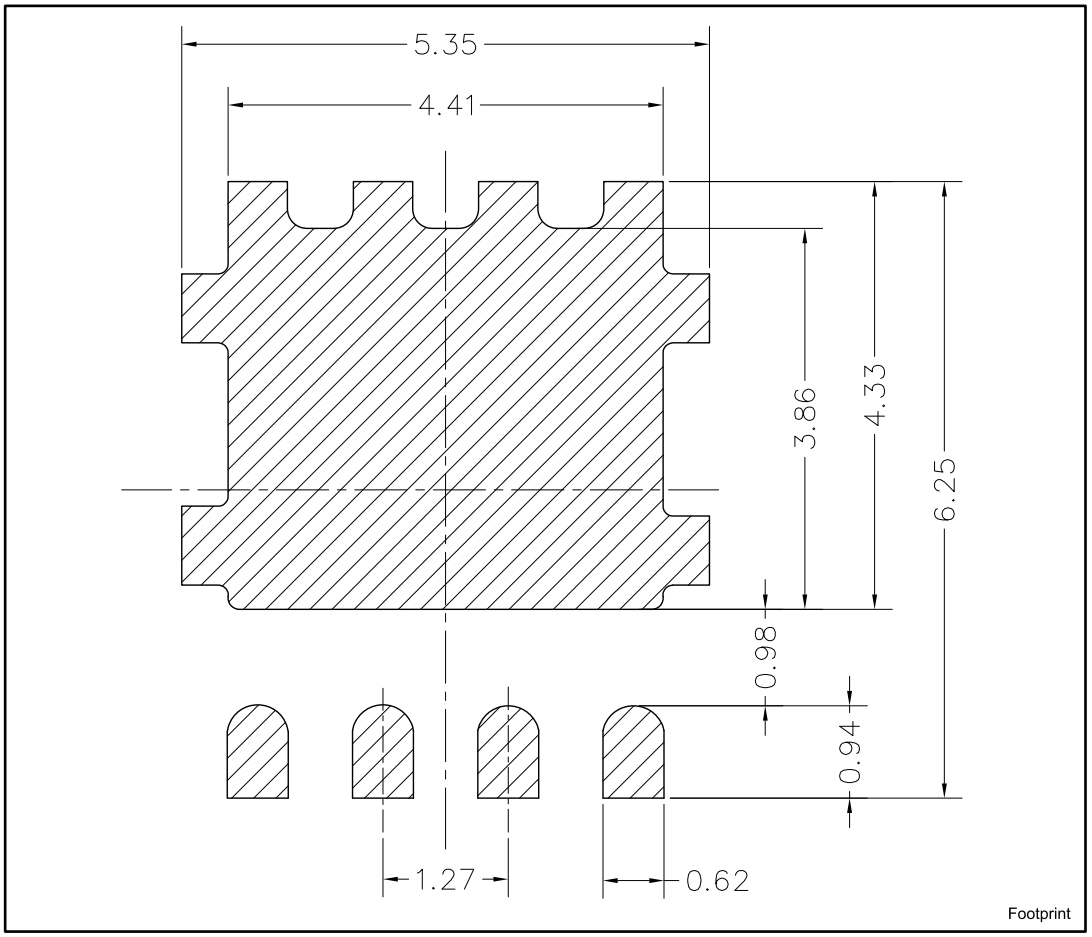


Table 8: PowerFLAT 5x6 type S-R mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D	5.00	5.20	5.40
E	5.95	6.15	6.35
D2	4.11		4.31
E2	3.50		3.70
e		1.27	
L	0.60		0.80
K	1.275		1.575

Figure 6: PowerFLAT™ 5x6 recommended footprint (dimensions are in mm)



5 Packaging mechanical data

5.1 PowerFLAT™ 5x6 packaging mechanical data

Figure 7: PowerFLAT™ 5x6 tape (dimensions are in millimeters)

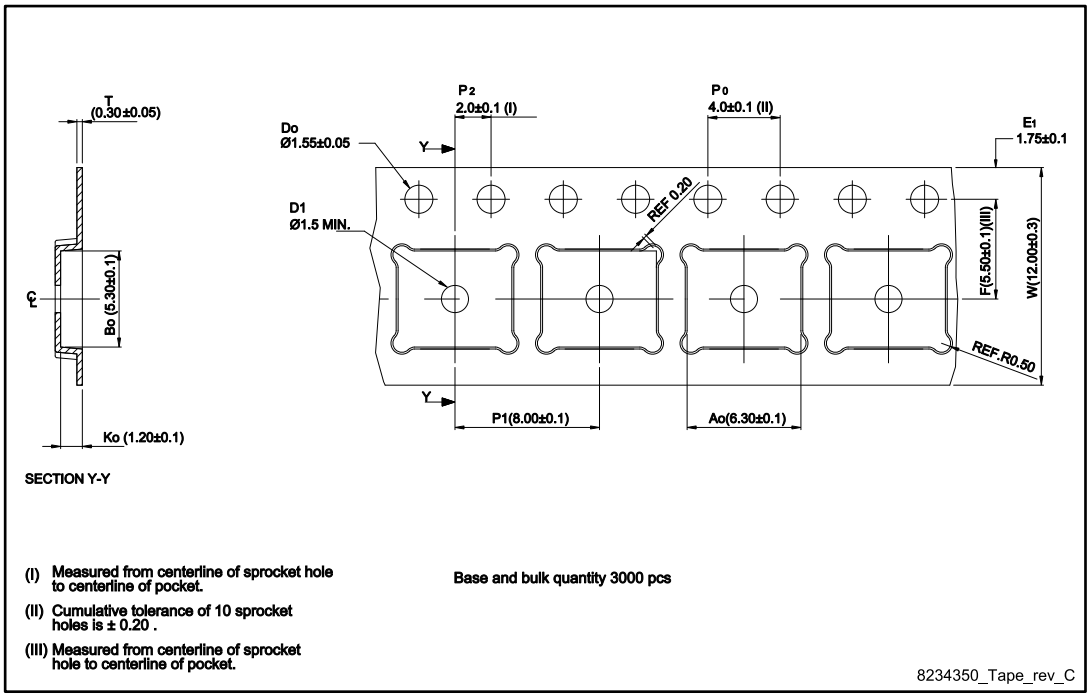


Figure 8: PowerFLAT™ 5x6 package orientation in carrier tape

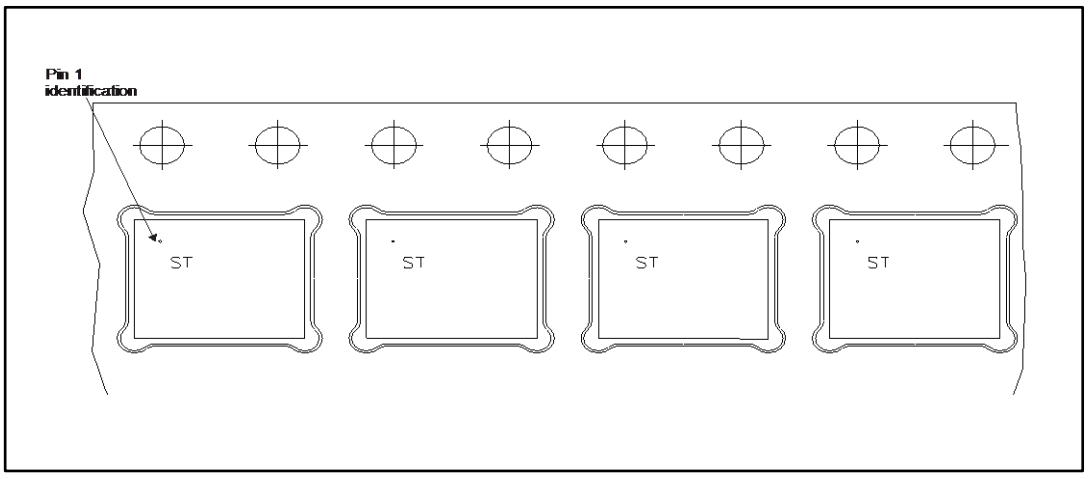
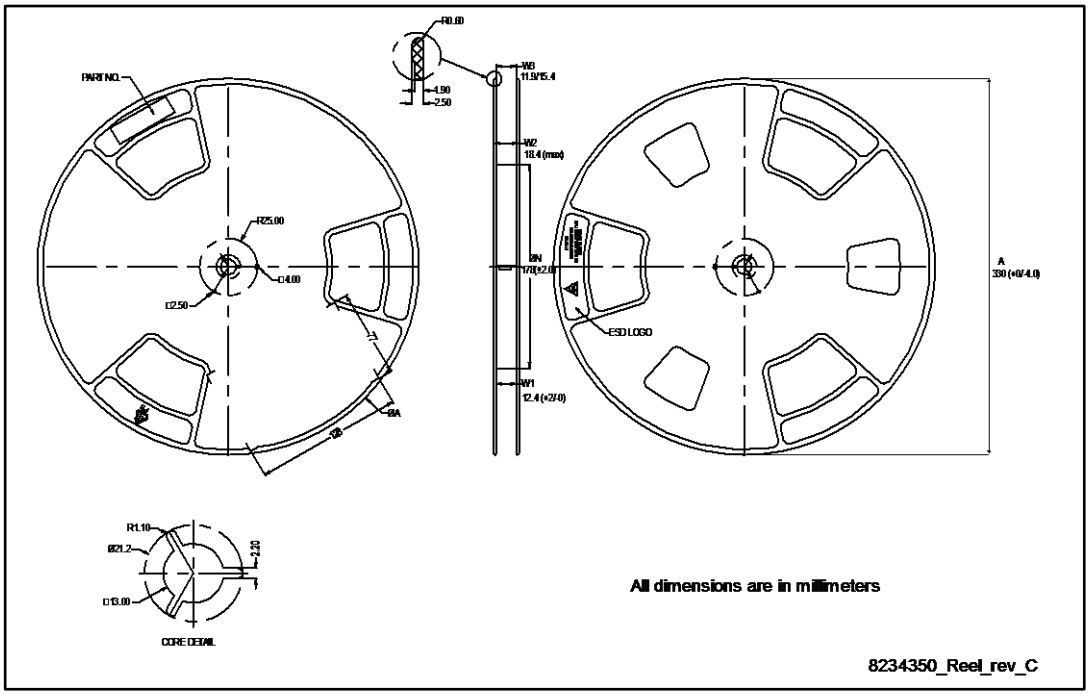


Figure 9: PowerFLAT™ 5x6 reel



6 Revision history

Table 9: Document revision history

Date	Revision	Changes
28-Jan-2014	1	First release.

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