

P-channel 30 V, 0.009 Ω typ., 62 A STripFET™ H6 Power MOSFET in a PowerFLAT 5x6 package

Datasheet - production data

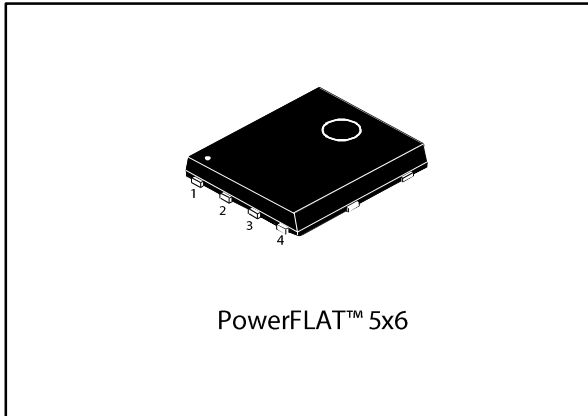
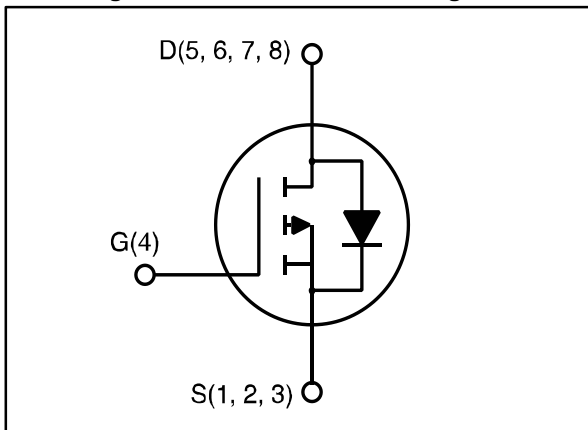


Figure 1: Internal schematic diagram



Features

Order codes	V _{DS}	R _{DS(on)} max	I _D
STL62P3LLH6	30 V	0.0105 Ω	62 A

- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

Applications

- Switching applications

Description

This device is a P-channel Power MOSFET developed using the STripFET™ H6 technology, with a new trench gate structure. The resulting Power MOSFET exhibits very low R_{DS(on)} in all packages.

Table 1: Device summary

Order codes	Marking	Package	Packaging
STL62P3LLH6	62P3LLH6	PowerFLAT™ 5x6	Tape and reel



For the P-channel Power MOSFETs the actual polarity of the voltages and the current must be reversed.

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	30	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	62	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	44	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$	14	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 100\text{ }^\circ\text{C}$	9.5	A
$I_D^{(1)(2)}$	Drain current (pulsed)	248	A
$I_{DM}^{(2)(3)}$	Drain current (pulsed)	56	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	100	W
$P_{TOT}^{(2)}$	Total dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$	4.8	W
T_{stg}	Storage temperature	- 55 to 175	$^\circ\text{C}$
T_j	Max. operating junction temperature	175	$^\circ\text{C}$

Notes:

- (1)The value is rated according to R_{thj-c} .
 (2)This value is rated according to $R_{thj-pcb}$.
 (3)Pulse width is limited by safe operating area.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	1.5	$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb, single operation	31.3	$^\circ\text{C/W}$

Notes:

- (1)When mounted on FR-4 board of 1inch², 2oz Cu, steady state



For the P-channel Power MOSFETs the actual polarity of the voltages and the current must be reversed.

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 4: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0, I_D = 250\ \mu\text{A}$	30			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0, V_{DS} = 30\text{ V}$			1	μA
		$V_{GS} = 0, V_{DS} = 30\text{ V}, T_C = 125\text{ °C}$			10	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0, V_{GS} = \pm 20\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1			V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 7\text{ A}$		0.009	0.0105	Ω
		$V_{GS} = 4.5\text{ V}, I_D = 7\text{ A}$		0.013	0.016	Ω

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}, f = 1\text{ MHz}, V_{GS} = 0$	-	3350	-	pF
C_{oss}	Output capacitance		-	414	-	pF
C_{rss}	Reverse transfer capacitance		-	287	-	pF
Q_g	Total gate charge	$V_{DD} = 15\text{ V}, I_D = 14\text{ A}, V_{GS} = 4.5\text{ V}$ (see Figure 14: "Gate charge test circuit")	-	33	-	nC
Q_{gs}	Gate-source charge		-	14	-	nC
Q_{gd}	Gate-drain charge		-	11	-	nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 15\text{ V}, I_D = 7\text{ A}, R_G = 4.7\ \Omega, V_{GS} = 10\text{ V}$ (see Figure 13: "Switching times test circuit for resistive load")	-	12.8	-	ns
t_r	Rise time		-	112	-	ns
$t_{d(off)}$	Turn-off delay time		-	61	-	ns
t_f	Fall time		-	45	-	ns



For the P-channel Power MOSFETs the actual polarity of the voltages and the current must be reversed.

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min	Typ	Max.	Unit
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 7 \text{ A}$, $V_{GS} = 0$	-		1.1	V
t_{rr}	Reverse recovery time	$I_{SD} = 24 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$	-	25.2		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 16 \text{ V}$, $T_j = 150 \text{ }^\circ\text{C}$	-	17.4		nC
I_{RRM}	Reverse recovery current	(see Figure 15: "Source-drain diode forward characteristics")	-	1.4		A

Notes:

⁽¹⁾Pulsed: pulse duration = 300 μs , duty cycle 1.5%



For the P-channel Power MOSFETs the actual polarity of the voltages and the current must be reversed.

2.2 Electrical characteristics (curves)

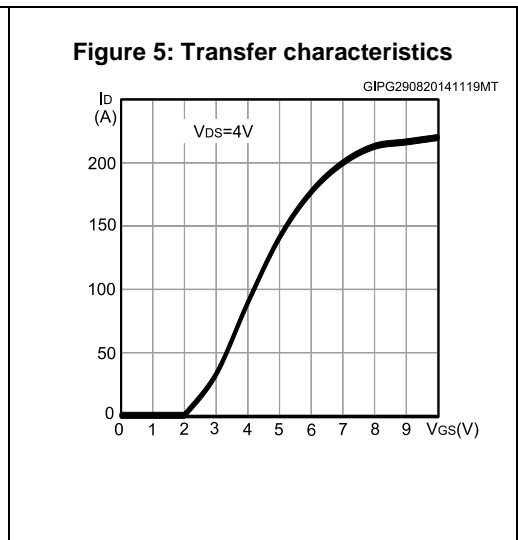
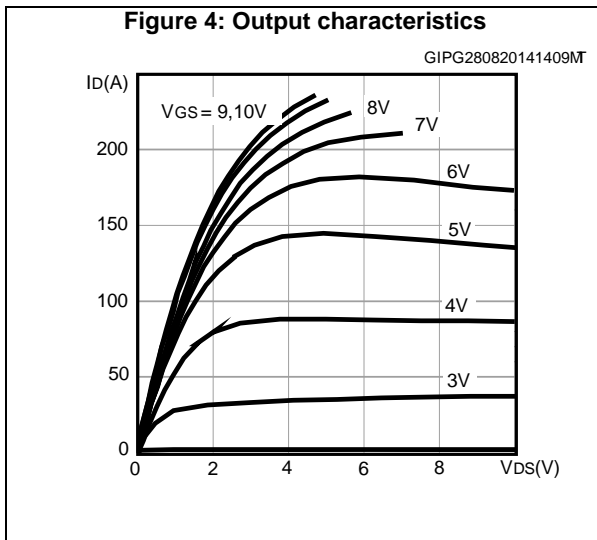
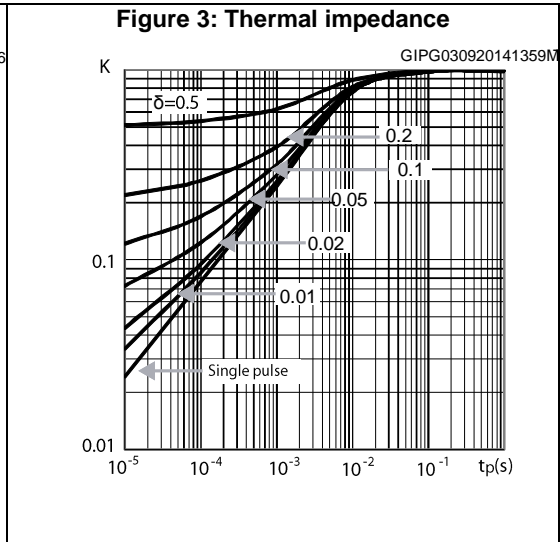
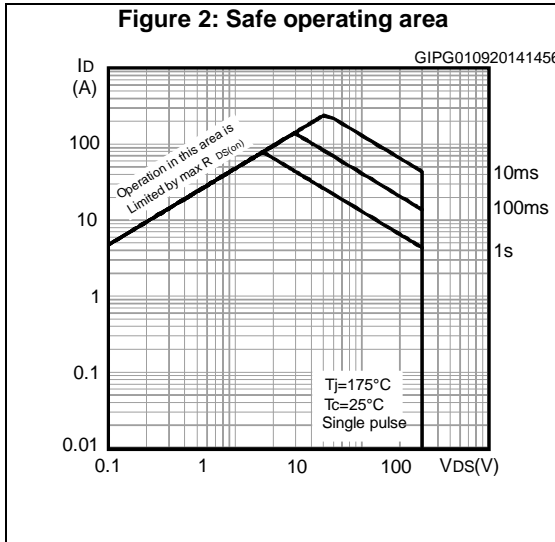


Figure 6: Gate charge vs gate-source voltage

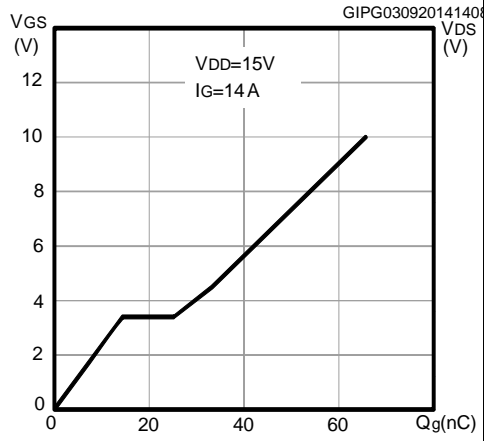


Figure 7: Static drain-source on-resistance

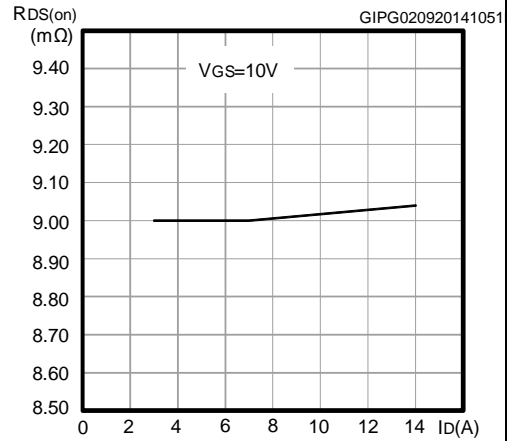


Figure 8: Capacitance variations

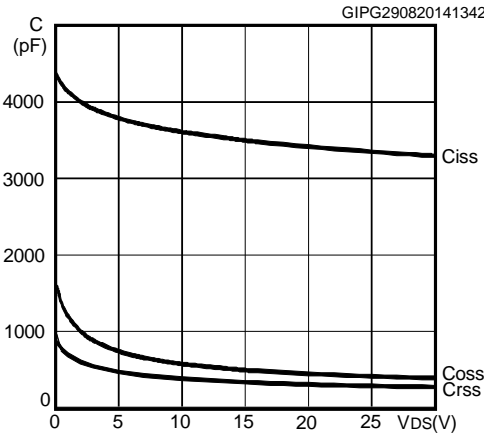


Figure 9: Normalized gate threshold voltage vs temperature

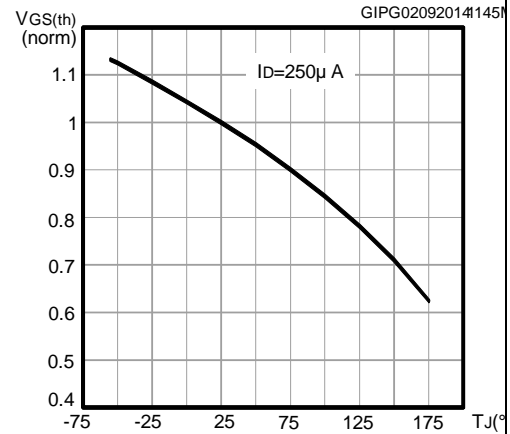


Figure 10: Normalized on-resistance vs temperature

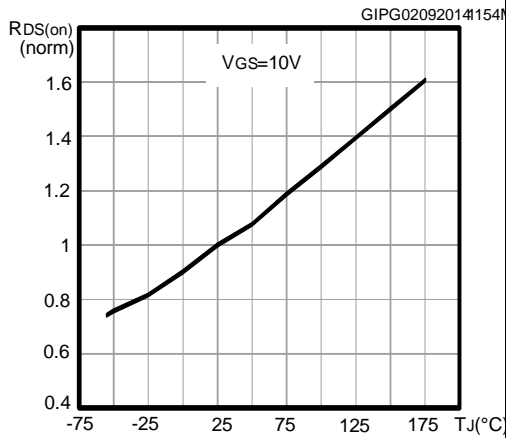


Figure 11: Normalized V(BR)DSS vs temperature

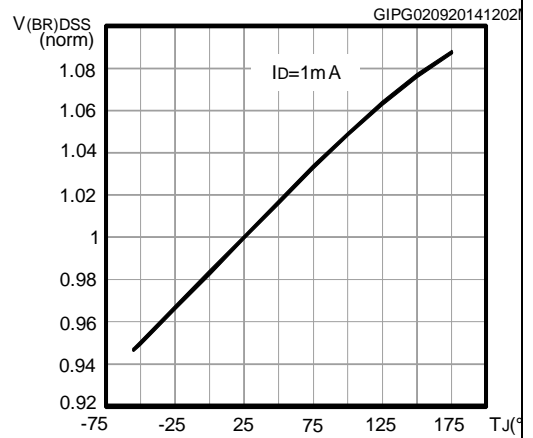
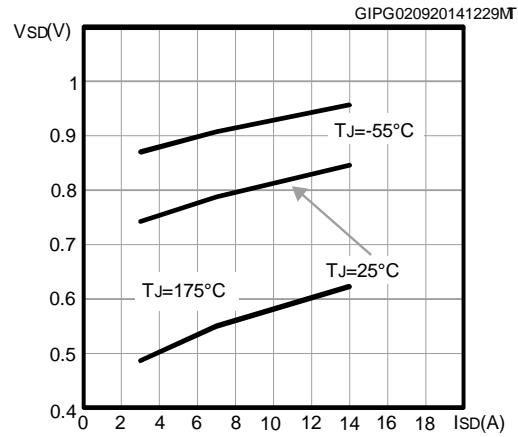


Figure 12: Source-drain diode forward characteristics



3 Test circuits

Figure 13: Switching times test circuit for resistive load

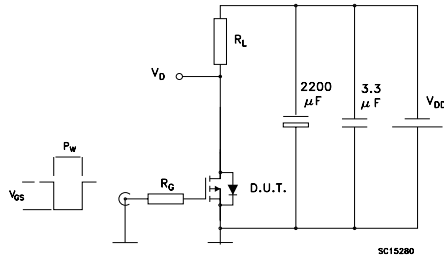


Figure 14: Gate charge test circuit

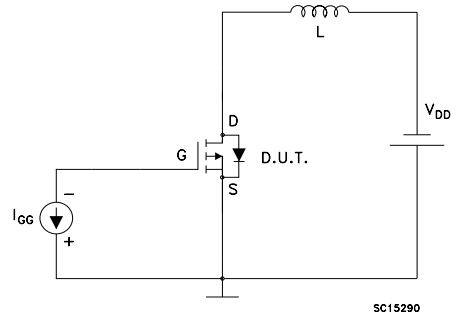
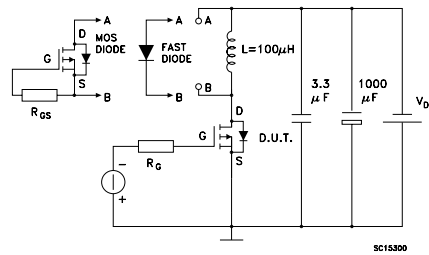


Figure 15: Source-drain diode forward characteristics



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 PowerFLAT 5x6 type S-R mechanical data

Figure 16: PowerFLAT™ 5x6 type S-R drawing

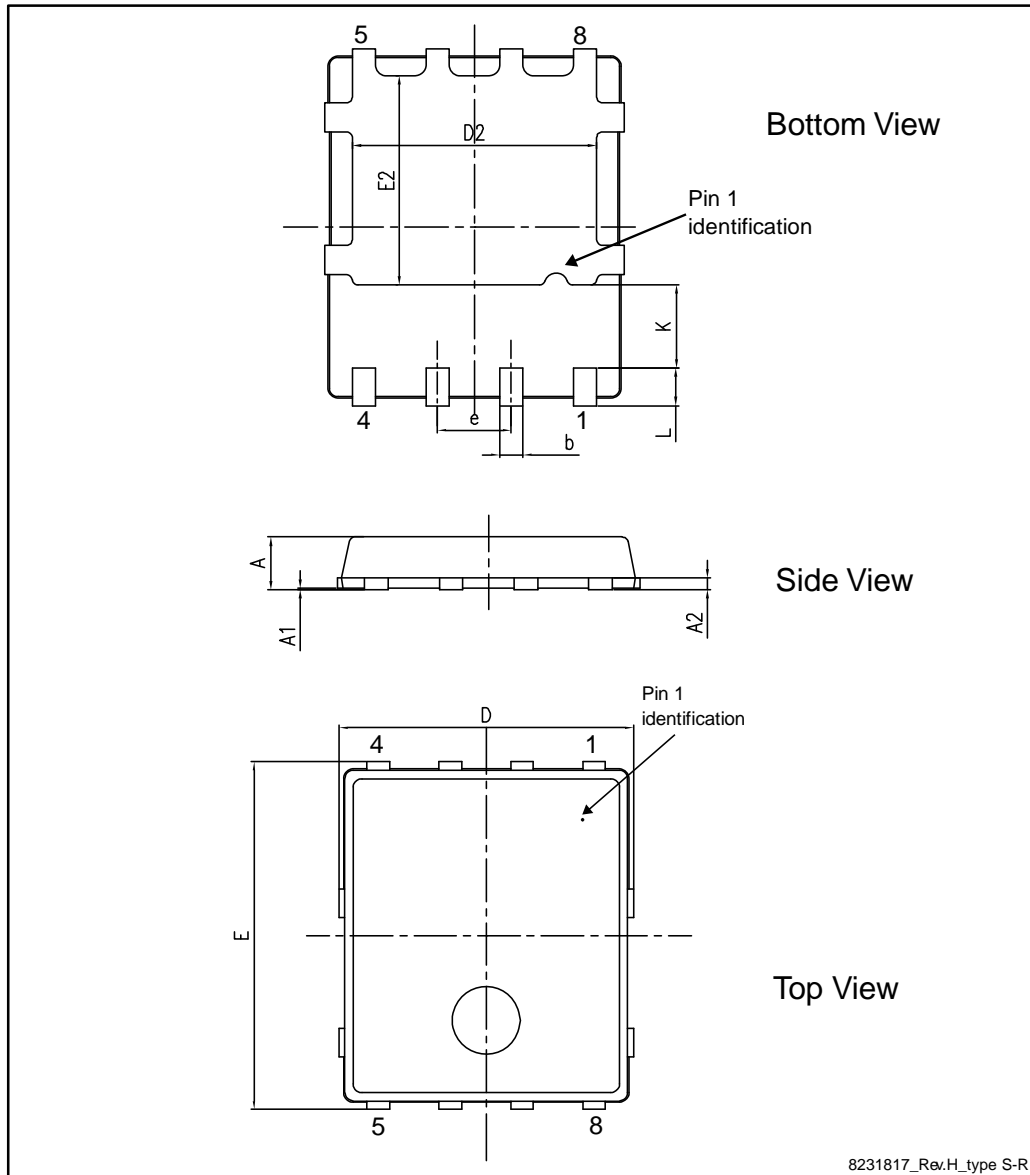
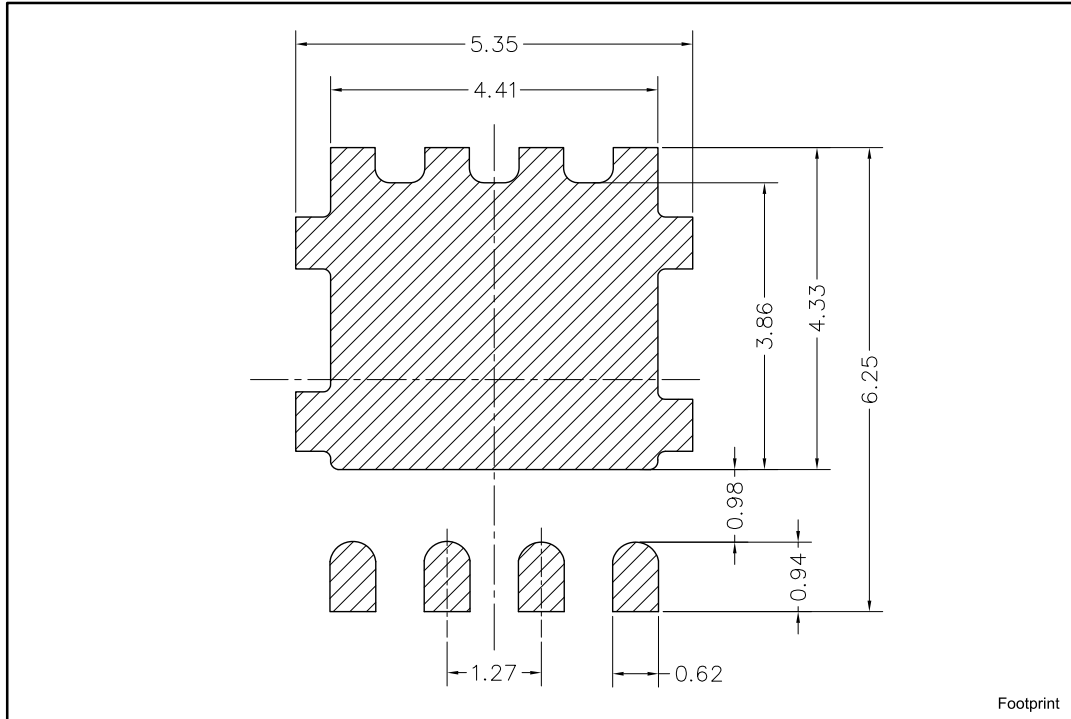


Table 8: PowerFLAT 5x6 type S-R mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D	5.00	5.20	5.40
E	5.95	6.15	6.35
D2	4.11		4.31
E2	3.50		3.70
e		1.27	
L	0.60		0.80
K	1.275		1.575

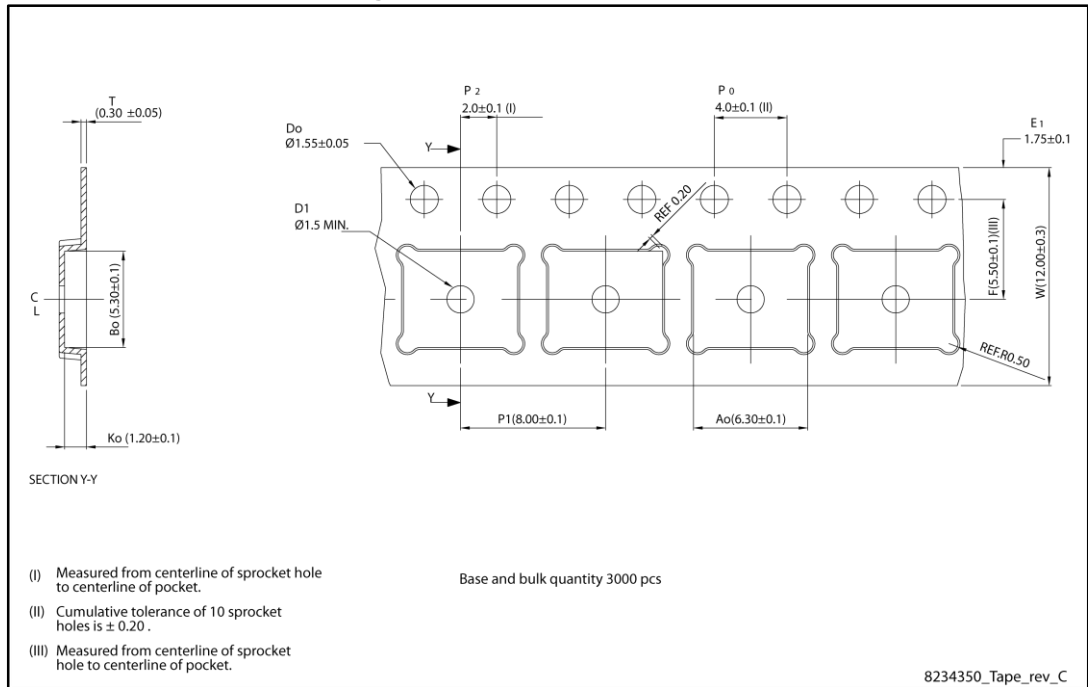
Figure 17: PowerFLAT™ 5x6 recommended footprint (dimensions are in mm)



5 Packaging mechanical data

5.1 PowerFLAT™ 5x6 tape

Figure 18: PowerFLAT™ 5x6 tape



All dimensions are in millimeters.

Figure 19: PowerFLAT™ 5x6 package orientation in carrier tape

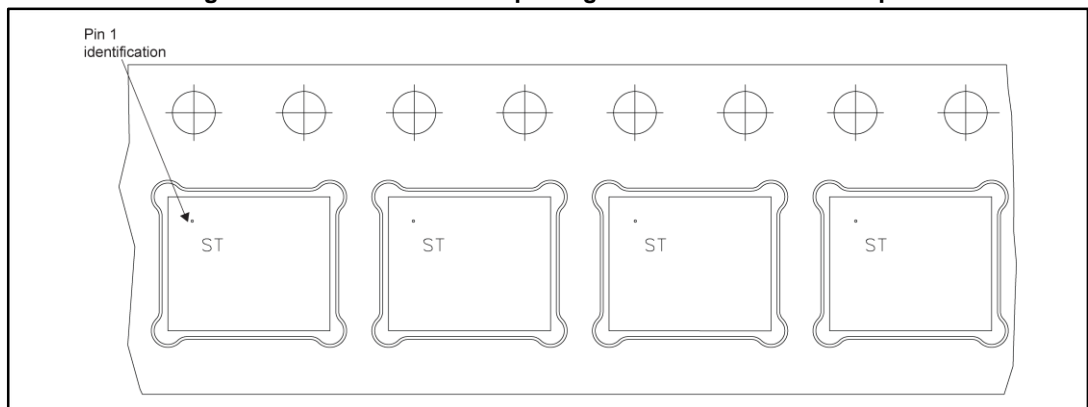
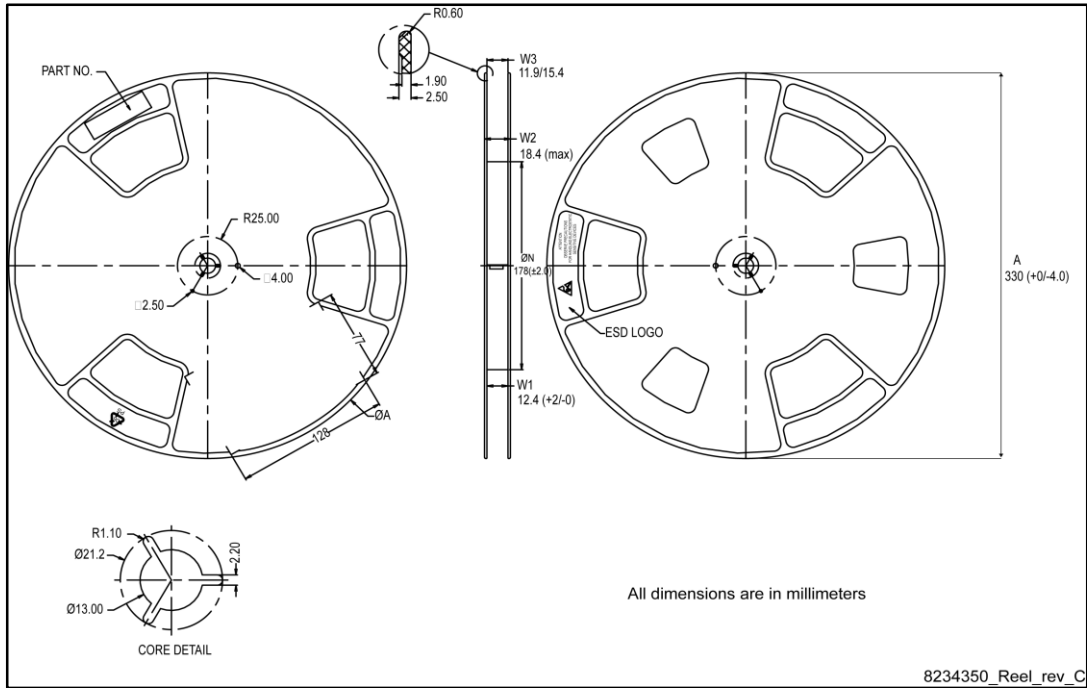


Figure 20: PowerFLAT™ 5x6 reel



6 Revision history

Table 9: Document revision history

Date	Revision	Changes
30-May-2014	1	First release.
05-Sep-2014	2	Updated the title, the features and the description in cover page. Updated Section 7: "Electrical characteristics" . Minor text changes.
11-Sep-2014	3	Updated Figure 6: "Gate charge vs gate-source voltage" . Minor text changes.
16-Dec-2014	4	Document status promoted from preliminary to production data.

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