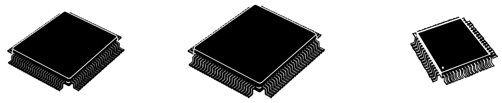
STM32F101xC STM32F101xD STM32F101xE

High-density access line, ARM-based 32-bit MCU with 256 to 512 KB Flash, 9 timers, 1 ADC and 10 communication interfaces

Features

- Core: ARM 32-bit Cortex™-M3 CPU
  - 36 MHz maximum frequency, 1.25 DMIPS/MHz (Dhrystone 2.1) performance
  - Single-cycle multiplication and hardware division
- Memories
  - 256 to 512 Kbytes of Flash memory
  - up to 48 Kbytes of SRAM
  - Flexible static memory controller with 4 Chip Select. Supports Compact Flash, SRAM, PSRAM, NOR and NAND memories
  - LCD parallel interface, 8080/6800 modes
- Clock, reset and supply management
  - 2.0 to 3.6 V application supply and I/Os
  - POR, PDR, and programmable voltage detector (PVD)
  - 4-to-16 MHz crystal oscillator
  - Internal 8 MHz factory-trimmed RC
  - Internal 40 kHz RC with calibration capability
  - 32 kHz oscillator for RTC with calibration
- Low power
  - Sleep, Stop and Standby modes
  - V_{BAT} supply for RTC and backup registers
- 1 x 12-bit, 1 µs A/D converters (up to 16 channels)
  - Conversion range: 0 to 3.6 V
  - Temperature sensor
- 2 × 12-bit D/A converters
- DMA
  - 12-channel DMA controller
  - Peripherals supported: timers, ADC, DAC, SPIs, I^2Cs and USARTs
- Up to 112 fast I/O ports



LQFP100 14 x 14 mm | LQFP144 20 x 20 mm | LQFP64 10 x 10 mm

  - 51/80/112 I/Os, all mappable on 16 external interrupt vectors and almost all 5 V-tolerant
- Debug mode
  - Serial wire debug (SWD) & JTAG interfaces
  - Cortex-M3 Embedded Trace Macrocell™
- Up to 9 timers
  - Up to four 16-bit timers, each with up to 4 IC/OC/PWM or pulse counter
  - 2 x watchdog timers (Independent and Window)
  - SysTick timer: a 24-bit downcounter
  - 2 × 16-bit basic timers to drive the DAC
- Up to 10 communication interfaces
  - Up to 2 x I^2C interfaces (SMBus/PMBus)
  - Up to 5 USARTs (ISO 7816 interface, LIN, IrDA capability, modem control)
  - Up to 3 SPIs (18 Mbit/s)
- CRC calculation unit, 96-bit unique ID
- ECOPACK® packages

Table 1. Device summary

Reference	Part number
STM32F101xC	STM32F101RC STM32F101VC STM32F101ZC
STM32F101xD	STM32F101RD STM32F101VD STM32F101ZD
STM32F101xE	STM32F101RE STM32F101ZE STM32F101VE

Contents

List of tables

List of figures

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F101xC, STM32F101xD and STM32F101xE high-density access line microcontrollers. For more details on the whole STMicroelectronics STM32F101xx family, please refer to *Section 2.2: Full compatibility throughout the family*.

The high-density STM32F101xx datasheet should be read in conjunction with the Medium- and high-density STM32F10xxx reference manual.
For information on programming, erasing and protection of the internal Flash memory please refer to the *STM32F10xxx Flash programming manual.*
The reference and Flash programming manuals are both available from the STMicroelectronics website www.st.com.

For information on the Cortex™-M3 core please refer to the Cortex™-M3 Technical Reference Manual, available from the www.arm.com website at the following address: http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ddi0337e/.

2 Description

The STM32F101xC, STM32F101xD and STM32F101xE access line family incorporates the high-performance ARM® Cortex™-M3 32-bit RISC core operating at a 36 MHz frequency, high-speed embedded memories (Flash memory up to 512 Kbytes and SRAM up to 48 Kbytes), and an extensive range of enhanced I/Os and peripherals connected to two APB buses. All devices offer one 12-bit ADC, four general-purpose 16-bit timers, as well as standard and advanced communication interfaces: up to two I^2Cs, three SPIs and five USARTs.

The STM32F101xx high-density access line family operates in the –40 to +85 °C temperature range, from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F101xx high-density access line family offers devices in 3 different package types: from 64 pins to 144 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

These features make the STM32F101xx high-density access line microcontroller family suitable for a wide range of applications:

- Medical and handheld equipment
- PC peripherals gaming and GPS platforms
- Industrial applications: PLC, printers, and scanners
- Alarm systems and Video intercom

Figure 1 shows the general block diagram of the device family.

2.1 Device overview

Table 2. STM32F101xC, STM32F101xD and STM32F101xE features and peripheral counts

Peripherals		STM32F101Rx			STM32F101Vx			STM32F101Zx		
Flash memory in Kbytes		256	384	512	256	384	512	256	384	512
SRAM in Kbytes		32	48		32	48		32	48	
FSMC		No			Yes[1]			Yes		
Timers	General-purpose	4								
	Basic	2								
Comm	SPI	3								
	I^2C	2								
	USART	5								
GPIOs		51			80			112		
12-bit ADC Number of channels		1 16			1 16			1 16		
12-bit DAC Number of channels		1 2								
CPU frequency		36 MHz								
Operating voltage		2.0 to 3.6 V								
Operating temperatures		Ambient temperature: –40 to +85 °C (see *Table 10*) Junction temperature: –40 to +105 °C (see *Table 10*)								
Package		LQFP64			LQFP100			LQFP144		

1. For the LQFP100 package, only FSMC Bank1 and Bank2 are available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select. Bank2 can only support a 16- or 8-bit NAND Flash memory using the NCE2 Chip Select. The interrupt line cannot be used since Port G is not available in this package.

2.2 Full compatibility throughout the family

The STM32F101xx is a complete family whose members are fully pin-to-pin, software and feature compatible. In the reference manual, the STM32F101x4 and STM32F101x6 are identified as low-density devices, the STM32F101x8 and STM32F101xB are referred to as medium-density devices, and the STM32F101xC, STM32F101xD and STM32F101xE are referred to as high-density devices.

Low- and high-density devices are an extension of the STM32F101x8/B medium-density devices, they are specified in the STM32F101x4/6 and STM32F101xC/D/E datasheets, respectively.

Low-density devices feature lower Flash memory and RAM capacities, less timers and peripherals. High-density devices have higher Flash memory and RAM densities, and additional peripherals like FSMC and DAC while remaining fully compatible with the other members of the family.

The STM32F101x4, STM32F101x6, STM32F101xC, STM32F101xD and STM32F101xE are a drop-in replacement for the STM32F101x8/B devices, allowing the user to try different memory densities and providing a greater degree of freedom during the development cycle.

Moreover, the STM32F101xx access line family is fully compatible with all existing STM32F103xx performance line and STM32F102xx USB access line devices.

Table 3. STM32F101xx family

<table>
<tr><th rowspan="4">Pinout</th><th colspan="7">Memory size</th></tr>
<tr><th colspan="2">Low-density devices</th><th colspan="2">Medium-density devices</th><th colspan="3">High-density devices</th></tr>
<tr><th>16 KB Flash</th><th>32 KB Flash(1)</th><th>64 KB Flash</th><th>128 KB Flash</th><th>256 KB Flash</th><th>384 KB Flash</th><th>512 KB Flash</th></tr>
<tr><th>4 KB RAM</th><th>6 KB RAM</th><th>10 KB RAM</th><th>16 KB RAM</th><th>32 KB RAM</th><th>48 KB RAM</th><th>48 KB RAM</th></tr>
<tr><td>144</td><td></td><td></td><td></td><td></td><td colspan="3" rowspan="3">5 × USARTs
4 × 16-bit timers, 2 × basic timers
3 × SPIs, 2 × I²Cs, 1 × ADC, 1 × DAC
FSMC (100 and 144 pins)</td></tr>
<tr><td>100</td><td></td><td></td><td colspan="2" rowspan="3">3 × USARTs
3 × 16-bit timers
2 × SPIs, 2 × I2Cs,
1 × ADC</td></tr>
<tr><td>64</td><td colspan="2" rowspan="3">2 × USARTs
2 × 16-bit timers
1 × SPI, 1 × I²C
1 × ADC</td></tr>
<tr><td>48</td><td></td><td></td><td></td></tr>
<tr><td>36</td><td></td><td></td><td></td><td></td><td></td></tr>
</table>

1. For orderable part numbers that do not show the A internal code after the temperature range code (6), the reference datasheet for electrical characteristics is that of the STM32F101x8/B medium-density devices.

2.3 Overview

2.3.1 ARM® Cortex™-M3 core with embedded Flash and SRAM

The ARM Cortex™-M3 processor is the latest generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM Cortex™-M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The STM32F101xC, STM32F101xD and STM32F101xE access line family having an embedded ARM core, is therefore compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the device family.

2.3.2 Embedded Flash memory

256 to 512 Kbytes of embedded Flash are available for storing programs and data.

2.3.3 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

2.3.4 Embedded SRAM

Up to 48 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states.

2.3.5 FSMC (flexible static memory controller)

The FSMC is embedded in the STM32F101xC, STM32F101xD and STM32F101xE access line family. It has four Chip Select outputs supporting the following modes: PC Card/Compact Flash, SRAM, PSRAM, NOR and NAND.

Functionality overview:

- The three FSMC interrupt lines are ORed in order to be connected to the NVIC
- No read FIFO
- Code execution from external memory except for NAND Flash and PC Card
- No boot capability
- The targeted frequency is HCLK/2, so external access is at 18 MHz when HCLK is at 36 MHz

2.3.6 LCD parallel interface

The FSMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost-effective graphic applications using LCD modules with embedded controllers or high-performance solutions using external controllers with dedicated acceleration.

2.3.7 Nested vectored interrupt controller (NVIC)

The STM32F101xC, STM32F101xD and STM32F101xE access line embeds a nested vectored interrupt controller able to handle up to 60 maskable interrupt channels (not including the 16 interrupt lines of Cortex™-M3) and 16 priority levels.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving* higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

2.3.8 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 19 edge detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 112 GPIOs can be connected to the 16 external interrupt lines.

2.3.9 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-16 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers are used to configure the AHB frequency, the high-speed APB (APB2) domain and the low-speed APB (APB1) domain. The maximum frequency of the AHB and APB domains is 36 MHz. See *Figure 2* for details on the clock tree.

2.3.10 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from User Flash
- Boot from System Memory
- Boot from embedded SRAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART1.

2.3.11 Power supply schemes

- V_{DD} = 2.0 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 2.0 to 3.6 V: external analog power supplies for ADC, Reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 2.4 V when the ADC is used). V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{BAT} = 1.8 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

For more details on how to connect power pins, refer to *Figure 9: Power supply scheme*.

2.3.12 Power supply supervisor

The device has an integrated power-on reset (POR)/power-down reset (PDR) circuitry. It is always active, and ensures proper operation starting from/down to 2 V. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software. Refer to *Table 12: Embedded reset and power control block characteristics* for the values of $V_{POR/PDR}$ and V_{PVD}.

2.3.13 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR) and power down.

- MR is used in the nominal regulation mode (Run)
- LPR is used in the Stop modes.
- Power down is used in Standby mode: the regulator output is in high impedance: the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost)

This regulator is always enabled after reset. It is disabled in Standby mode.

2.3.14 Low-power modes

The STM32F101xC, STM32F101xD and STM32F101xE access line supports three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.
- **Stop** mode

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low power mode.

The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output or the RTC alarm.

- **Standby** mode

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), a IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

2.3.15 DMA

The flexible 12-channel general-purpose DMAs (7 channels for DMA1 and 5 channels for DMA2) are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers.

The two DMA controllers support circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

DMA can be used with the main peripherals: SPI, I^2C, USART, general-purpose and basic timers TIMx, DAC and ADC.

2.3.16 RTC (real-time clock) and backup registers

The RTC and the backup registers are supplied through a switch that takes power either on V_{DD} supply when present or through the V_{BAT} pin. The backup registers are forty-two 16-bit registers used to store 84 bytes of user application data when V_{DD} power is not present. They are not reset by a system or power reset, and they are not reset when the device wakes up from the Standby mode.

The real-time clock provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and a periodic interrupt. It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low power RC oscillator or the high speed external clock divided by 128. The internal low-speed RC has a typical frequency of 40 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural quartz deviation. The RTC features a 32-bit programmable counter for long term measurement using the Compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

2.3.17 Timers and watchdogs

The high-density STM32F101xx access line devices include up to four general-purpose timers, two basic timers, two watchdog timers and a SysTick timer.

Table 4 compares the features of the general-purpose and basic timers.

Table 4. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TIM2, TIM3, TIM4, TIM5	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

General-purpose timers (TIMx)

There are up to 4 synchronizable general-purpose timers (TIM2, TIM3, TIM4 and TIM5) embedded in the STM32F101xC, STM32F101xD and STM32F101xE access line devices. These timers are based on a 16-bit auto-reload up/down counter, a 16-bit prescaler and feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input captures / output compares / PWMs on the largest packages.
The general-purpose timers can work together with the advanced-control timer via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs. They all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger generation. They can also be used as a generic 16-bit time base.

Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

2.3.18 I²C bus

Up to two I²C bus interfaces can operate in multi-master and slave modes. They support standard and fast modes.
They support 7/10-bit addressing mode and 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is embedded.
They can be served by DMA and they support SMBus 2.0/PMBus.

2.3.19 Universal synchronous/asynchronous receiver transmitters (USARTs)

The STM32F101xC, STM32F101xD and STM32F101xE access line embeds three universal synchronous/asynchronous receiver transmitters (USART1, USART2 and USART3) and two universal asynchronous receiver transmitters (UART4 and UART5).

These five interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability. The five interfaces are able to communicate at speeds of up to 2.25 Mbit/s.

USART1, USART2 and USART3 also provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller except for UART5.

2.3.20 Serial peripheral interface (SPI)

Up to three SPIs are able to communicate up to 18 Mbits/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

All SPIs can be served by the DMA controller.

2.3.21 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current-capable except for analog inputs.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

2.3.22 ADC (analog to digital converter)

A 12-bit analog-to-digital converter is embedded into STM32F101xC, STM32F101xD and STM32F101xE access line devices. It has up to 16 external channels, performing conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) can be internally connected to the ADC start trigger and injection trigger, respectively, to allow the application to synchronize A/D conversion and timers.

2.3.23 DAC (digital-to-analog converter)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- 8-bit or 12-bit monotonic output
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- external triggers for conversion
- input voltage reference V_{REF+}

Seven DAC trigger inputs are used in the STM32F101xC, STM32F101xD and STM32F101xE access line family. The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

2.3.24 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 2 V < V_{DDA} < 3.6 V. The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

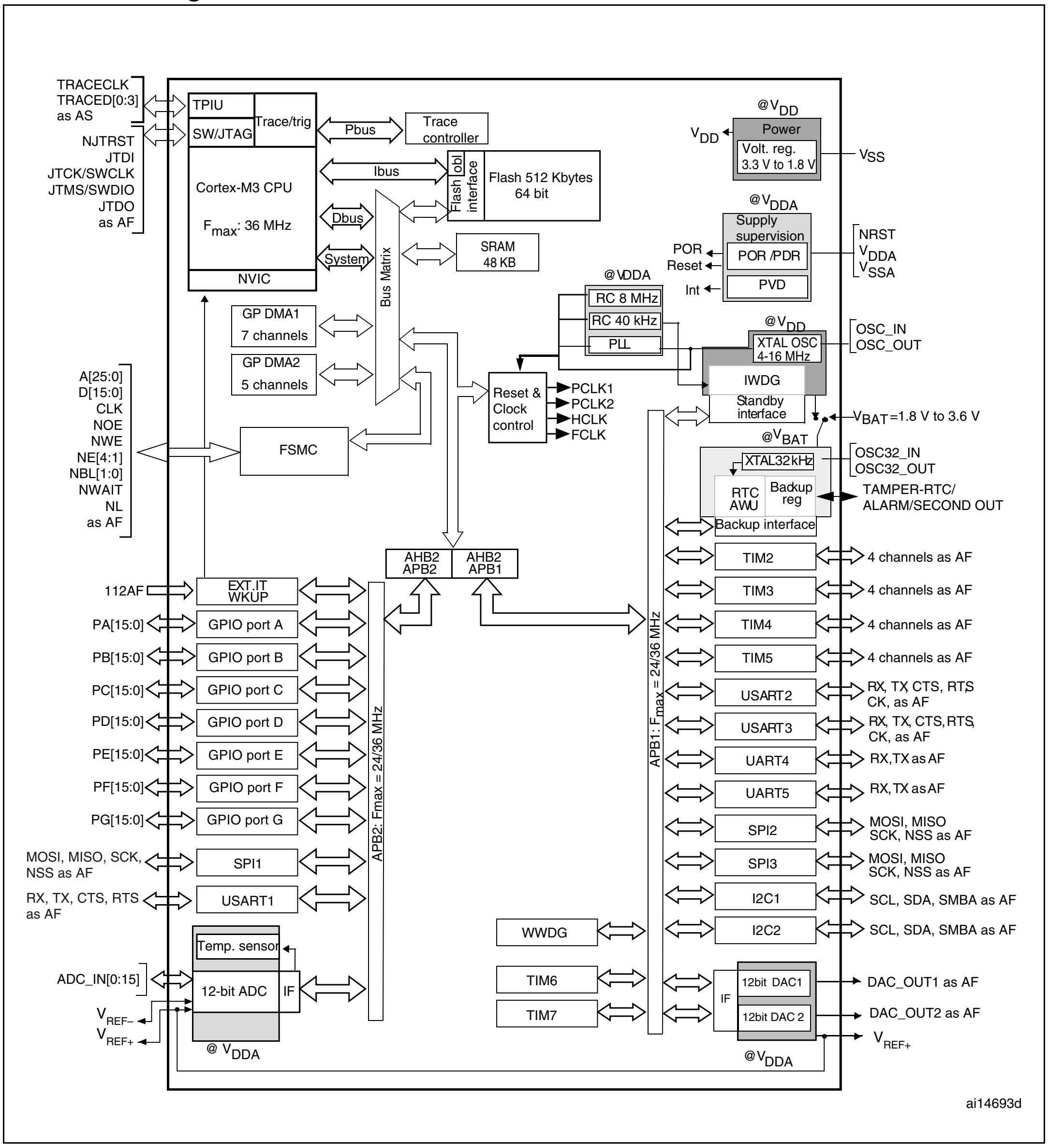
2.3.25 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

2.3.26 Embedded Trace Macrocell™

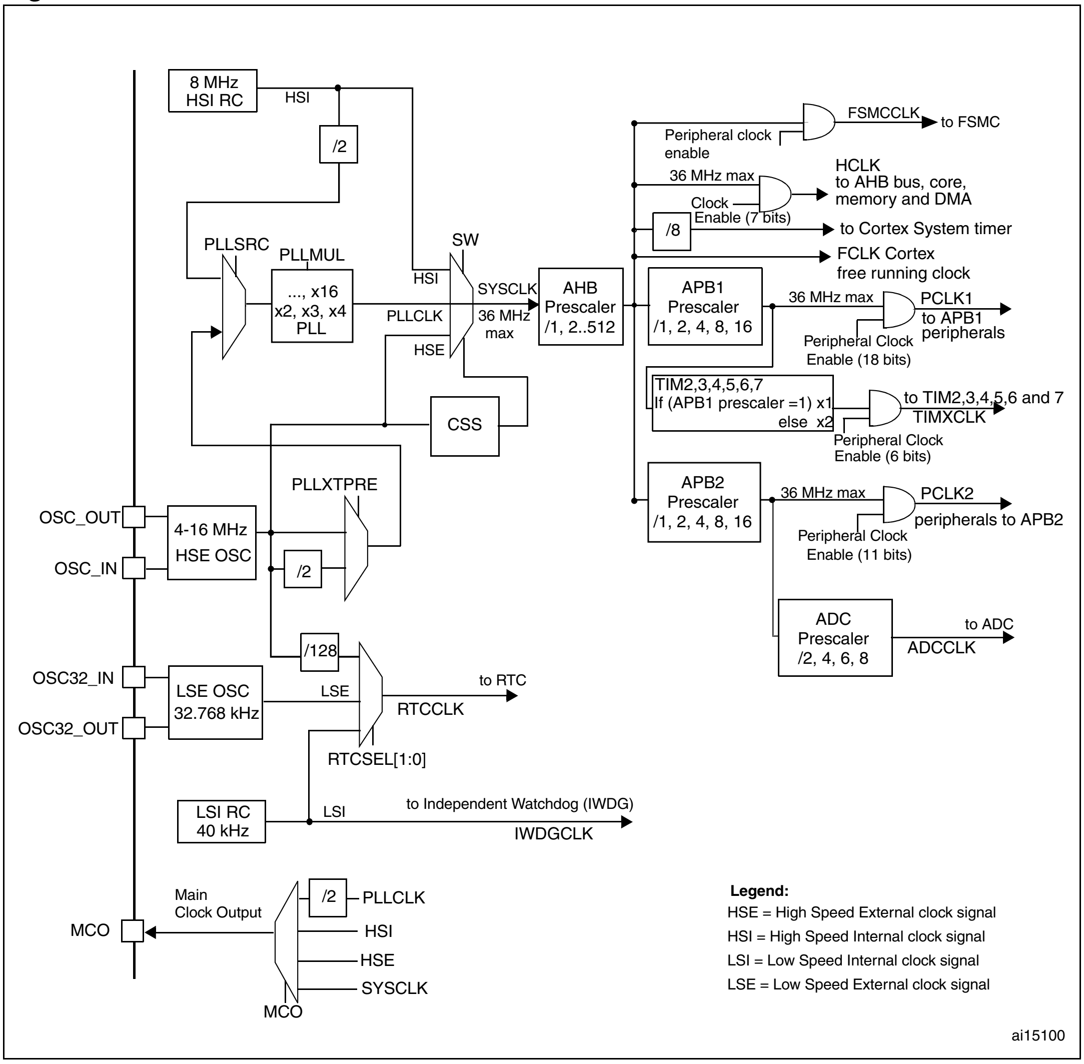
The ARM® Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F10xxx through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer running debugger software. TPA hardware is commercially available from common development tool vendors. It operates with third party debugger software tools.

Figure 1. STM32F101xC, STM32F101xD and STM32F101xE access line block diagram



1. T_A = –40 °C to +85 °C (junction temperature up to 105 °C).
2. AF = alternate function on I/O port pin.

Figure 2. Clock tree



1. When the HSI is used as a PLL clock input, the maximum system clock frequency that can be achieved is 36 MHz.
2. To have an ADC conversion time of 1 μs, APB2 must be at 14 MHz or 28 MHz.

3 Pinouts and pin descriptions

Figure 3. STM32F101xC, STM32F101xD and STM32F101xE access line LQFP144 pinout

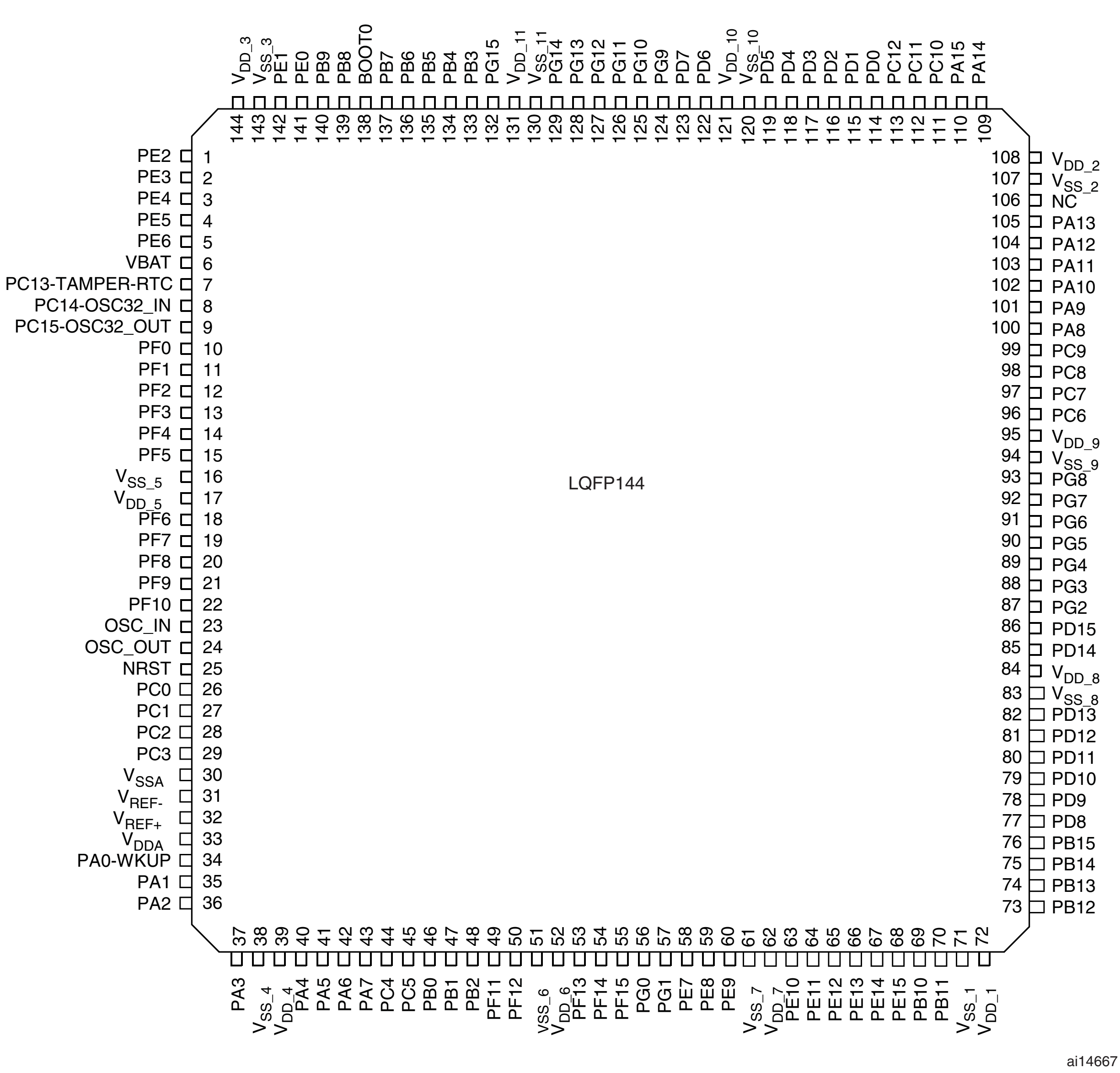


Figure 4. STM32F101xC, STM32F101xD and STM32F101xE access line LQFP100 pinout

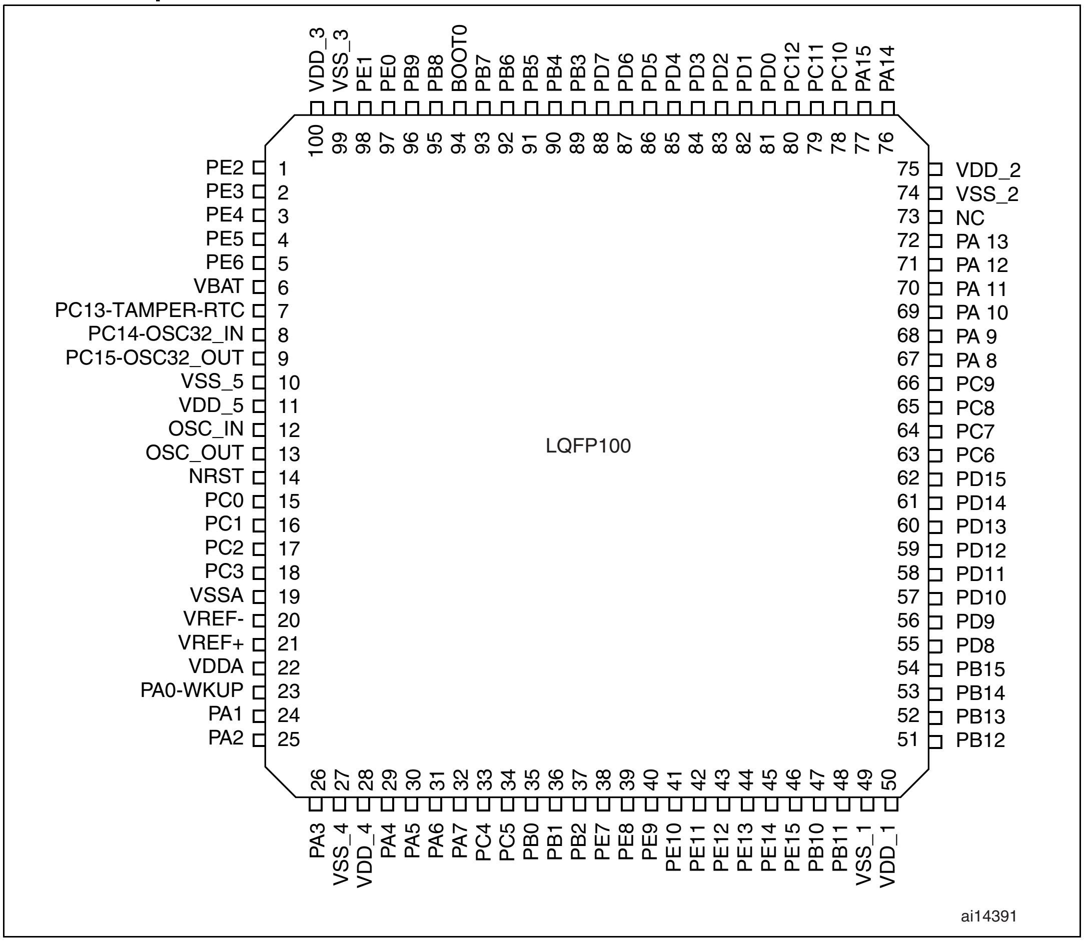


Figure 5. STM32F101xC, STM32F101xD and STM32F101xE access line LQFP64 pinout

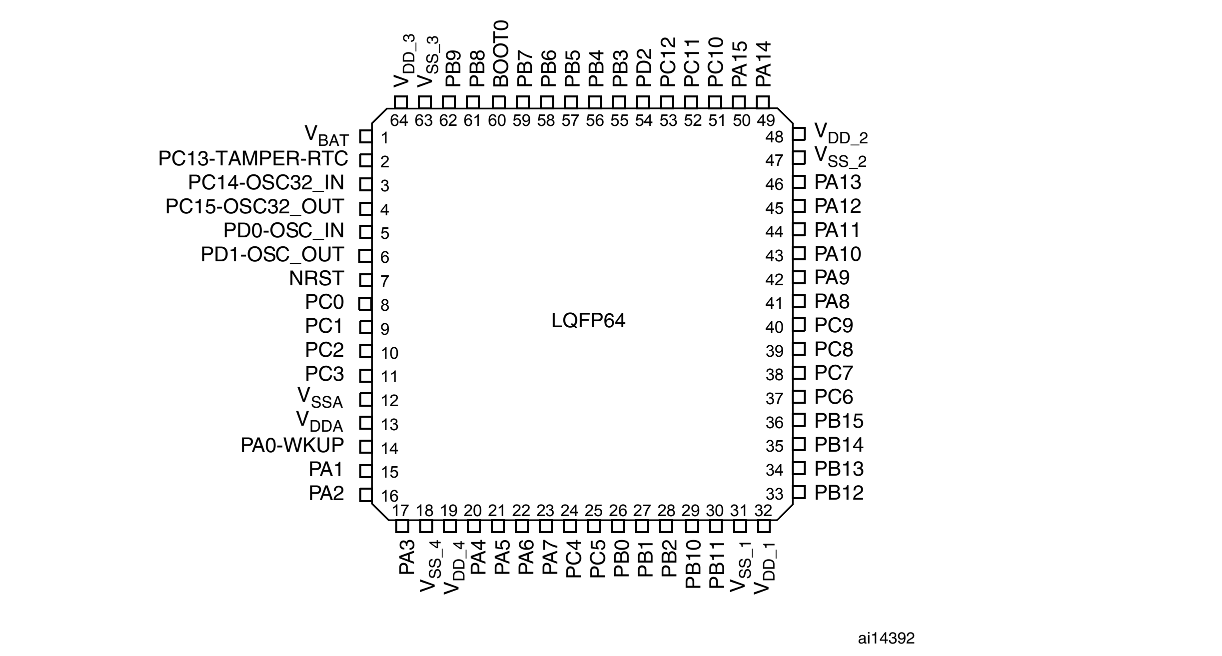


Table 5. High-density STM32F101xx pin definitions

Pins			Pin name	Type[1]	I / O Level[2]	Main function[3] (after reset)	Alternate functions	
LQFP64	LQFP100	LQFP144					Default	Remap
-	1	1	PE2	I/O	FT	PE2	TRACECLK/ FSMC_A23	
-	2	2	PE3	I/O	FT	PE3	TRACED0/FSMC_A19	
-	3	3	PE4	I/O	FT	PE4	TRACED1/FSMC_A20	
-	4	4	PE5	I/O	FT	PE5	TRACED2/FSMC_A21	
-	5	5	PE6	I/O	FT	PE6	TRACED3/FSMC_A22	
1	6	6	V_{BAT}	S		V_{BAT}		
2	7	7	PC13-TAMPER-RTC[4]	I/O		PC13[5]	TAMPER-RTC	
3	8	8	PC14-OSC32_IN[4]	I/O		PC14[5]	OSC32_IN	
4	9	9	PC15-OSC32_OUT[4]	I/O		PC15[5]	OSC32_OUT	
-	-	10	PF0	I/O	FT	PF0	FSMC_A0	
-	-	11	PF1	I/O	FT	PF1	FSMC_A1	
-	-	12	PF2	I/O	FT	PF2	FSMC_A2	
-	-	13	PF3	I/O	FT	PF3	FSMC_A3	
-	-	14	PF4	I/O	FT	PF4	FSMC_A4	
-	-	15	PF5	I/O	FT	PF5	FSMC_A5	
-	10	16	V_{SS_5}	S		V_{SS_5}		
-	11	17	V_{DD_5}	S		V_{DD_5}		

Table 5. High-density STM32F101xx pin definitions (continued)

Pins			Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions	
LQFP64	LQFP100	LQFP144					Default	Remap
-	-	18	PF6	I/O		PF6	FSMC_NIORD	
-	-	19	PF7	I/O		PF7	FSMC_NREG	
-	-	20	PF8	I/O		PF8	FSMC_NIOWR	
-	-	21	PF9	I/O		PF9	FSMC_CD	
-	-	22	PF10	I/O		PF10	FSMC_INTR	
5	12	23	OSC_IN	I		OSC_IN		
6	13	24	OSC_OUT	O		OSC_OUT		
7	14	25	NRST	I/O		NRST		
8	15	26	PC0	I/O		PC0	ADC_IN10	
9	16	27	PC1	I/O		PC1	ADC_IN11	
10	17	28	PC2	I/O		PC2	ADC_IN12	
11	18	29	PC3	I/O		PC3	ADC_IN13	
12	19	30	V_{SSA}	S		V_{SSA}		
-	20	31	V_{REF-}	S		V_{REF-}		
-	21	32	V_{REF+}	S		V_{REF+}		
13	22	33	V_{DDA}	S		V_{DDA}		
14	23	34	PA0-WKUP	I/O		PA0	WKUP/ USART2_CTS(6)/ ADC_IN0/TIM5_CH1/ TIM2_CH1_ETR(6)	
15	24	35	PA1	I/O		PA1	USART2_RTS(6)/ ADC_IN1/TIM5_CH2 TIM2_CH2(6)	
16	25	36	PA2	I/O		PA2	USART2_TX(6)/ TIM5_CH3/ADC_IN2/ TIM2_CH3(6)	
17	26	37	PA3	I/O		PA3	USART2_RX(6)/ TIM5_CH4 / ADC_IN3/ TIM2_CH4(6)	
18	27	38	V_{SS_4}	S		V_{SS_4}		
19	28	39	V_{DD_4}	S		V_{DD_4}		
20	29	40	PA4	I/O		PA4	SPI1_NSS/ DAC_OUT1 ADC_IN4 / USART2_CK(6)	
21	30	41	PA5	I/O		PA5	SPI1_SCK/ DAC_OUT2/ADC_IN5	
22	31	42	PA6	I/O		PA6	SPI1_MISO / ADC_IN6 / TIM3_CH1(6)	

Table 5. High-density STM32F101xx pin definitions (continued)

Pins			Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions	
LQFP64	LQFP100	LQFP144					Default	Remap
23	32	43	PA7	I/O		PA7	SPI1_MOSI / ADC_IN7/ TIM3_CH2(6)	
24	33	44	PC4	I/O		PC4	ADC_IN14	
25	34	45	PC5	I/O		PC5	ADC_IN15	
26	35	46	PB0	I/O		PB0	ADC_IN8 / TIM3_CH3(6)	
27	36	47	PB1	I/O		PB1	ADC_IN9/TIM3_CH4(6)	
28	37	48	PB2	I/O	FT	PB2/BOOT1		
-	-	49	PF11	I/O	FT	PF11	FSMC_NIOS16	
-	-	50	PF12	I/O	FT	PF12	FSMC_A6	
-	-	51	V_{SS_6}	S		V_{SS_6}		
-	-	52	V_{DD_6}	S		V_{DD_6}		
-	-	53	PF13	I/O	FT	PF13	FSMC_A7	
-	-	54	PF14	I/O	FT	PF14	FSMC_A8	
-	-	55	PF15	I/O	FT	PF15	FSMC_A9	
-	-	56	PG0	I/O	FT	PG0	FSMC_A10	
-	-	57	PG1	I/O	FT	PG1	FSMC_A11	
-	38	58	PE7	I/O	FT	PE7	FSMC_D4	
-	39	59	PE8	I/O	FT	PE8	FSMC_D5	
-	40	60	PE9	I/O	FT	PE9	FSMC_D6	
-	-	61	V_{SS_7}	S		V_{SS_7}		
-	-	62	V_{DD_7}	S		V_{DD_7}		
-	41	63	PE10	I/O	FT	PE10	FSMC_D7	
-	42	64	PE11	I/O	FT	PE11	FSMC_D8	
-	43	65	PE12	I/O	FT	PE12	FSMC_D9	
-	44	66	PE13	I/O	FT	PE13	FSMC_D10	
-	45	67	PE14	I/O	FT	PE14	FSMC_D11	
-	46	68	PE15	I/O	FT	PE15	FSMC_D12	
29	47	69	PB10	I/O	FT	PB10	I2C2_SCL/ USART3_TX(6)	TIM2_CH3
30	48	70	PB11	I/O	FT	PB11	I2C2_SDA/ USART3_RX(6)	TIM2_CH4
31	49	71	V_{SS_1}	S		V_{SS_1}		
32	50	72	V_{DD_1}	S		V_{DD_1}		
33	51	73	PB12	I/O	FT	PB12	SPI2_NSS(6)/ I2C2_SMBAI USART3_CK(6)	

Table 5. High-density STM32F101xx pin definitions (continued)

Pins			Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions	
LQFP64	LQFP100	LQFP144					Default	Remap
34	52	74	PB13	I/O	FT	PB13	SPI2_SCK(6)/ USART3_CTS(6)	
35	53	75	PB14	I/O	FT	PB14	SPI2_MISO(6)/ USART3_RTS(6)	
36	54	76	PB15	I/O	FT	PB15	SPI2_MOSI(6)	
-	55	77	PD8	I/O	FT	PD8	FSMC_D13	USART3_TX
-	56	78	PD9	I/O	FT	PD9	FSMC_D14	USART3_RX
-	57	79	PD10	I/O	FT	PD10	FSMC_D15	USART3_CK
-	58	80	PD11	I/O	FT	PD11	FSMC_A16	USART3_CTS
-	59	81	PD12	I/O	FT	PD12	FSMC_A17	TIM4_CH1 / USART3_RTS
-	60	82	PD13	I/O	FT	PD13	FSMC_A18	TIM4_CH2
-	-	83	V_{SS_8}	S		V_{SS_8}		
-	-	84	V_{DD_8}	S		V_{DD_8}		
-	61	85	PD14	I/O	FT	PD14	FSMC_D0	TIM4_CH3
-	62	86	PD15	I/O	FT	PD15	FSMC_D1	TIM4_CH4
-	-	87	PG2	I/O	FT	PG2	FSMC_A12	
-	-	88	PG3	I/O	FT	PG3	FSMC_A13	
-	-	89	PG4	I/O	FT	PG4	FSMC_A14	
-	-	90	PG5	I/O	FT	PG5	FSMC_A15	
-	-	91	PG6	I/O	FT	PG6	FSMC_INT2	
-	-	92	PG7	I/O	FT	PG7	FSMC_INT3	
-	-	93	PG8	I/O	FT	PG8		
-	-	94	V_{SS_9}	S		V_{SS_9}		
-	-	95	V_{DD_9}	S		V_{DD_9}		
37	63	96	PC6	I/O	FT	PC6		TIM3_CH1
38	64	97	PC7	I/O	FT	PC7		TIM3_CH2
39	65	98	PC8	I/O	FT	PC8		TIM3_CH3
40	66	99	PC9	I/O	FT	PC9		TIM3_CH4
41	67	100	PA8	I/O	FT	PA8	USART1_CK/ MCO	
42	68	101	PA9	I/O	FT	PA9	USART1_TX(6)	
43	69	102	PA10	I/O	FT	PA10	USART1_RX(6)	
44	70	103	PA11	I/O	FT	PA11	USART1_CTS	

Table 5. High-density STM32F101xx pin definitions (continued)

Pins			Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions	
LQFP64	LQFP100	LQFP144					Default	Remap
45	71	104	PA12	I/O	FT	PA12	USART1_RTS	
46	72	105	PA13	I/O	FT	JTMS-SWDIO		PA13
-	73	106	Not connected					
47	74	107	V_{SS_2}	S		V_{SS_2}		
48	75	108	V_{DD_2}	S		V_{DD_2}		
49	76	109	PA14	I/O	FT	JTCK-SWCLK		PA14
50	77	110	PA15	I/O	FT	JTDI	SPI3_NSS	TIM2_CH1_ETR/ PA15 /SPI1_NSS
51	78	111	PC10	I/O	FT	PC10	UART4_TX	USART3_TX
52	79	112	PC11	I/O	FT	PC11	UART4_RX	USART3_RX
53	80	113	PC12	I/O	FT	PC12	UART5_TX	USART3_CK
5	81	114	PD0	I/O	FT	OSC_IN(7)	FSMC_D2(8)	
6	82	115	PD1	I/O	FT	OSC_OUT(7)	FSMC_D3(8)	
54	83	116	PD2	I/O	FT	PD2	TIM3_ETR/UART5_RX	
-	84	117	PD3	I/O	FT	PD3	FSMC_CLK	USART2_CTS
-	85	118	PD4	I/O	FT	PD4	FSMC_NOE	USART2_RTS
-	86	119	PD5	I/O	FT	PD5	FSMC_NWE	USART2_TX
-	-	120	V_{SS_10}	S		V_{SS_10}		
-	-	121	V_{DD_10}	S		V_{DD_10}		
-	87	122	PD6	I/O	FT	PD6	FSMC_NWAIT	USART2_RX
-	88	123	PD7	I/O	FT	PD7	FSMC_NE1/ FSMC_NCE2	USART2_CK
-	-	124	PG9	I/O	FT	PG9	FSMC_NE2/ FSMC_NCE3	
-	-	125	PG10	I/O	FT	PG10	FSMC_NE3/ FSMC_NCE4_1	
-	-	126	PG11	I/O	FT	PG11	FSMC_NCE4_2	
-	-	127	PG12	I/O	FT	PG12	FSMC_NE4	
-	-	128	PG13	I/O	FT	PG13	FSMC_A24	
-	-	129	PG14	I/O	FT	PG14	FSMC_A25	
-	-	130	V_{SS_11}	S		V_{SS_11}		
-	-	131	V_{DD_11}	S		V_{DD_11}		
-	-	132	PG15	I/O	FT	PG15		

Table 5. High-density STM32F101xx pin definitions (continued)

Pins			Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions	
LQFP64	LQFP100	LQFP144					Default	Remap
55	89	133	PB3	I/O	FT	JTDO	SPI3_SCK	TIM2_CH2 /PB3 TRACESWO SPI1_SCK
56	90	134	PB4	I/O	FT	NJTRST	SPI3_MISO	PB4 / TIM3_CH1 SPI1_MISO
57	91	135	PB5	I/O		PB5	I2C1_SMBAI/ SPI3_MOSI	TIM3_CH2 / SPI1_MOSI
58	92	136	PB6	I/O	FT	PB6	I2C1_SCL/ TIM4_CH1(6)	USART1_TX
59	93	137	PB7	I/O	FT	PB7	I2C1_SDA/FSMC_NADV TIM4_CH2(6)	USART1_RX
60	94	138	BOOT0	I		BOOT0		
61	95	139	PB8	I/O	FT	PB8	TIM4_CH3 (6)	I2C1_SCL
62	96	140	PB9	I/O	FT	PB9	TIM4_CH4 (6)	I2C1_SDA
-	97	141	PE0	I/O	FT	PE0	TIM4_ETR(6)/ FSMC_NBL0	
-	98	142	PE1	I/O	FT	PE1	FSMC_NBL1	
63	99	143	V_{SS_3}	S		V_{SS_3}		
64	100	144	V_{DD_3}	S		V_{DD_3}		

1. I = input, O = output, S = supply, HiZ = high impedance.
2. FT = 5 V tolerant.
3. Function availability depends on the chosen device.
4. PC13, PC14 and PC15 are supplied through the power switch and since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 is restricted: only one I/O at a time can be used as an output, the speed has to be limited to 2 MHz with a maximum load of 30 pF and these I/Os must not be used as a current source (e.g. to drive an LED).
5. Main function after the first backup domain power-up. Later on, it depends on the contents of the Backup registers even after reset (because these registers are not reset by the main reset). For details on how to manage these IOs, refer to the Battery backup domain and BKP register description sections in the STM32F10xxx reference manual, available from the STMicroelectronics website: www.st.com.
6. This alternate function can be remapped by software to some other port pins (if available on the used package). For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual, available from the STMicroelectronics website: www.st.com.
7. For the LQFP64 package, the pins number 5 and 6 are configured as OSC_IN/OSC_OUT after reset, however the functionality of PD0 and PD1 can be remapped by software on these pins. For the LQFP100 and LQFP144 packages, PD0 and PD1 are available by default, so there is no need for remapping. For more details, refer to Alternate function I/O and debug configuration section in the STM32F10xxx reference manual
8. For devices delivered in LQFP64 packages, the FSMC function is not available.

Table 6. FSMC pin definition

Pins	FSMC					LQFP100 BGA100[1]
	CF	CF/IDE	NOR/PSRAM/ SRAM	NOR/PSRAM Mux	NAND 16 bit	
PE2			A23	A23		Yes
PE3			A19	A19		Yes
PE4			A20	A20		Yes
PE5			A21	A21		Yes
PE6			A22	A22		Yes
PF0	A0	A0	A0			-
PF1	A1	A1	A1			-
PF2	A2	A2	A2			-
PF3	A3		A3			-
PF4	A4		A4			-
PF5	A5		A5			-
PF6	NIORD	NIORD				-
PF7	NREG	NREG				-
PF8	NIOWR	NIOWR				-
PF9	CD	CD				-
PF10	INTR	INTR				-
PF11	NIOS16	NIOS16				-
PF12	A6		A6			-
PF13	A7		A7			-
PF14	A8		A8			-
PF15	A9		A9			-
PG0	A10		A10			-
PG1			A11			-
PE7	D4	D4	D4	DA4	D4	Yes
PE8	D5	D5	D5	DA5	D5	Yes
PE9	D6	D6	D6	DA6	D6	Yes
PE10	D7	D7	D7	DA7	D7	Yes
PE11	D8	D8	D8	DA8	D8	Yes
PE12	D9	D9	D9	DA9	D9	Yes
PE13	D10	D10	D10	DA10	D10	Yes
PE14	D11	D11	D11	DA11	D11	Yes
PE15	D12	D12	D12	DA12	D12	Yes
PD8	D13	D13	D13	DA13	D13	Yes

Table 6. FSMC pin definition (continued)

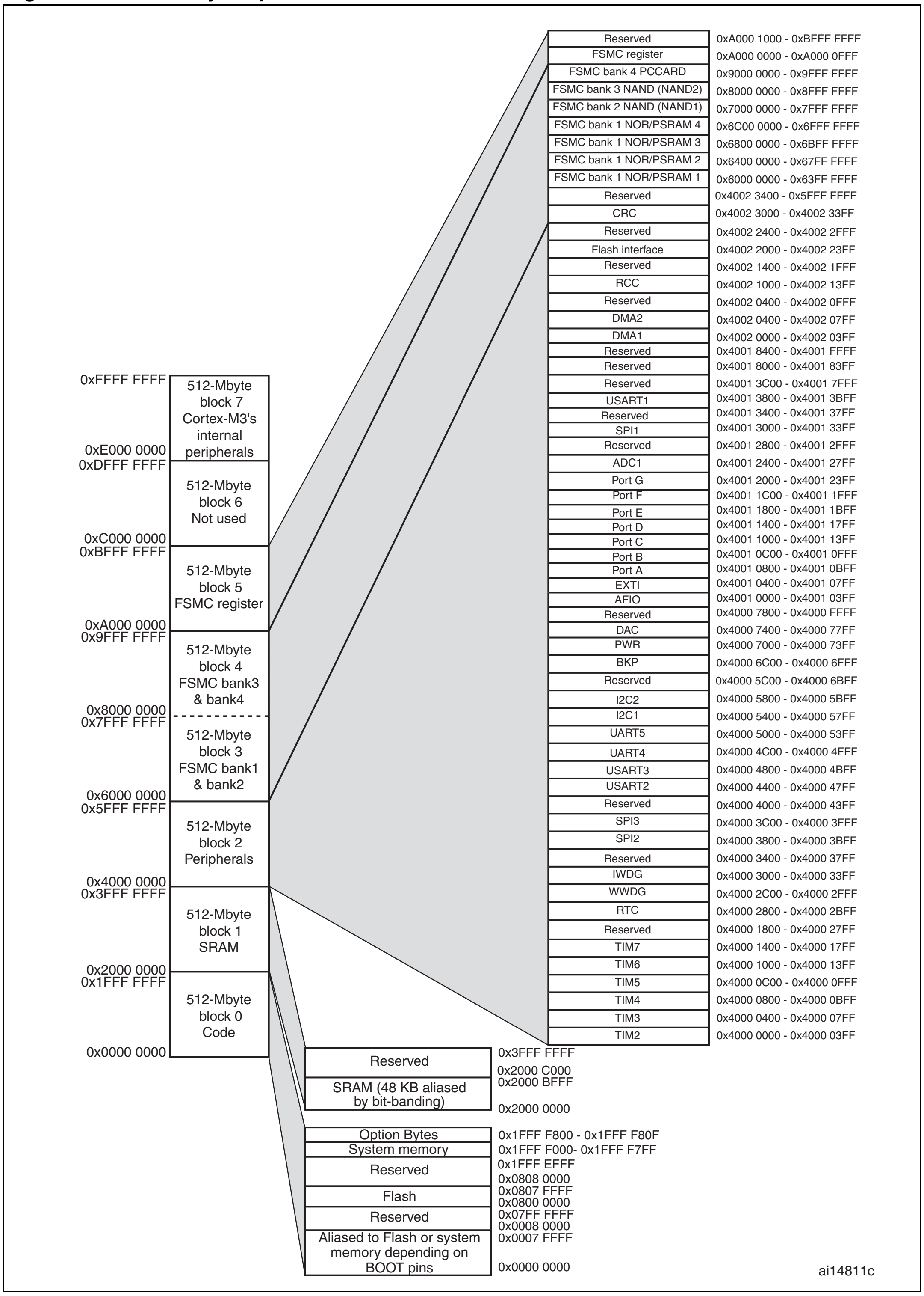
Pins	FSMC					LQFP100 BGA100[(1)]
	CF	CF/IDE	NOR/PSRAM/ SRAM	NOR/PSRAM Mux	NAND 16 bit	
PD9	D14	D14	D14	DA14	D14	Yes
PD10	D15	D15	D15	DA15	D15	Yes
PD11			A16	A16	CLE	Yes
PD12			A17	A17	ALE	Yes
PD13			A18	A18		Yes
PD14	D0	D0	D0	DA0	D0	Yes
PD15	D1	D1	D1	DA1	D1	Yes
PG2			A12			-
PG3			A13			-
PG4			A14			-
PG5			A15			-
PG6					INT2	-
PG7					INT3	-
PD0	D2	D2	D2	DA2	D2	Yes
PD1	D3	D3	D3	DA3	D3	Yes
PD3			CLK	CLK		Yes
PD4	NOE	NOE	NOE	NOE	NOE	Yes
PD5	NWE	NWE	NWE	NWE	NWE	Yes
PD6	NWAIT	NWAIT	NWAIT	NWAIT	NWAIT	Yes
PD7			NE1	NE1	NCE2	Yes
PG9			NE2	NE2	NCE3	-
PG10	NCE4_1	NCE4_1	NE3	NE3		-
PG11	NCE4_2	NCE4_2				-
PG12			NE4	NE4		-
PG13			A24	A24		-
PG14			A25	A25		-
PB7			NADV	NADV		Yes
PE0			NBL0	NBL0		Yes
PE1			NBL1	NBL1		Yes

1. Ports F and G are not available in devices delivered in 100-pin packages.

4 Memory mapping

The memory map is shown in *Figure 6*.

Figure 6. Memory map



5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.3 V (for the 2 V ≤V_{DD} ≤3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2Σ).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 7*.

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 8*.

Figure 7. Pin loading conditions

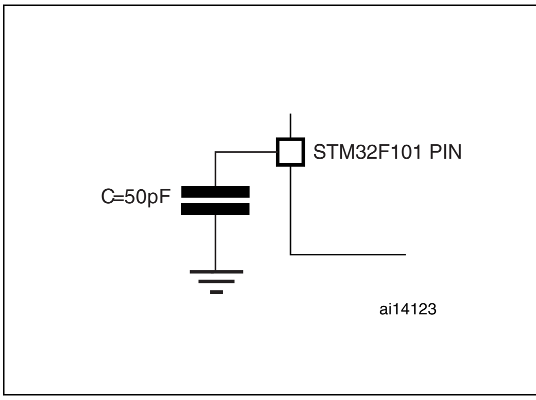
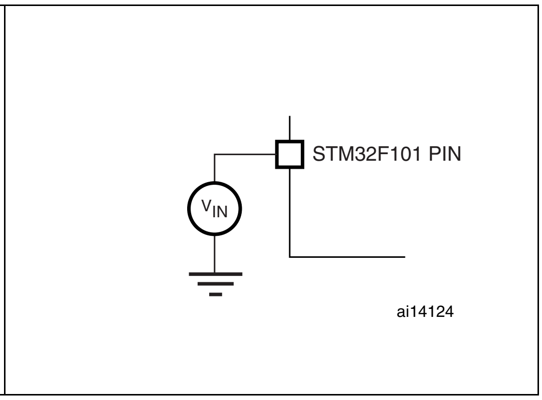
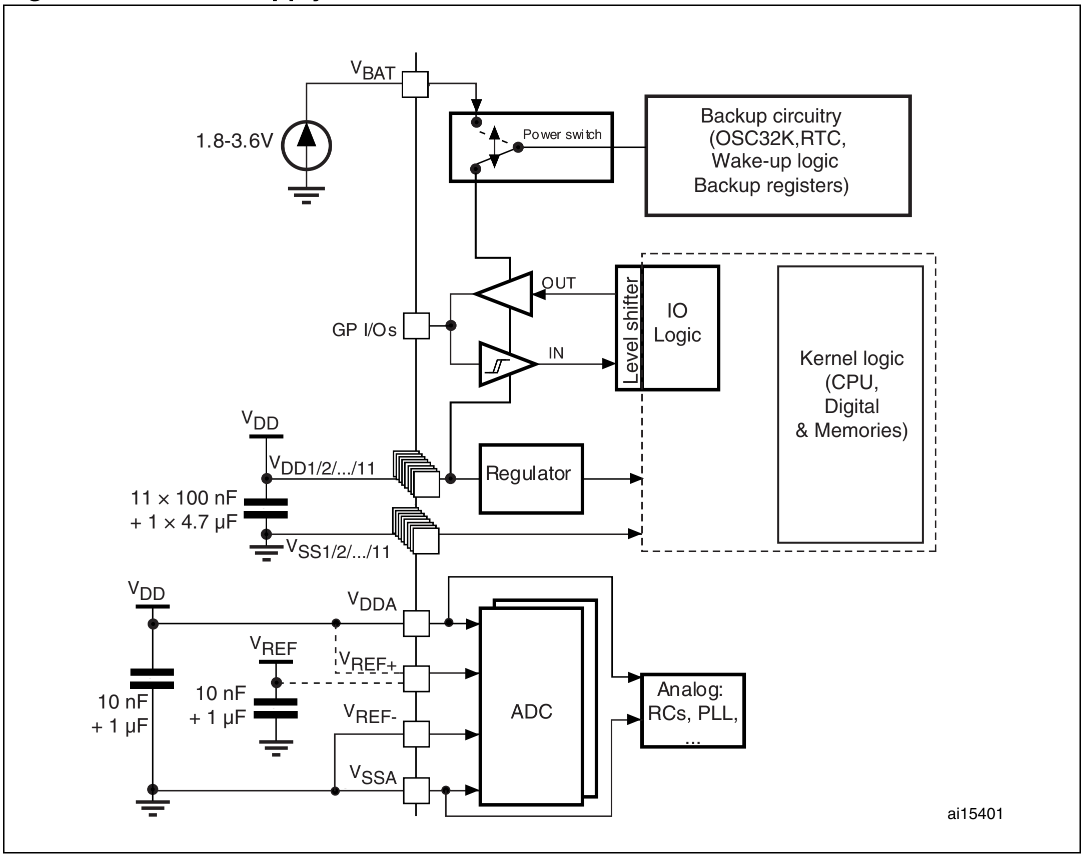


Figure 8. Pin input voltage



5.1.6 Power supply scheme

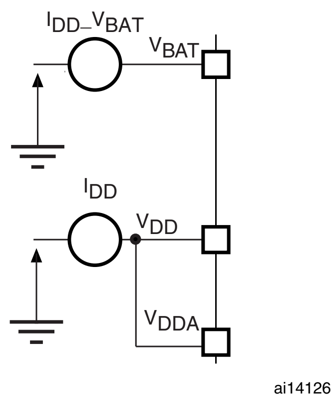
Figure 9. Power supply scheme



Caution: In *Figure 9*, the 4.7 µF capacitor must be connected to V_{DD3}.

5.1.7 Current consumption measurement

Figure 10. Current consumption measurement scheme



5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 7: Voltage characteristics*, *Table 8: Current characteristics*, and *Table 9: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 7. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
$V_{DD}-V_{SS}$	External main supply voltage (including V_{DDA} and V_{DD})(1)	–0.3	4.0	V
V_{IN}	Input voltage on five volt tolerant pin(2)	$V_{SS}-0.3$	+5.5	
	Input voltage on any other pin(2)	$V_{SS}-0.3$	$V_{DD}+0.3$	
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DD} power pins		50	mV
$\lvert V_{SSX}-V_{SS}\rvert$	Variations between all the different ground pins		50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 5.3.12: Absolute maximum ratings (electrical sensitivity)*		

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. $I_{INJ(PIN)}$ must never be exceeded (see *Table 8: Current characteristics*). This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{IN}$max while a negative injection is induced by $V_{IN}<V_{SS}$.

Table 8. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} power lines (source)[1]	150	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)[1]	150	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	–25	
$I_{INJ(PIN)}$ [2][3]	Injected current on NRST pin	± 5	
	Injected current on High-speed external OSC_IN and Low-speed external OSC_IN pins	± 5	
	Injected current on any other pin[4]	± 5	
$\Sigma I_{INJ(PIN)}$[2]	Total injected current (sum of all I/O and control pins)[4]	± 25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$.
3. Negative injection disturbs the analog performance of the device. See note in *Section 5.3.17: 12-bit ADC characteristics*.
4. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

Table 9. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

5.3 Operating conditions

5.3.1 General operating conditions

Table 10. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency		0	36	MHz
f_{PCLK1}	Internal APB1 clock frequency		0	36	
f_{PCLK2}	Internal APB2 clock frequency		0	36	
V_{DD}	Standard operating voltage		2	3.6	V
V_{DDA}(1)	Analog operating voltage (ADC not used)	Must be the same potential as V_{DD}(2)	2	3.6	V
	Analog operating voltage (ADC used)		2.4	3.6	
V_{BAT}	Backup operating voltage		1.8	3.6	V
P_D	Power dissipation at T_A = 85 °C(3)	LQFP144		666	mW
		LQFP100		434	
		LQFP64		444	
TA	Ambient temperature	Maximum power dissipation	–40	85	°C
		Low power dissipation(4)	–40	105	°C
TJ	Junction temperature range		–40	105	°C

1. When the ADC is used, refer to *Table 53: ADC characteristics*.
2. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and operation.
3. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed $T_J$max (see *Table 6.2: Thermal characteristics on page 94*).
4. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed $T_J$max (see *Table 6.2: Thermal characteristics on page 94*).

5.3.2 Operating conditions at power-up / power-down

The parameters given in *Table 11* are derived from tests performed under the ambient temperature condition summarized in *Table 10*.

Table 11. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate		0	∞	µs/V
	V_{DD} fall time rate		20	∞	

5.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 12* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

Table 12. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.1	2.18	2.26	V
		PLS[2:0]=000 (falling edge)	2	2.08	2.16	V
		PLS[2:0]=001 (rising edge)	2.19	2.28	2.37	V
		PLS[2:0]=001 (falling edge)	2.09	2.18	2.27	V
		PLS[2:0]=010 (rising edge)	2.28	2.38	2.48	V
		PLS[2:0]=010 (falling edge)	2.18	2.28	2.38	V
		PLS[2:0]=011 (rising edge)	2.38	2.48	2.58	V
		PLS[2:0]=011 (falling edge)	2.28	2.38	2.48	V
		PLS[2:0]=100 (rising edge)	2.47	2.58	2.69	V
		PLS[2:0]=100 (falling edge)	2.37	2.48	2.59	V
		PLS[2:0]=101 (rising edge)	2.57	2.68	2.79	V
		PLS[2:0]=101 (falling edge)	2.47	2.58	2.69	V
		PLS[2:0]=110 (rising edge)	2.66	2.78	2.9	V
		PLS[2:0]=110 (falling edge)	2.56	2.68	2.8	V
		PLS[2:0]=111 (rising edge)	2.76	2.88	3	V
		PLS[2:0]=111 (falling edge)	2.66	2.78	2.9	V
$V_{PVDhyst}$[2]	PVD hysteresis			100		mV
$V_{POR/PDR}$	Power on/power down reset threshold	Falling edge	1.8[1]	1.88	1.96	V
		Rising edge	1.84	1.92	2.0	V
$V_{PDRhyst}$[2]	PDR hysteresis			40		mV
$t_{RSTTEMPO}$[2]	Reset temporization		1.5	2.5	3.5	ms

1. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
2. Guaranteed by design, not tested in production.

5.3.4 Embedded reference voltage

The parameters given in *Table 13* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

Table 13. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +85 °C	1.16	1.20	1.24	V
$T_{S\_vrefint}$[1]	ADC sampling time when reading the internal reference voltage			5.1	17.1[2]	µs

1. Shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design, not tested in production.

5.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.
The current consumption is measured as described in *Figure 10: Current consumption measurement scheme*.
All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to Dhrystone 2.1 code.

Maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except if it is explicitly mentioned
- The Flash access time is adjusted to f_{HCLK} frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 36 MHz)
- Prefetch in on (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{PCLK1} = f_{HCLK/2}$, $f_{PCLK2} = f_{HCLK}$

The parameters given in *Table 14* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

Table 14. Maximum current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Max(1) T_A = 85 °C	Unit
I_{DD}	Supply current in Run mode	External clock (2), all peripherals enabled	36 MHz	39	mA
			24 MHz	27	
			16 MHz	20	
			8 MHz	11	
		External clock (2), all peripherals Disabled	36 MHz	22	
			24 MHz	16.5	
			16 MHz	12.5	
			8 MHz	8	

1. Based on characterization, not tested in production.
2. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 15. Maximum current consumption in Run mode, code with data processing running from RAM

Symbol	Parameter	Conditions	f_{HCLK}	Max(1) T_A = 85 °C	Unit
I_{DD}	Supply current in Run mode	External clock (2), all peripherals enabled	36 MHz	34	mA
			24 MHz	24	
			16 MHz	17	
			8 MHz	10	
		External clock(2) all peripherals disabled	36 MHz	18	
			24 MHz	13	
			16 MHz	10	
			8 MHz	6	

1. Based on characterization, tested in production at V_{DD} max, f_{HCLK} max.
2. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Figure 11. Typical current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals enabled

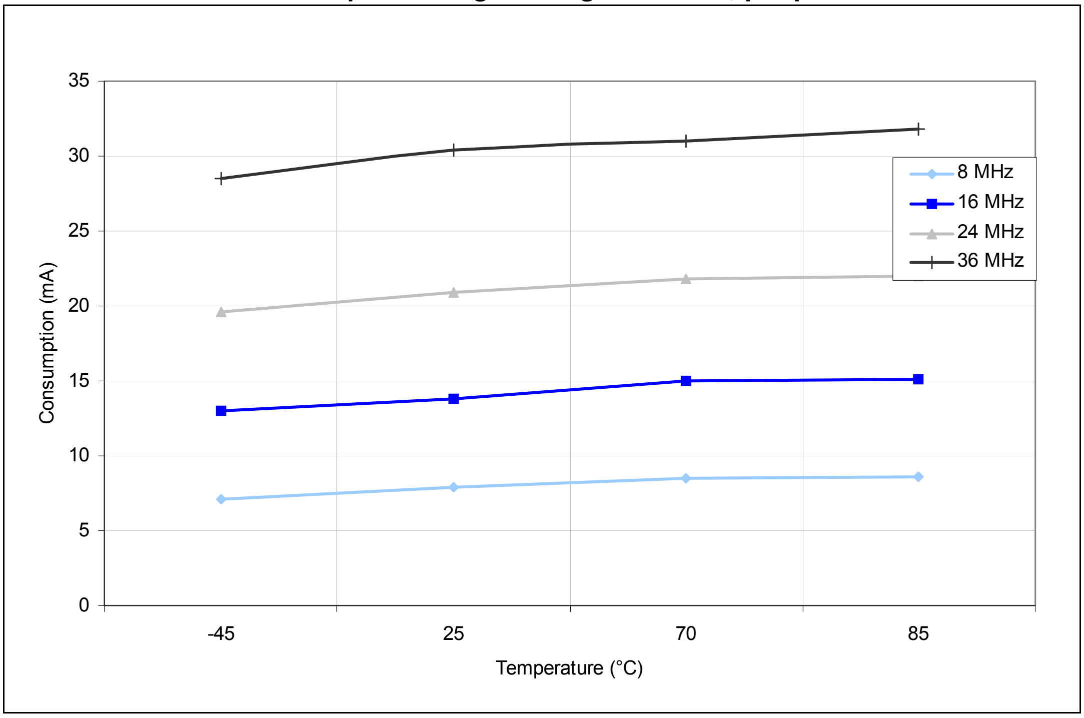


Figure 12. Typical current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals disabled

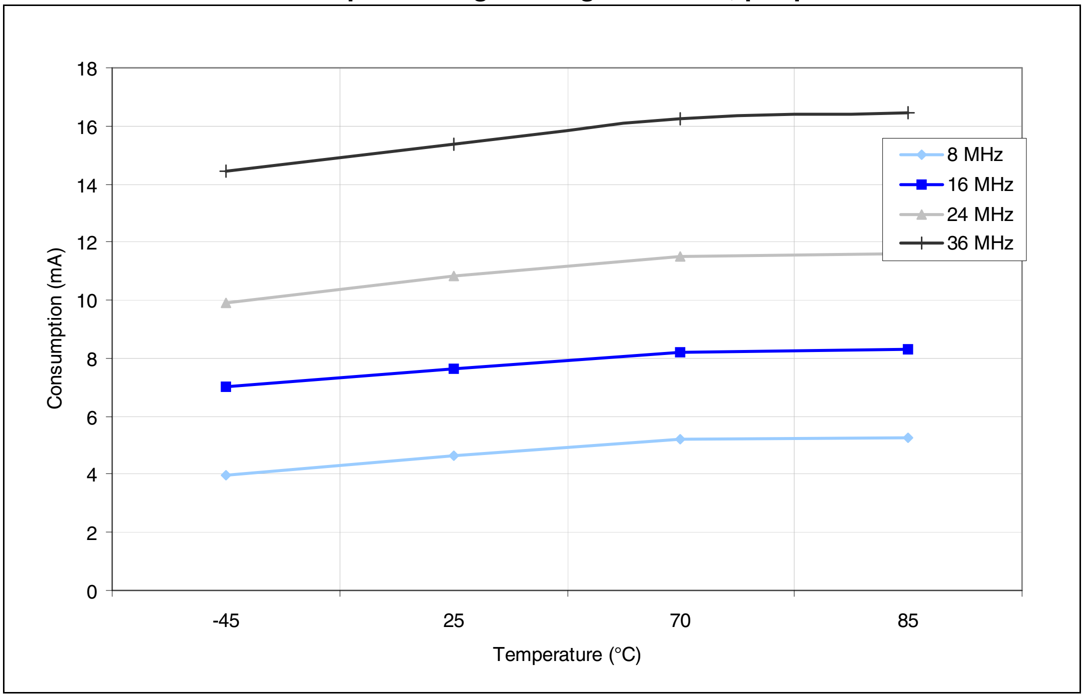


Table 16. Maximum current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Max[1] $T_A = 85\ °C$	Unit
I_{DD}	Supply current in Sleep mode	External clock[2] all peripherals enabled	36 MHz	24	mA
			24 MHz	17	
			16 MHz	12.5	
			8 MHz	8	
		External clock[2], all peripherals disabled	36 MHz	6	
			24 MHz	5	
			16 MHz	4.5	
			8 MHz	4	

1. Based on characterization, tested in production at V_{DD} max, f_{HCLK} max with peripherals enabled.
2. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 17. Typical and maximum current consumptions in Stop and Standby modes

Symbol	Parameter	Conditions	Typ(1)		Max	Unit
			V_{DD}/V_{BAT} = 2.4 V	V_{DD}/V_{BAT} = 3.3 V	T_A = 85 °C	
I_{DD}	Supply current in Stop mode	Regulator in Run mode, Low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	34.5	35	379	µA
		Regulator in Low-power mode, Low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	24.5	25	365	
	Supply current in Standby mode	Low-speed internal RC oscillator and independent watchdog ON	3	3.8	-	
		Low-speed internal RC oscillator ON, independent watchdog OFF	2.8	3.6	-	
		Low-speed internal RC oscillator and independent watchdog OFF, low-speed oscillator and RTC OFF	1.9	2.1	5(2)	
I_{DD_VBAT}	Backup domain supply current	Low-speed oscillator and RTC ON	1.1	1.4	2(2)	

1. Typical values are measured at T_A = 25 °C.
2. Based on characterization, not tested in production.

Figure 13. Typical current consumption in Stop mode with regulator in run mode versus temperature at different V_{DD} values

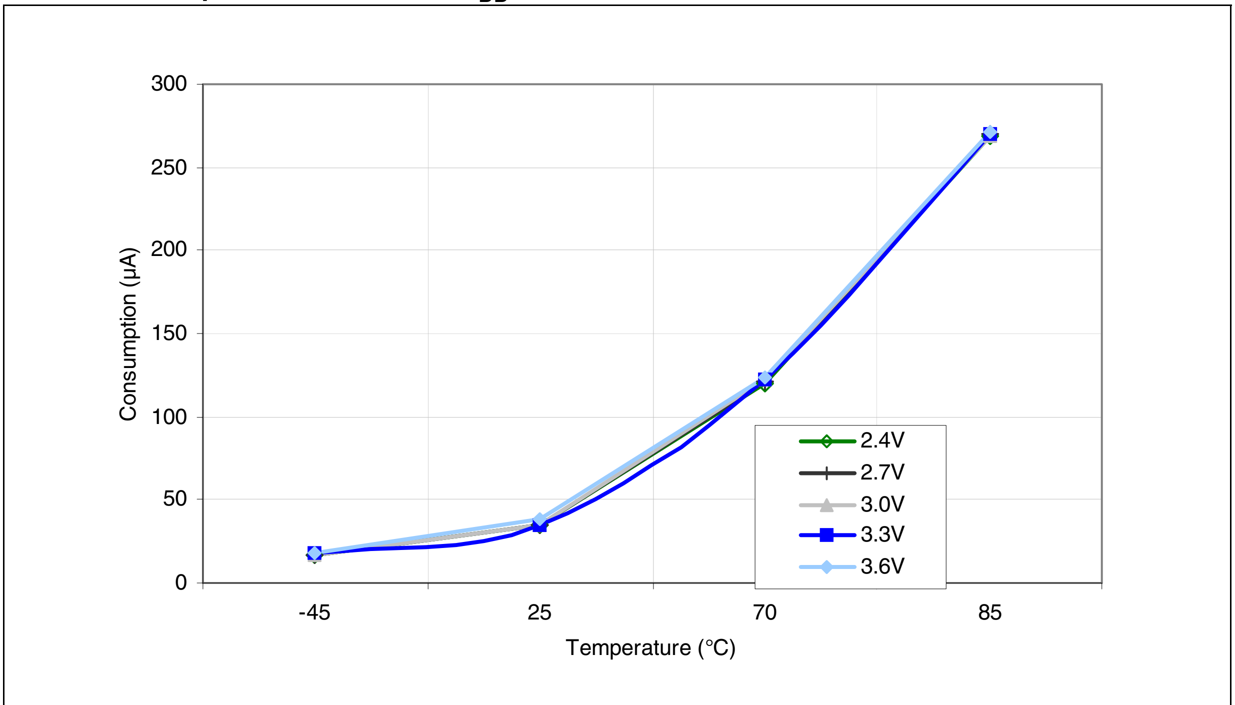


Figure 14. Typical current consumption in Stop mode with regulator in low-power mode versus temperature at different V_{DD} values

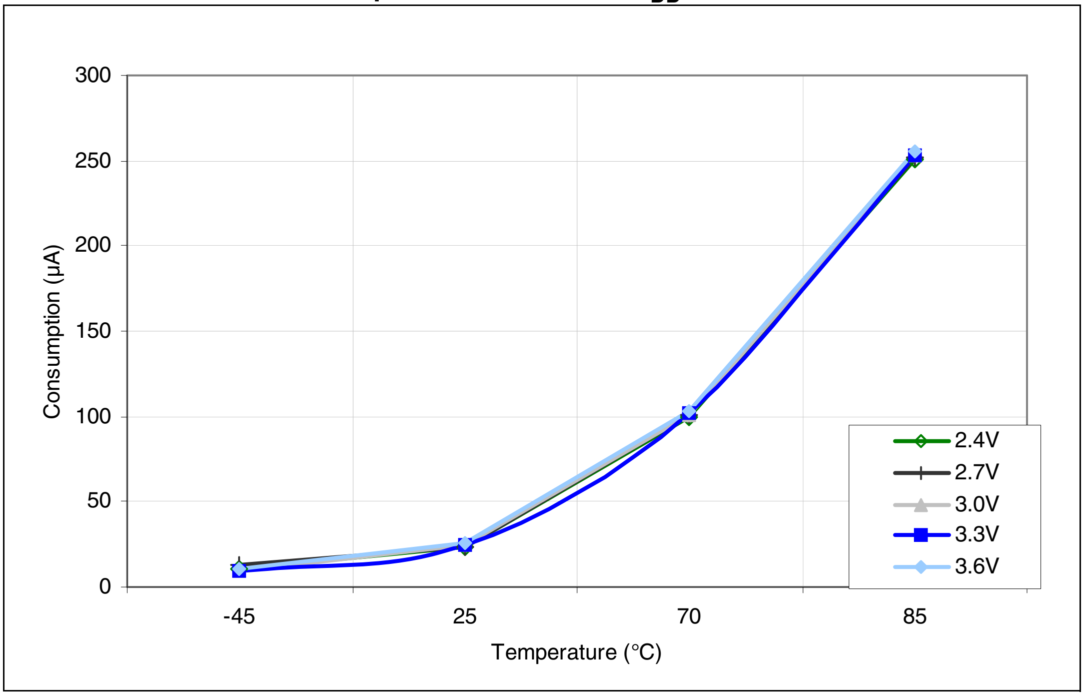
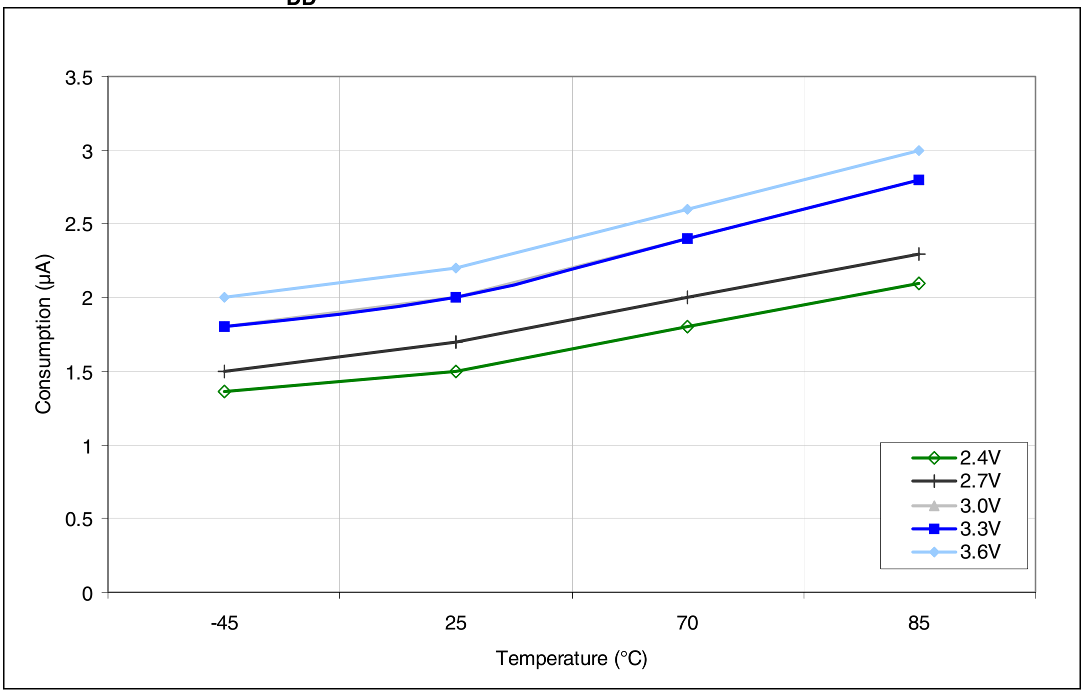


Figure 15. Typical current consumption in Standby mode versus temperature at different V_{DD} values



Typical current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except if it is explicitly mentioned
- The Flash access time is adjusted to f_{HCLK} frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 36 MHz)
- Prefetch is on (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{PCLK1} = f_{HCLK/4}$, $f_{PCLK2} = f_{HCLK/2}$, $f_{ADCCLK} = f_{PCLK2}/4$

The parameters given in *Table 18* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

Table 18. Typical current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1) All peripherals enabled(2)	Typ(1) All peripherals disabled	Unit
I_{DD}	Supply current in Run mode	External clock(3)	36 MHz	26.6	16.2	mA
			24 MHz	18.5	11.4	
			16 MHz	12.8	8.2	
			8 MHz	7.2	5	
			4 MHz	4.2	3.1	
			2 MHz	2.7	2.1	
			1 MHz	2	1.7	
			500 kHz	1.6	1.4	
			125 kHz	1.3	1.2	
		Running on high speed internal RC (HSI), AHB prescaler used to reduce the frequency	36 MHz	26	15.6	
			24 MHz	17.9	10.8	
			16 MHz	12.2	7.6	
			8 MHz	6.6	4.4	
			4 MHz	3.6	2.5	
			2 MHz	2.1	1.5	
			1 MHz	1.4	1.1	
			500 kHz	1	0.8	
			125 kHz	0.7	0.6	

1. Typical values are measures at $T_A = 25$ °C, $V_{DD} = 3.3$ V.
2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. External clock is 8 MHz and PLL is on when $f_{HCLK} > 8$ MHz.

Table 19. Typical current consumption in Sleep mode, code with data processing code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1) All peripherals enabled(2)	Typ(1) All peripherals disabled	Unit
I_{DD}	Supply current in Sleep mode	External clock(3)	36 MHz	15.1	3.6	mA
			24 MHz	10.4	2.6	
			16 MHz	7.2	2	
			8 MHz	3.9	1.3	
			4 MHz	2.6	1.2	
			2 MHz	1.85	1.15	
			1 MHz	1.5	1.1	
			500 kHz	1.3	1.05	
			125 kHz	1.2	1.05	
		Running on High Speed Internal RC (HSI), AHB prescaler used to reduce the frequency	36 MHz	14.5	3	
			24 MHz	9.8	2	
			16 MHz	6.6	1.4	
			8 MHz	3.3	0.7	
			4 MHz	2	0.6	
			2 MHz	1.25	0.55	
			1 MHz	0.9	0.5	
			500 kHz	0.7	0.45	
			125 kHz	0.6	0.45	

1. Typical values are measures at T_A = 25 °C, V_{DD} = 3.3 V.
2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 20*. The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- ambient operating temperature and V_{DD} supply voltage conditions summarized in *Table 7*.

Table 20. Peripheral current consumption

Peripheral		Typical consumption at 25 °C(1)	Unit
APB1	TIM2	0.6	mA
	TIM3	0.6	
	TIM4	0.6	
	TIM5	0.6	
	TIM6	0.2	
	TIM7	0.2	
	SPI2	0.15	
	SPI3	0.15	
	USART2	0.25	
	USART3	0.25	
	UART4	0.3	
	UART5	0.3	
	I2C1	0.22	
	I2C2	0.22	
	DAC	0.72	
APB2	GPIOA	0.3	
	GPIOB	0.4	
	GPIOC	0.4	
	GPIOD	0.3	
	GPIOE	0.5	
	GPIOF	0.4	
	GPIOG	0.5	
	ADC(2)	1.4	
	SPI1	0.3	
	USART1	0.6	

1. f_{HCLK} = 36 MHz, $f_{APB1} = f_{HCLK/2}$, $f_{APB2} = f_{HCLK}$, default prescaler value for each peripheral.
2. Specific conditions for ADC: f_{HCLK} = 28 MHz, $f_{APB1} = f_{HCLK/2}$, $f_{APB2} = f_{HCLK}$, $f_{ADCCLK} = f_{APB2}/2$, ADON bit in the ADC_CR2 register is set to 1.

5.3.6 External clock source characteristics

High-speed external user clock generated from an external source

The characteristics given in *Table 21* result from tests performed using an high-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 10*.

Table 21. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency(1)		0	8	25	MHz
V_{HSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$		V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}		$0.3V_{DD}$	V
$t_{w(HSE)}$ $t_{w(HSE)}$	OSC_IN high or low time(1)		16			ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time(1)				20	ns
$C_{in(HSE)}$	OSC_IN input capacitance(1)			5		pF
$DuCy_{(HSE)}$	Duty cycle		45		55	%
I_L	OSC_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$			±1	µA

1. Guaranteed by design, not tested in production

Low-speed external user clock generated from an external source

The characteristics given in *Table 22* result from tests performed using an low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 10*.

Table 22. Low-speed user external clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency(1)			32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$		V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}		$0.3V_{DD}$	V
$t_{w(LSE)}$ $t_{w(LSE)}$	OSC32_IN high or low time(1)		450			ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time(1)				50	ns
$C_{in(LSE)}$	OSC32_IN input capacitance(1)			5		pF
$DuCy_{(LSE)}$	Duty cycle		30		70	%
I_L	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$			±1	µA

1. Guaranteed by design, not tested in production.

Figure 16. High-speed external clock source AC timing diagram

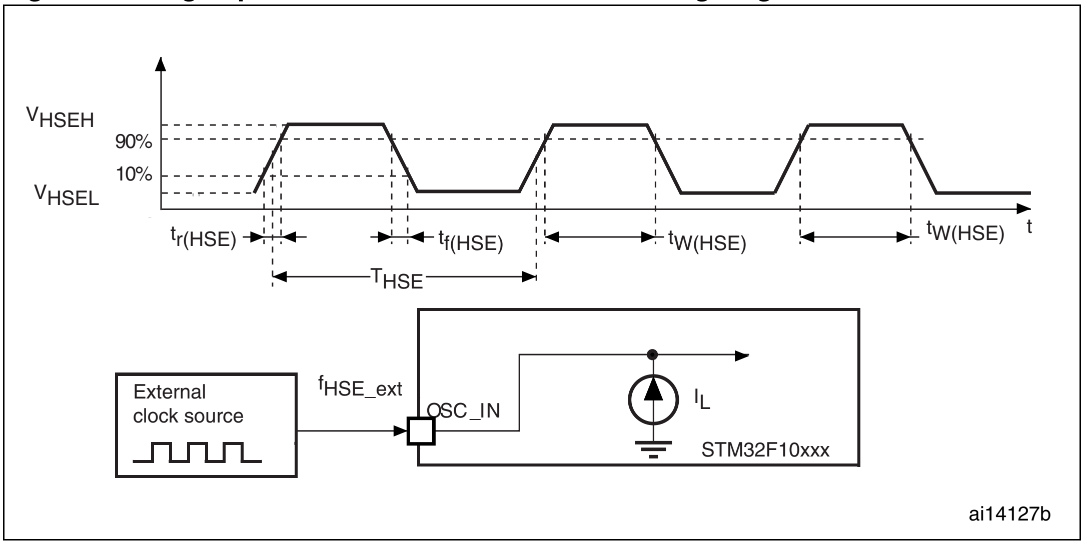
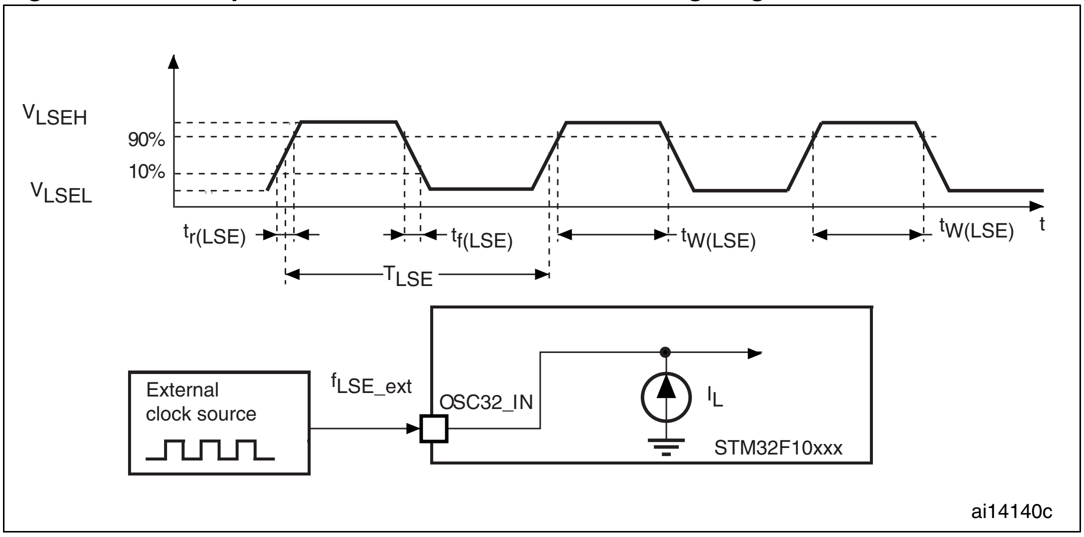


Figure 17. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

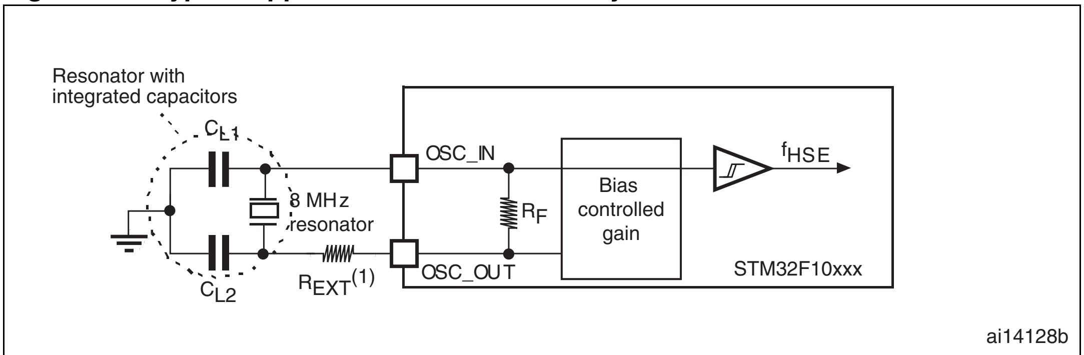
The high-speed external (HSE) clock can be supplied with a 4 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in Table 23. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 23. HSE 4-16 MHz oscillator characteristics[1][2]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency		4	8	16	MHz
R_F	Feedback resistor			200		kΩ
C_{L1} C_{L2}[3]	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)[4]	R_S = 30 Ω		30		pF
i_2	HSE driving current	V_{DD} = 3.3 V $V_{IN} = V_{SS}$ with 30 pF load			1	mA
g_m	Oscillator transconductance	Startup	25			mA/V
$t_{SU(HSE)}$[5]	Startup time	V_{DD} is stabilized		2		ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Based on characterization results, not tested in production.
3. For C_{L1} and C_{L2} it is recommended to use high-quality ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.
4. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
5. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

Figure 18. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics. Typical value is in the range of 5 to 6R_S.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 24*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Note: *For C_{L1} and C_{L2} it is recommended to use high-quality ceramic capacitors in the 5 pF to 15 pF range selected to match the requirements of the crystal or resonator. C_{L1} and $C_{L2,}$ are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}.*
Load capacitance C_L has the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$ where C_{stray} is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.

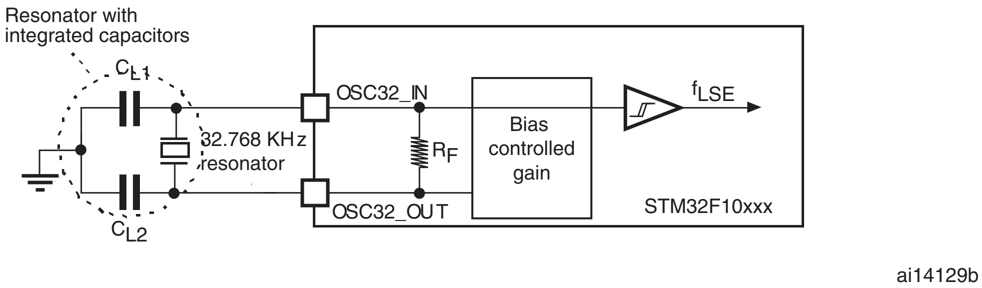
Caution: To avoid exceeding the maximum value of C_{L1} and C_{L2} (15 pF) it is strongly recommended to use a resonator with a load capacitance $C_L \leq 7$ pF. Never use a resonator with a load capacitance of 12.5 pF.
Example: if you choose a resonator with a load capacitance of C_L = 6 pF, and C_{stray} = 2 pF, then $C_{L1} = C_{L2}$ = 8 pF.

Table 24. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_F	Feedback resistor			5		MΩ
C_{L1} C_{L2}(2)	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)(3)	R_S = 30 KΩ			15	pF
I_2	LSE driving current	V_{DD} = 3.3 V $V_{IN} = V_{SS}$			1.4	µA
g_m	Oscillator transconductance		5			µA/V
$t_{SU(LSE)}$(4)	Startup time	V_{DD} is stabilized		3		s

1. Based on characterization, not tested in production.
2. Refer to the note and caution paragraphs above the table.
3. The oscillator selection can be optimized in terms of supply current using an high quality resonator with small R_S value for example MSIV-TIN32.768 kHz. Refer to crystal manufacturer for more details
4. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

Figure 19. Typical application with a 32.768 kHz crystal



5.3.7 Internal clock source characteristics

The parameters given in *Table 25* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

High-speed internal (HSI) RC oscillator

Table 25. HSI oscillator characteristics(1) (2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency			8		MHz
ACC_{HSI}	Accuracy of HSI oscillator	T_A = –40 to 85 °C	–2	±1	2.5	%
		T_A = –10 to 85 °C	–1.5	±1	2.2	
		T_A = 00 to 70 °C	–1.3	±1	2	
		T_A = 25 °C	–1.1	±1	1.8	%
$t_{su(HSI)}$	HSI oscillator startup time		1		2	µs
$I_{DD(HSI)}$	HSI oscillator power consumption			80	100	µA

1. V_{DD} = 3.3 V, T_A = –40 to 85 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.

Low-speed internal (LSI) RC oscillator

Table 26. LSI oscillator characteristics (1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}(2)	Frequency	30	40	60	kHz
$t_{su(LSI)}$(3)	LSI oscillator startup time			85	µs
$I_{DD(LSI)}$(3)	LSI oscillator power consumption		0.65	1.2	µA

1. V_{DD} = 3 V, T_A = –40 to 85 °C unless otherwise specified.
2. Based on characterization, not tested in production.
3. Guaranteed by design, not tested in production.

Wakeup time from low-power mode

The wakeup times given in Table 27 are measured on a wakeup phase with an 8-MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or Standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock that was set before entering Sleep mode.

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in Table 10.

Table 27. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ	Unit
$t_{WUSLEEP}$(1)	Wakeup from Sleep mode	Wakeup on HSI RC clock	1.8	µs
t_{WUSTOP}(1)	Wakeup from Stop mode (regulator in run mode)	HSI RC wakeup time = 2 µs	3.6	µs
	Wakeup from Stop mode (regulator in low-power mode)	HSI RC wakeup time = 2 µs, Regulator wakeup from LP mode time = 5 µs	5.4	
$t_{WUSTDBY}$(1)	Wakeup from Standby mode	HSI RC wakeup time = 2 µs, Regulator wakeup from power down time = 38 µs	50	µs

1. The wakeup times are measured from the wakeup event to the point at which the user application code reads the first instruction.

5.3.8 PLL characteristics

The parameters given in Table 28 are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in Table 10.

Table 28. PLL characteristics

Symbol	Parameter	Value			Unit
		Min(1)	Typ	Max(1)	
f_{PLL_IN}	PLL input clock(2)	1	8.0	25	MHz
	PLL input clock duty cycle	40		60	%
f_{PLL_OUT}	PLL multiplier output clock	16		36	MHz
t_{LOCK}	PLL lock time			200	µs

1. Based on characterization, not tested in production.
2. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.

5.3.9 Memory characteristics

Flash memory

The characteristics are given at T_A = –40 to 85 °C unless otherwise specified.

Table 29. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
t_{prog}	16-bit programming time	T_A = –40 to +85 °C	40	52.5	70	µs
t_{ERASE}	Page (2 KB) erase time	T_A = –40 to +85 °C	20		40	ms
t_{ME}	Mass erase time	T_A = –40 to +85 °C	20		40	ms
I_{DD}	Supply current	Read mode f_{HCLK} = 36 MHz with 1 wait state, V_{DD} = 3.3 V			28	mA
		Write mode f_{HCLK} = 36 MHz, V_{DD} = 3.3 V			7	mA
		Erase mode f_{HCLK} = 36 MHz, V_{DD} = 3.3 V			5	mA
		Power-down mode / Halt, V_{DD} = 3.0 to 3.6 V			50	µA
V_{prog}	Programming voltage		2		3.6	V

1. Guaranteed by design, not tested in production.

Table 30. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value			Unit
			Min(1)	Typ	Max	
N_{END}	Endurance	T_A = –40 °C to 85 °C	10			kcycles
t_{RET}	Data retention	T_A = 85 °C, 1 kcycle(2)	30			Years
		T_A = 55 °C, 10 kcycle(2)	20			

1. Based on characterization, not tested in production.
2. Cycling performed over the whole temperature range.

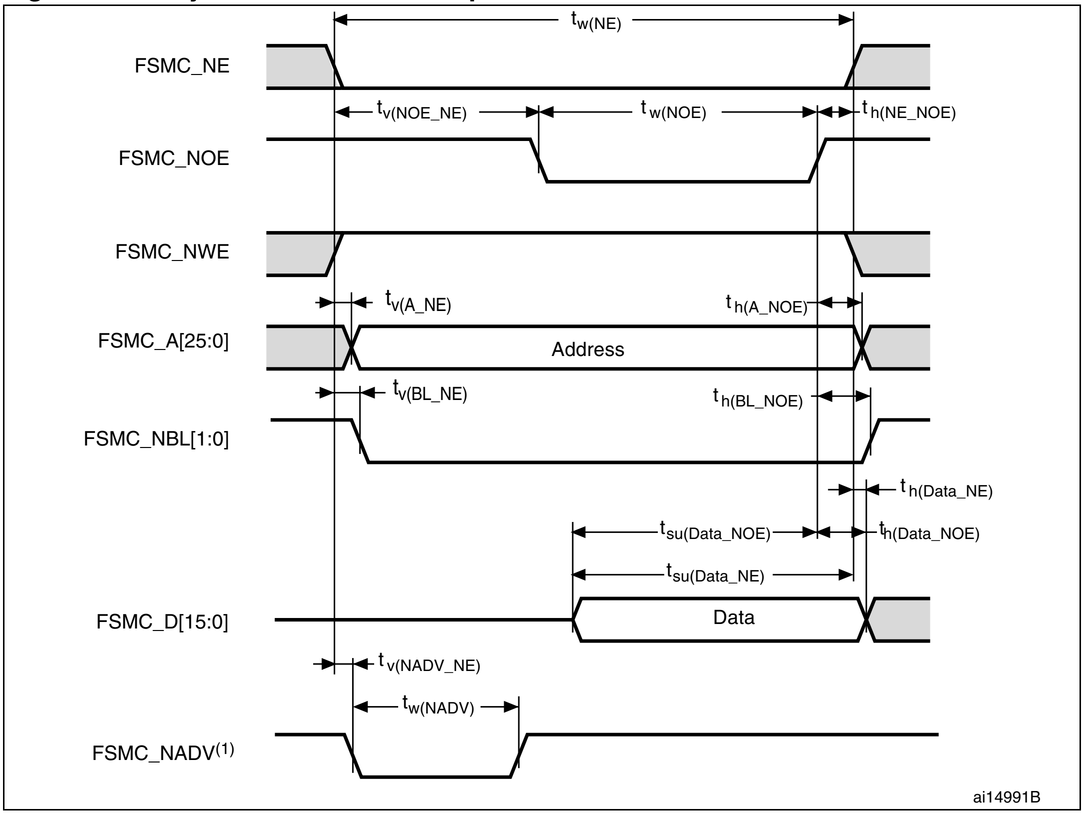
5.3.10 FSMC characteristics

Asynchronous waveforms and timings

Figure 20 through *Figure 23* represent asynchronous waveforms and *Table 31* through *Table 34* provide the corresponding timings. The results shown in these tables are obtained with the following FSMC configuration:

- AddressSetupTime = 0
- AddressHoldTime = 1
- DataSetupTime = 1

Figure 20. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms



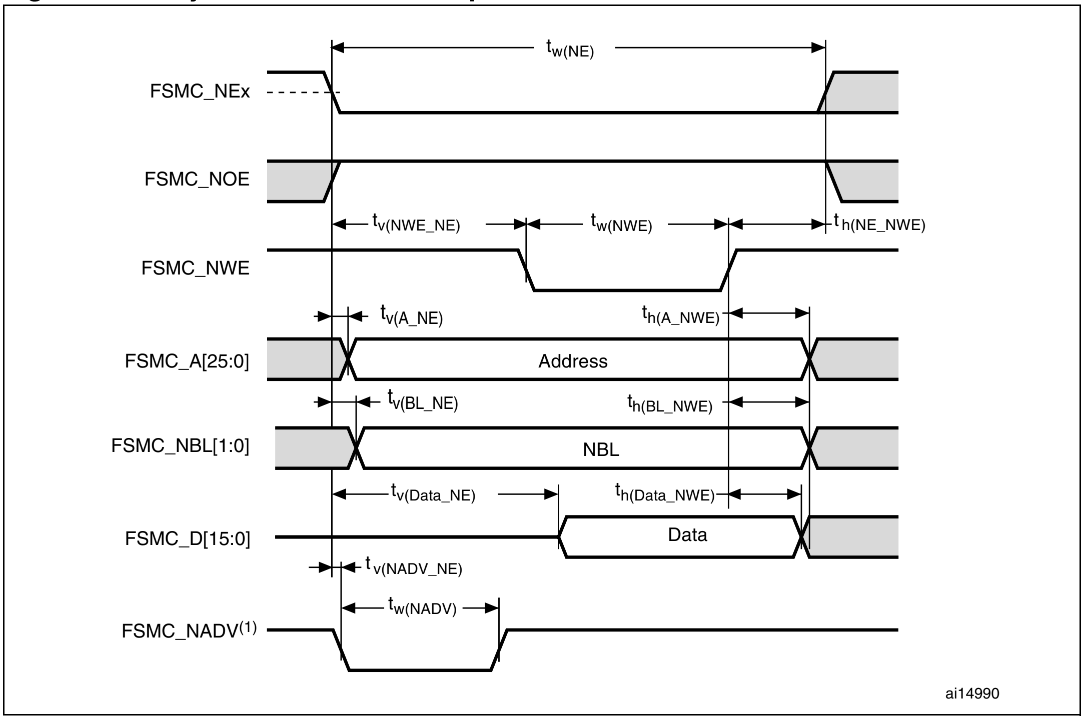
1. Mode 2/B, C and D only. In Mode 1, FSMC_NADV is not used.

Table 31. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings(1) (2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$5T_{HCLK} - 1.5$	$5T_{HCLK} + 2$	ns
$t_{v(NOE\_NE)}$	FSMC_NEx low to FSMC_NOE low	0.5	1.5	ns
$t_{w(NOE)}$	FSMC_NOE low time	$5T_{HCLK} - 1.5$	$5T_{HCLK} + 1.5$	ns
$t_{h(NE\_NOE)}$	FSMC_NOE high to FSMC_NE high hold time	–1.5		ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid		7	ns
$t_{h(A\_NOE)}$	Address hold time after FSMC_NOE high	2.5		ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid		0	ns
$t_{h(BL\_NOE)}$	FSMC_BL hold time after FSMC_NOE high	2.5		ns
$t_{su(Data\_NE)}$	Data to FSMC_NEx high setup time	$2T_{HCLK} + 25$		ns
$t_{su(Data\_NOE)}$	Data to FSMC_NOEx high setup time	$2T_{HCLK} + 25$		ns
$t_{h(Data\_NOE)}$	Data hold time after FSMC_NOE high	0		ns
$t_{h(Data\_NE)}$	Data hold time after FSMC_NEx high	0		ns
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low		5	ns
$t_{w(NADV)}$	FSMC_NADV low time		$T_{HCLK} + 1.5$	ns

1. V_{DD_IO} = V and C_L = 15 pF.
2. Based on characterization, not tested in production.

Figure 21. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms



1. Mode 2/B, C and D only. In Mode 1, FSMC_NADV is not used.

Table 32. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings[(1)(2)]

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$3T_{HCLK} - 1$	$3T_{HCLK} + 2$	ns
$t_{v(NWE\_NE)}$	FSMC_NEx low to FSMC_NWE low	$T_{HCLK} - 0.5$	$T_{HCLK} + 1.5$	ns
$t_{w(NWE)}$	FSMC_NWE low time	$T_{HCLK} - 0.5$	$T_{HCLK} + 1.5$	ns
$t_{h(NE\_NWE)}$	FSMC_NWE high to FSMC_NE high hold time	T_{HCLK}		ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid		7.5	ns
$t_{h(A\_NWE)}$	Address hold time after FSMC_NWE high	$T_{HCLK} + 2$		ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid		1.5	ns
$t_{h(BL\_NWE)}$	FSMC_BL hold time after FSMC_NWE high	$T_{HCLK} - 0.5$		ns
$t_{v(Data\_NE)}$	FSMC_NEx low to Data valid		$T_{HCLK} + 7$	ns
$t_{h(Data\_NWE)}$	Data hold time after FSMC_NWE high	$T_{HCLK} + 3$		ns
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low		5.5	ns
$t_{w(NADV)}$	FSMC_NADV low time		$T_{HCLK} + 1.5$	ns

1. V_{DD_IO} = V and C_L = 15 pF.
2. Based on characterization, not tested in production.

Figure 22. Asynchronous multiplexed NOR/PSRAM read waveforms

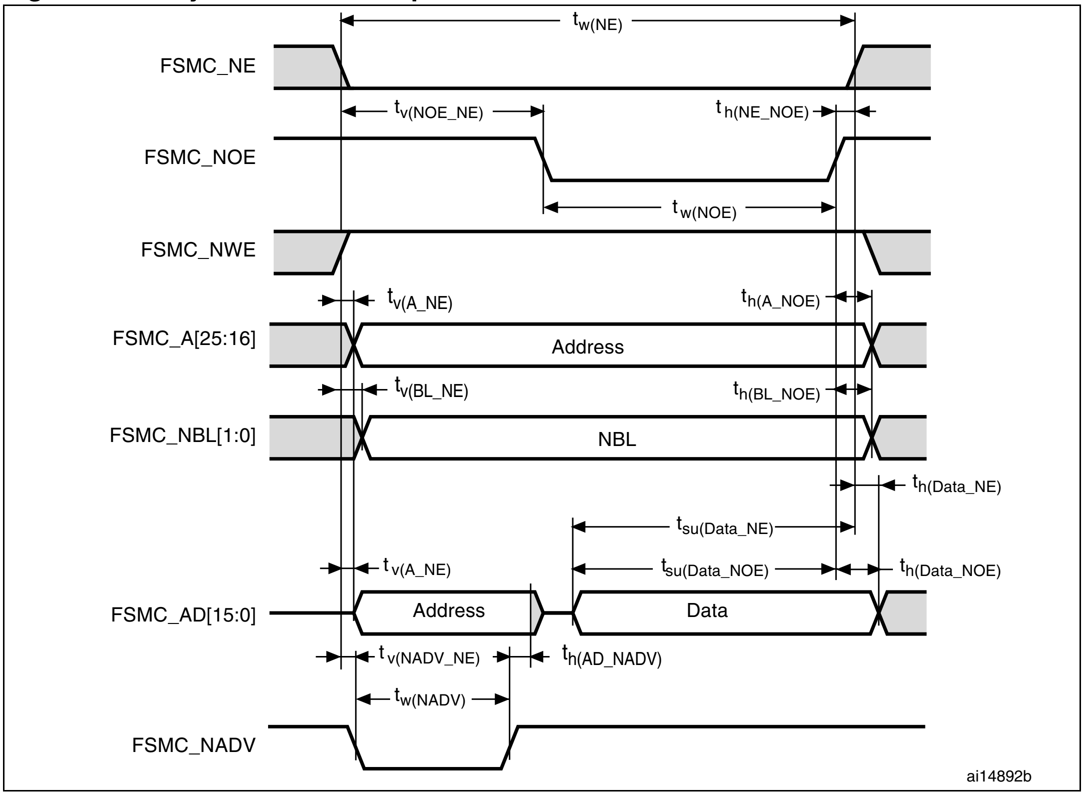


Table 33. Asynchronous multiplexed NOR/PSRAM read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$7T_{HCLK} - 2$	$7T_{HCLK} + 2$	ns
$t_{v(NOE\_NE)}$	FSMC_NEx low to FSMC_NOE low	$3T_{HCLK} - 0.5$	$3T_{HCLK} + 1.5$	ns
$t_{w(NOE)}$	FSMC_NOE low time	$4T_{HCLK} - 1$	$4T_{HCLK} + 2$	ns
$t_{h(NE\_NOE)}$	FSMC_NOE high to FSMC_NE high hold time	–1		ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid		0	ns
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	3	5	ns
$t_{w(NADV)}$	FSMC_NADV low time	$T_{HCLK} -1.5$	$T_{HCLK} + 1.5$	ns
$t_{h(AD\_NADV)}$	FSMC_AD (address) valid hold time after FSMC_NADV high	$T_{HCLK} + 3$		ns
$t_{h(A\_NOE)}$	Address hold time after FSMC_NOE high	$T_{HCLK} + 3$		ns
$t_{h(BL\_NOE)}$	FSMC_BL hold time after FSMC_NOE high	0		ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid		0	ns
$t_{su(Data\_NE)}$	Data to FSMC_NEx high setup time	$2T_{HCLK} + 24$		ns
$t_{su(Data\_NOE)}$	Data to FSMC_NOE high setup time	$2T_{HCLK} + 25$		ns
$t_{h(Data\_NE)}$	Data hold time after FSMC_NEx high	0		ns
$t_{h(Data\_NOE)}$	Data hold time after FSMC_NOE high	0		ns

1. V_{DD_IO} = V and C_L = 15 pF.
2. Based on characterization, not tested in production.

Figure 23. Asynchronous multiplexed NOR/PSRAM write waveforms

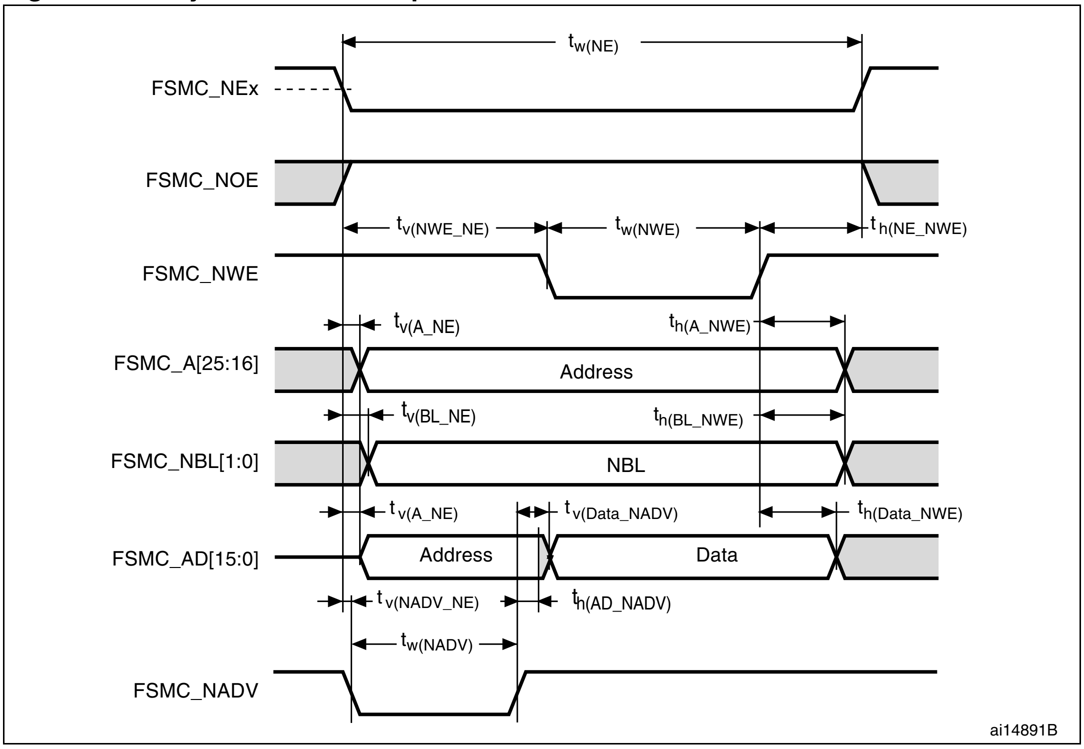


Table 34. Asynchronous multiplexed NOR/PSRAM write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$5T_{HCLK} - 1$	$5T_{HCLK} + 2$	ns
$t_{v(NWE\_NE)}$	FSMC_NEx low to FSMC_NWE low	$2T_{HCLK}$	$2T_{HCLK} + 1$	ns
$t_{w(NWE)}$	FSMC_NWE low time	$2T_{HCLK} - 1$	$2T_{HCLK} + 2$	ns
$t_{h(NE\_NWE)}$	FSMC_NWE high to FSMC_NE high hold time	$T_{HCLK} - 1$		ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid		7	ns
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	3	5	ns
$t_{w(NADV)}$	FSMC_NADV low time	$T_{HCLK} - 1$	$T_{HCLK} + 1$	ns
$t_{h(AD\_NADV)}$	FSMC_AD (address) valid hold time after FSMC_NADV high	$T_{HCLK} - 3$		ns
$t_{h(A\_NWE)}$	Address hold time after FSMC_NWE high	$4T_{HCLK} + 2.5$		ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid		1.6	ns
$t_{h(BL\_NWE)}$	FSMC_BL hold time after FSMC_NWE high	$T_{HCLK} - 1.5$		ns
$t_{v(Data\_NADV)}$	FSMC_NADV high to Data valid		$T_{HCLK} + 1.5$	ns
$t_{h(Data\_NWE)}$	Data hold time after FSMC_NWE high	$T_{HCLK} - 5$		ns

1. V_{DD_IO} = V and C_L = 15 pF.
2. Based on characterization, not tested in production.

Synchronous waveforms and timings

Figure 24 through *Figure 27* represent synchronous waveforms and *Table 36* through *Table 38* provide the corresponding timings. The results shown in these tables are obtained with the following FSMC configuration:

- BurstAccessMode = FSMC_BurstAccessMode_Enable;
- MemoryType = FSMC_MemoryType_CRAM;
- WriteBurst = FSMC_WriteBurst_Enable;
- CLKDivision = 1; (0 is not supported, see the STM32F10xxx reference manual)
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM

Figure 24. Synchronous multiplexed NOR/PSRAM read timings

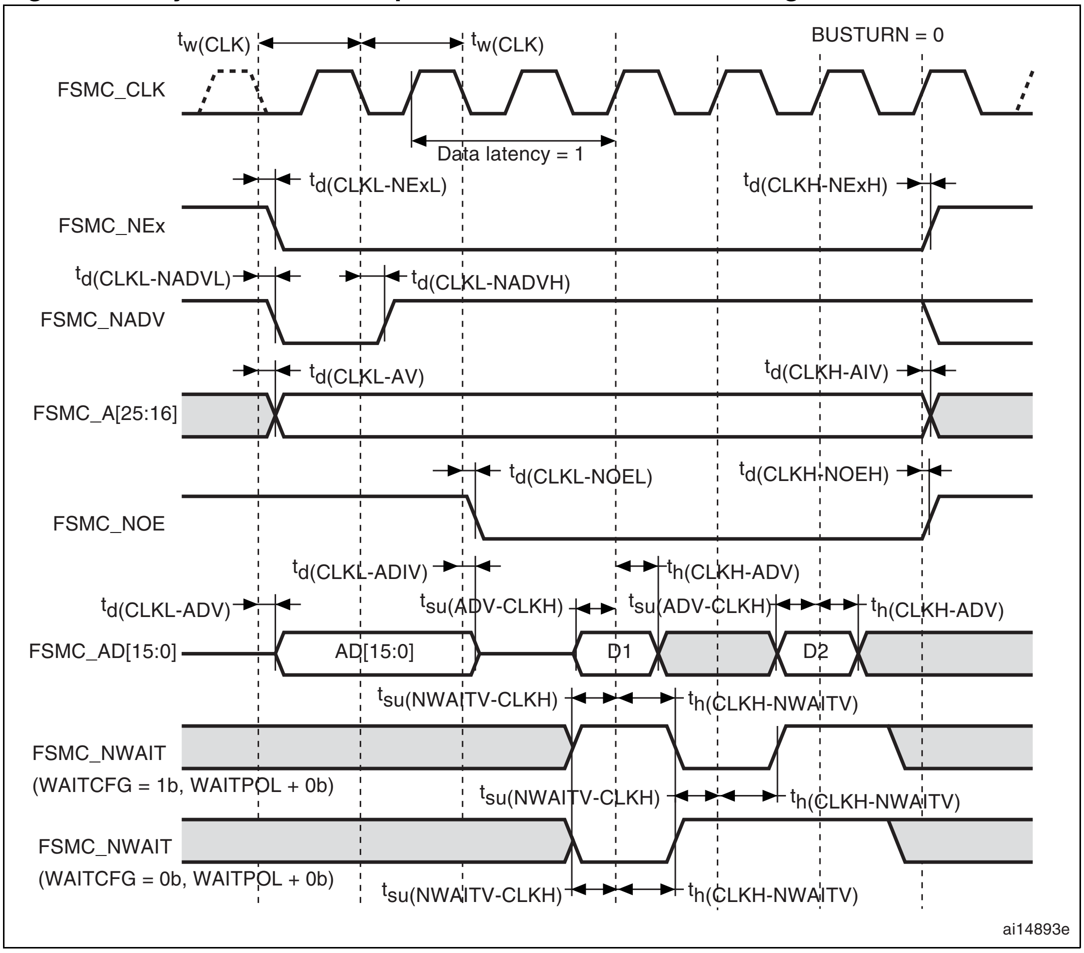


Table 35. Synchronous multiplexed NOR/PSRAM read timings[1][2]

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	27.7		ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x = 0...2)		1.5	ns
$t_{d(CLKH-NExH)}$	FSMC_CLK high to FSMC_NEx high (x = 0...2)	T_{HCLK} + 2		ns
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low		4	ns
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	5		ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x = 16...25)		0	ns
$t_{d(CLKH-AIV)}$	FSMC_CLK high to FSMC_Ax invalid (x = 16...25)	T_{HCLK} + 2		ns
$t_{d(CLKL-NOEL)}$	FSMC_CLK low to FSMC_NOE low		T_{HCLK} +1	ns
$t_{d(CLKH-NOEH)}$	FSMC_CLK high to FSMC_NOE high	T_{HCLK} + 0.5		ns
$t_{d(CLKL-ADV)}$	FSMC_CLK low to FSMC_AD[15:0] valid		12	ns
$t_{d(CLKL-ADIV)}$	FSMC_CLK low to FSMC_AD[15:0] invalid	0		ns
$t_{su(ADV-CLKH)}$	FSMC_A/D[15:0] valid data before FSMC_CLK high	6		ns
$t_{h(CLKH-ADV)}$	FSMC_A/D[15:0] valid data after FSMC_CLK high	T_{HCLK} – 10		ns
$t_{su(NWAITV-CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	8		ns
$t_{h(CLKH-NWAITV)}$	FSMC_NWAIT valid after FSMC_CLK high	6		ns

1. V_{DD_IO} = V and C_L = 15 pF.
2. Based on characterization, not tested in production.

Figure 25. Synchronous multiplexed PSRAM write timings

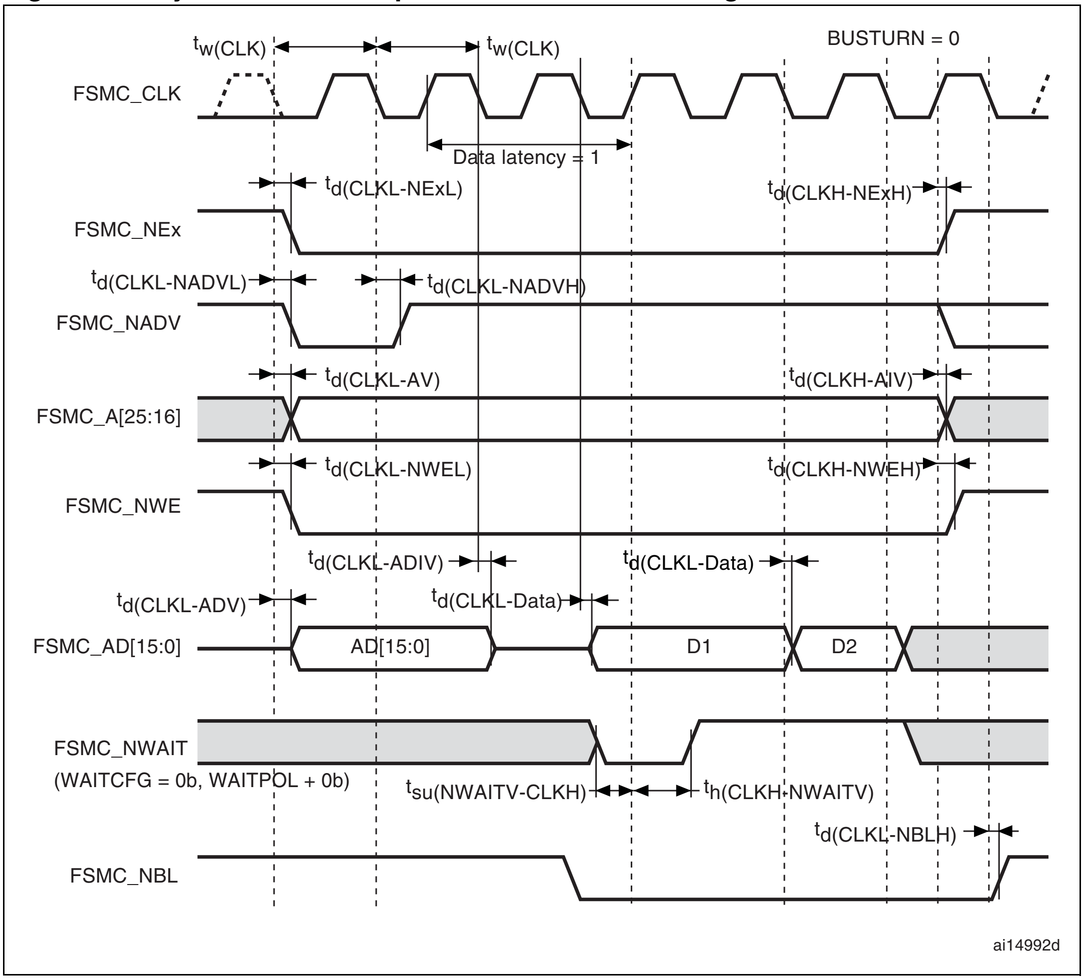


Table 36. Synchronous multiplexed PSRAM write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	27.7		ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_Nex low (x = 0...2)		2	ns
$t_{d(CLKH-NExH)}$	FSMC_CLK high to FSMC_NEx high (x = 0...2)	T_{HCLK} + 2		ns
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low		4	ns
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	5		ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x = 16...25)		0	ns
$t_{d(CLKH-AIV)}$	FSMC_CLK high to FSMC_Ax invalid (x = 16...25)	T_{CK} + 2		ns
$t_{d(CLKL-NWEL)}$	FSMC_CLK low to FSMC_NWE low		1	ns
$t_{d(CLKH-NWEH)}$	FSMC_CLK high to FSMC_NWE high	T_{HCLK} +1		ns
$t_{d(CLKL-ADV)}$	FSMC_CLK low to FSMC_AD[15:0] valid		12	ns
$t_{d(CLKL-ADIV)}$	FSMC_CLK low to FSMC_AD[15:0] invalid	3		ns
$t_{d(CLKL-Data)}$	FSMC_A/D[15:0] valid after FSMC_CLK low		6	ns
$t_{su(NWAITV-CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	7		ns
$t_{h(CLKH-NWAITV)}$	FSMC_NWAIT valid after FSMC_CLK high	2		ns
$t_{d(CLKL-NBLH)}$	FSMC_CLK low to FSMC_NBL high	1		ns

1. V_{DD_IO} = V and C_L = 15 pF.
2. Based on characterization, not tested in production.

Figure 26. Synchronous non-multiplexed NOR/PSRAM read timings

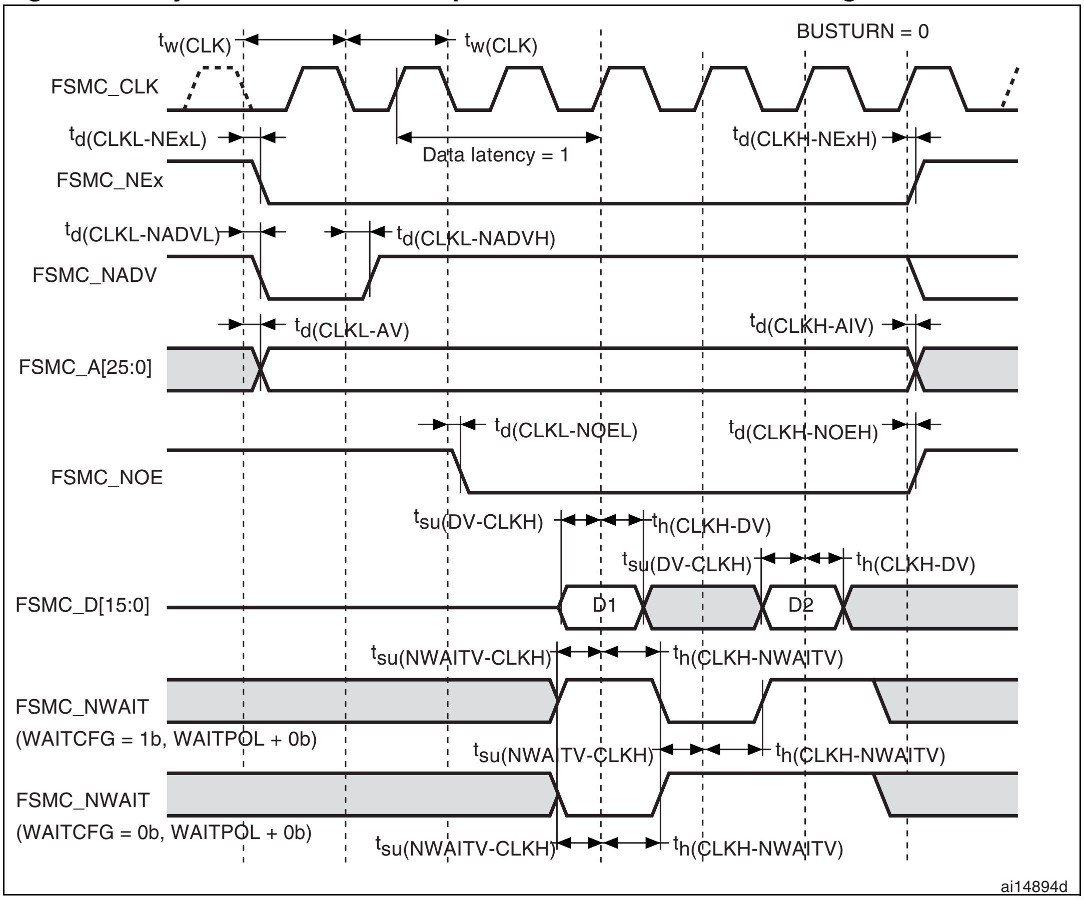


Table 37. Synchronous non-multiplexed NOR/PSRAM read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	27.7		ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x = 0...2)		1.5	ns
$t_{d(CLKH-NExH)}$	FSMC_CLK high to FSMC_NEx high (x = 0...2)	$T_{HCLK} + 2$		ns
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low		4	ns
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	5		ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x = 0...25)		0	ns
$t_{d(CLKH-AIV)}$	FSMC_CLK high to FSMC_Ax invalid (x = 0...25)	$T_{HCLK} + 4$		ns
$t_{d(CLKL-NOEL)}$	FSMC_CLK low to FSMC_NOE low		$T_{HCLK} + 1.5$	ns
$t_{d(CLKH-NOEH)}$	FSMC_CLK high to FSMC_NOE high	$T_{HCLK} + 1.5$		ns
$t_{su(DV-CLKH)}$	FSMC_D[15:0] valid data before FSMC_CLK high	6.5		ns
$t_{h(CLKH-DV)}$	FSMC_D[15:0] valid data after FSMC_CLK high	7		ns
$t_{su(NWAITV-CLKH)}$	FSMC_NWAIT valid before FSMC_SMCLK high	7		ns
$t_{h(CLKH-NWAITV)}$	FSMC_NWAIT valid after FSMC_CLK high	2		ns

1. V_{DD_IO} = V and C_L = 15 pF.
2. Based on characterization, not tested in production.

Figure 27. Synchronous non-multiplexed PSRAM write timings

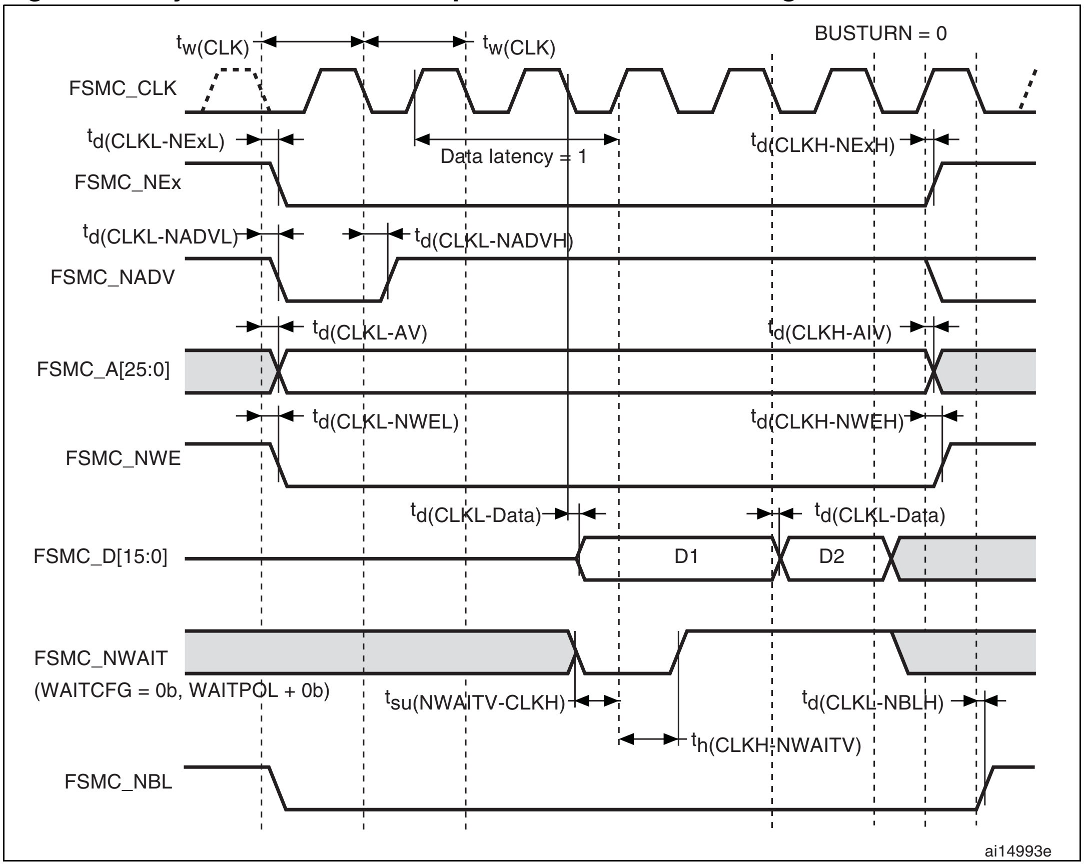


Table 38. Synchronous non-multiplexed PSRAM write timings[(1)(2)]

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	27.7		ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x = 0...2)		2	ns
$t_{d(CLKH-NExH)}$	FSMC_CLK high to FSMC_NEx high (x = 0...2)	T_{HCLK} + 2		ns
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low		4	ns
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	5		ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x = 16...25)		0	ns
$t_{d(CLKH-AIV)}$	FSMC_CLK high to FSMC_Ax invalid (x = 16...25)	T_{CK} + 2		ns
$t_{d(CLKL-NWEL)}$	FSMC_CLK low to FSMC_NWE low		1	ns
$t_{d(CLKH-NWEH)}$	FSMC_CLK high to FSMC_NWE high	T_{HCLK} + 1		ns
$t_{d(CLKL-Data)}$	FSMC_D[15:0] valid data after FSMC_CLK low		6	ns
$t_{su(NWAITV-CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	7		ns
$t_{h(CLKH-NWAITV)}$	FSMC_NWAIT valid after FSMC_CLK high	2		ns
$t_{d(CLKL-NBLH)}$	FSMC_CLK low to FSMC_NBL high	1		ns

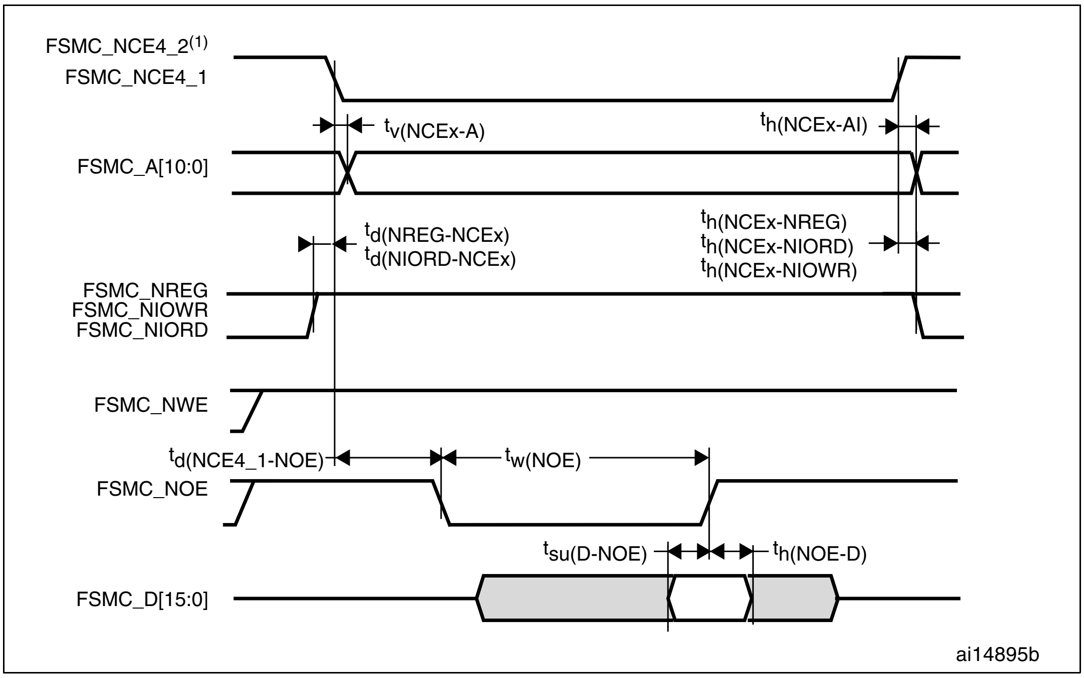
1. V_{DD_IO} = V and C_L = 15 pF.
2. Based on characterization, not tested in production.

PC Card/CompactFlash controller waveforms and timings

Figure 28 through *Figure 33* represent synchronous waveforms and *Table 39* provides the corresponding timings. The results shown in this table are obtained with the following FSMC configuration:

- COM.FSMC_SetupTime = 0x04;
- COM.FSMC_WaitSetupTime = 0x07;
- COM.FSMC_HoldSetupTime = 0x04;
- COM.FSMC_HiZSetupTime = 0x00;
- ATT.FSMC_SetupTime = 0x04;
- ATT.FSMC_WaitSetupTime = 0x07;
- ATT.FSMC_HoldSetupTime = 0x04;
- ATT.FSMC_HiZSetupTime = 0x00;
- IO.FSMC_SetupTime = 0x04;
- IO.FSMC_WaitSetupTime = 0x07;
- IO.FSMC_HoldSetupTime = 0x04;
- IO.FSMC_HiZSetupTime = 0x00;
- TCLRSetupTime = 0;
- TARSetupTime = 0;

Figure 28. PC Card/CompactFlash controller waveforms for common memory read access



1. FSMC_NCE4_2 remains high (inactive during 8-bit access.

Figure 29. PC Card/CompactFlash controller waveforms for common memory write access

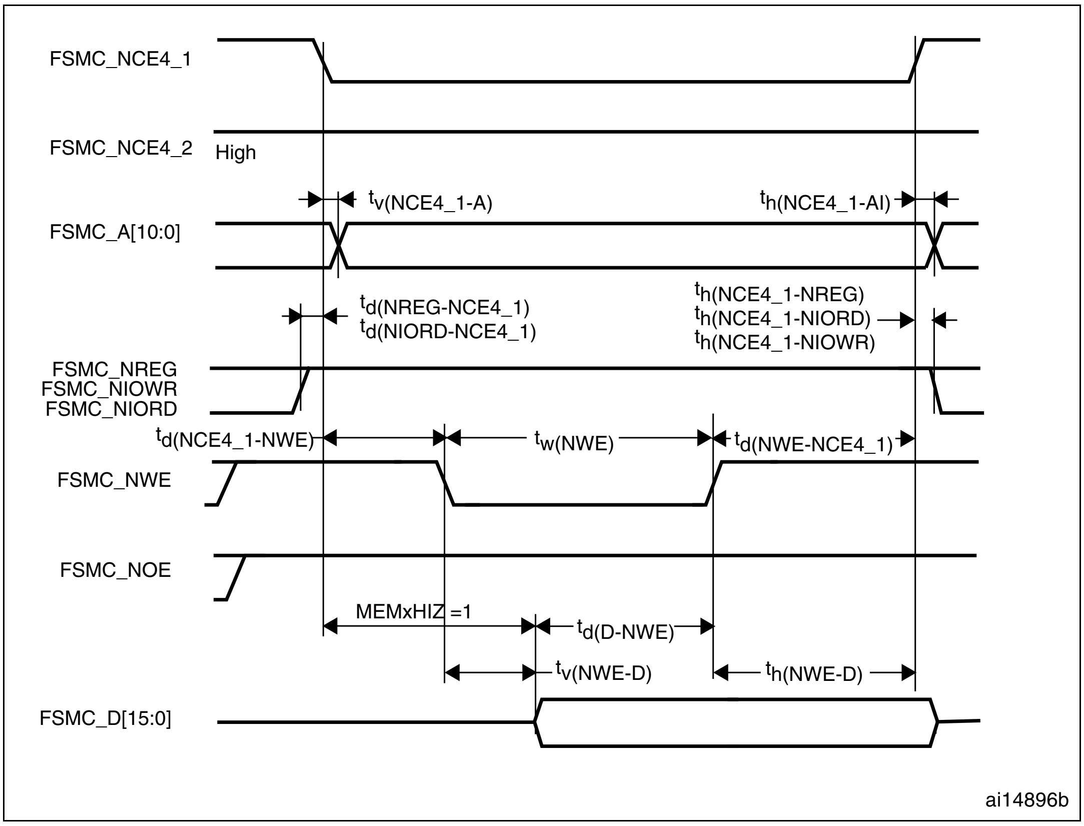
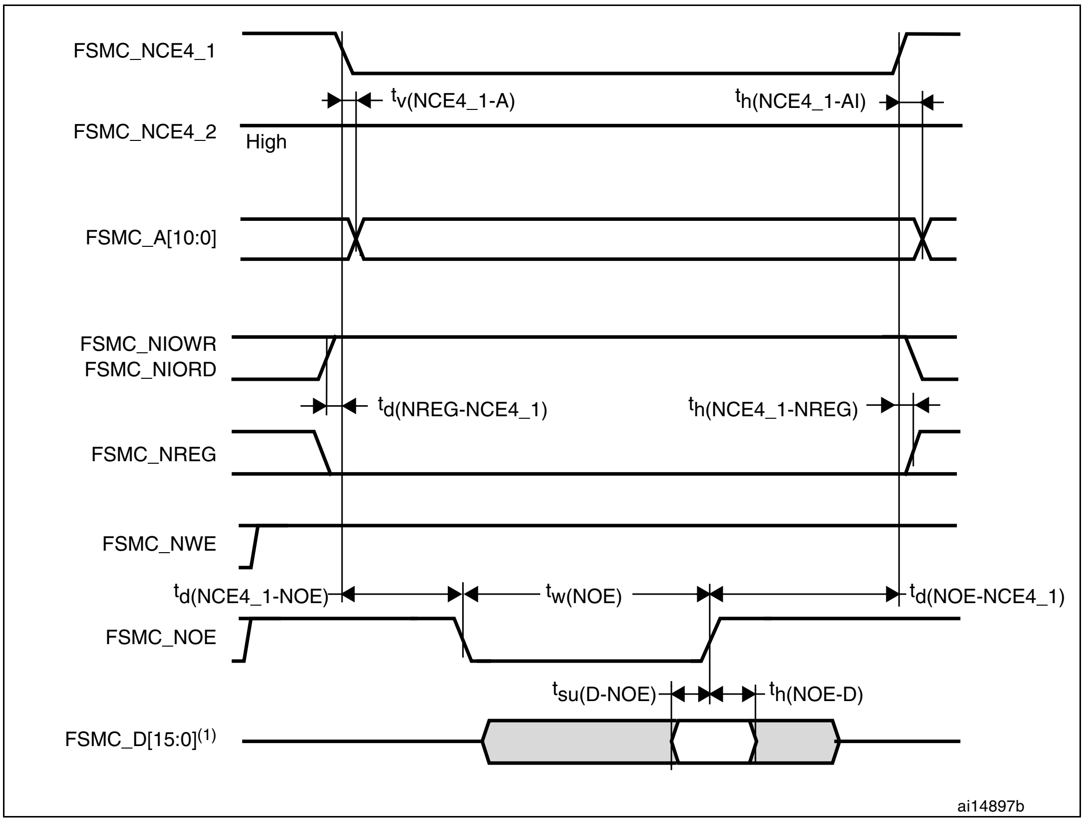
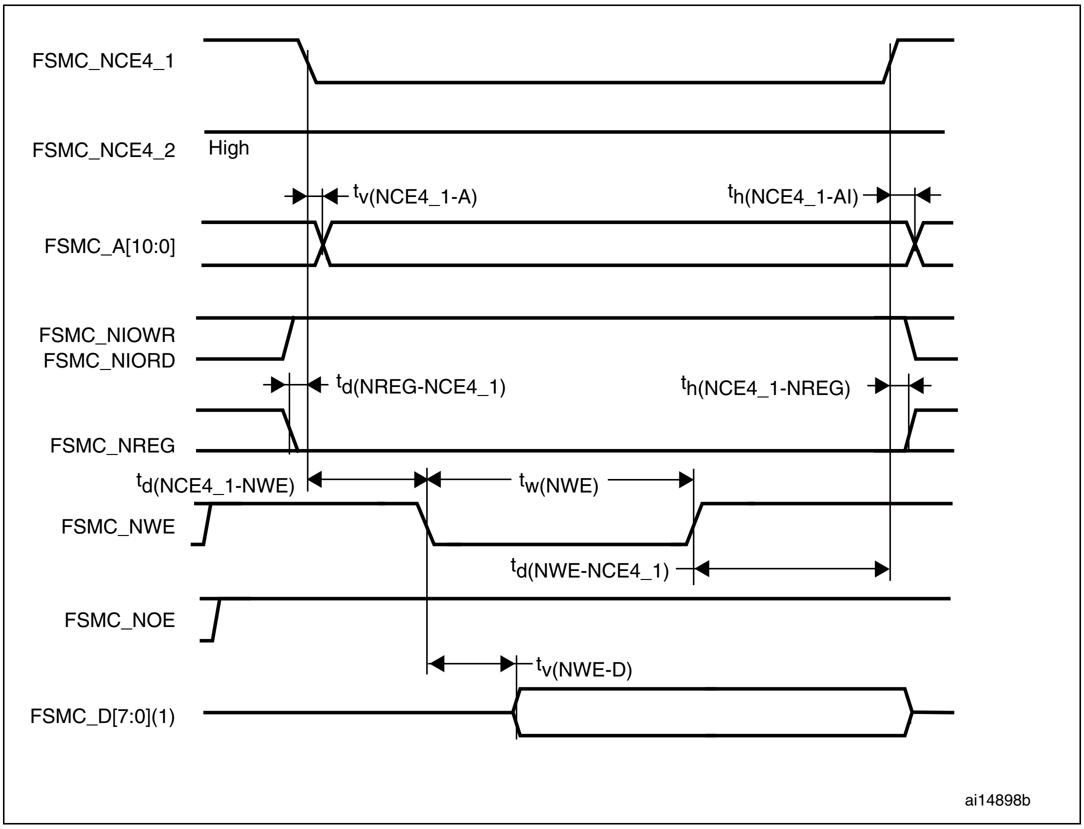


Figure 30. PC Card/CompactFlash controller waveforms for attribute memory read access



1. Only data bits 0...7 are read (bits 8...15 are disregarded).

Figure 31. PC Card/CompactFlash controller waveforms for attribute memory write access



1. Only data bits 0...7 are driven (bits 8...15 remains HiZ).

Figure 32. PC Card/CompactFlash controller waveforms for I/O space read access

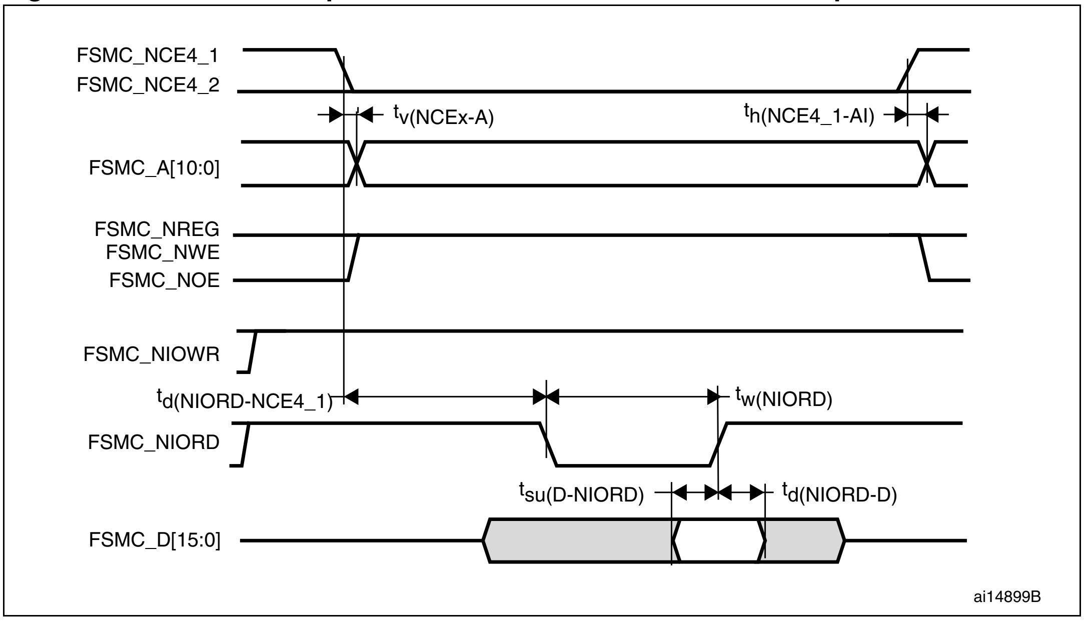


Figure 33. PC Card/CompactFlash controller waveforms for I/O space write access

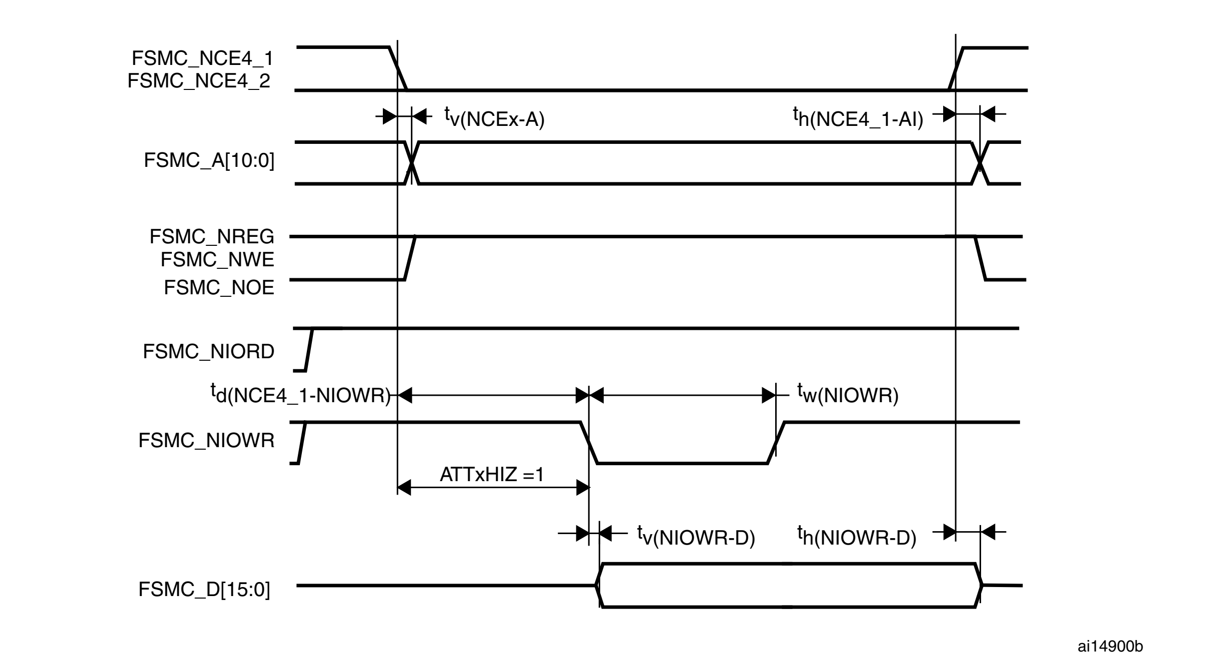


Table 39. Switching characteristics for PC Card/CF read and write cycles(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{v(NCEx-A)}$ $t_{v(NCE4\_1-A)}$	FSMC_NCEx low (x = 4_1/4_2) to FSMC_Ay valid (y = 0...10) FSMC_NCE4_1 low (x = 4_1/4_2) to FSMC_Ay valid (y = 0...10)		0	ns
$t_{h(NCEx-AI)}$ $t_{h(NCE4\_1-AI)}$	FSMC_NCEx high (x = 4_1/4_2) to FSMC_Ax invalid (x = 0...10) FSMC_NCE4_1 high (x = 4_1/4_2) to FSMC_Ax invalid (x = 0...10)	2.5		ns
$t_{d(NREG-NCEx)}$ $t_{d(NREG-NCE4\_1)}$	FSMC_NCEx low to FSMC_NREG valid FSMC_NCE4_1 low to FSMC_NREG valid		5	ns
$t_{h(NCEx-NREG)}$ $t_{h(NCE4\_1-NREG)}$	FSMC_NCEx high to FSMC_NREG invalid FSMC_NCE4_1 high to FSMC_NREG invalid	$T_{HCLK} + 3$		ns
$t_{d(NCE4\_1-NOE)}$	FSMC_NCE4_1 low to FSMC_NOE low		$5T_{HCLK} + 2$	ns
$t_{w(NOE)}$	FSMC_NOE low width	$8T_{HCLK} - 1.5$	$8T_{HCLK} + 1$	ns
$t_{d(NOE-NCE4\_1}$	FSMC_NOE high to FSMC_NCE4_1 high	$5T_{HCLK} + 2$		ns
$t_{su(D-NOE)}$	FSMC_D[15:0] valid data before FSMC_NOE high	25		ns
$t_{h(NOE-D)}$	FSMC_D[15:0] valid data after FSMC_NOE high	15		ns
$t_{w(NWE)}$	FSMC_NWE low width	$8T_{HCLK} - 1$	$8T_{HCLK} + 2$	ns
$t_{d(NWE-NCE4\_1)}$	FSMC_NWE high to FSMC_NCE4_1 high	$5T_{HCLK} + 2$		ns
$t_{d(NCE4\_1-NWE)}$	FSMC_NCE4_1 low to FSMC_NWE low		$5T_{HCLK} + 1.5$	ns
$t_{v(NWE-D)}$	FSMC_NWE low to FSMC_D[15:0] valid		0	ns
$t_{h(NWE-D)}$	FSMC_NWE high to FSMC_D[15:0] invalid	$11T_{HCLK}$		ns

Table 39. Switching characteristics for PC Card/CF read and write cycles(1)(2) (continued)

Symbol	Parameter	Min	Max	Unit
$t_{d(D-NWE)}$	FSMC_D[15:0] valid before FSMC_NWE high	$13T_{HCLK}$		ns
$t_{w(NIOWR)}$	FSMC_NIOWR low width	$8T_{HCLK} + 3$		ns
$t_{v(NIOWR-D)}$	FSMC_NIOWR low to FSMC_D[15:0] valid		$5T_{HCLK} +1$	ns
$t_{h(NIOWR-D)}$	FSMC_NIOWR high to FSMC_D[15:0] invalid	$11T_{HCLK}$		ns
$t_{d(NCE4\_1-NIOWR)}$	FSMC_NCE4_1 low to FSMC_NIOWR valid		$5T_{HCLK}+3ns$	ns
$t_{h(NCEx-NIOWR)}$ $t_{h(NCE4\_1-NIOWR)}$	FSMC_NCEx high to FSMC_NIOWR invalid FSMC_NCE4_1 high to FSMC_NIOWR invalid	$5T_{HCLK} - 5$		ns
$t_{d(NIORD-NCEx)}$ $t_{d(NIORD-NCE4\_1)}$	FSMC_NCEx low to FSMC_NIORD valid FSMC_NCE4_1 low to FSMC_NIORD valid		$5T_{HCLK} + 2.5$	ns
$t_{h(NCEx-NIORD)}$ $t_{h(NCE4\_1-NIORD)}$	FSMC_NCEx high to FSMC_NIORD invalid FSMC_NCE4_1 high to FSMC_NIORD invalid	$5T_{HCLK} - 5$		ns
$t_{su(D-NIORD)}$	FSMC_D[15:0] valid before FSMC_NIORD high	4.5		ns
$t_{d(NIORD-D)}$	FSMC_D[15:0] valid after FSMC_NIORD high	9		ns
$t_{w(NIORD)}$	FSMC_NIORD low width	$8T_{HCLK} + 2$		ns

1. V_{DD_IO} = V and C_L = 15 pF.
2. Based on characterization, not tested in production.

NAND controller waveforms and timings

Figure 34 through *Figure 37* represent synchronous waveforms and *Table 40* provides the corresponding timings. The results shown in this table are obtained with the following FSMC configuration:

- COM.FSMC_SetupTime = 0x01;
- COM.FSMC_WaitSetupTime = 0x03;
- COM.FSMC_HoldSetupTime = 0x02;
- COM.FSMC_HiZSetupTime = 0x01;
- ATT.FSMC_SetupTime = 0x01;
- ATT.FSMC_WaitSetupTime = 0x03;
- ATT.FSMC_HoldSetupTime = 0x02;
- ATT.FSMC_HiZSetupTime = 0x01;
- Bank = FSMC_Bank_NAND;
- MemoryDataWidth = FSMC_MemoryDataWidth_16b;
- ECC = FSMC_ECC_Enable;
- ECCPageSize = FSMC_ECCPageSize_512Bytes;
- TCLRSetupTime = 0;
- TARSetupTime = 0;

Figure 34. NAND controller waveforms for read access

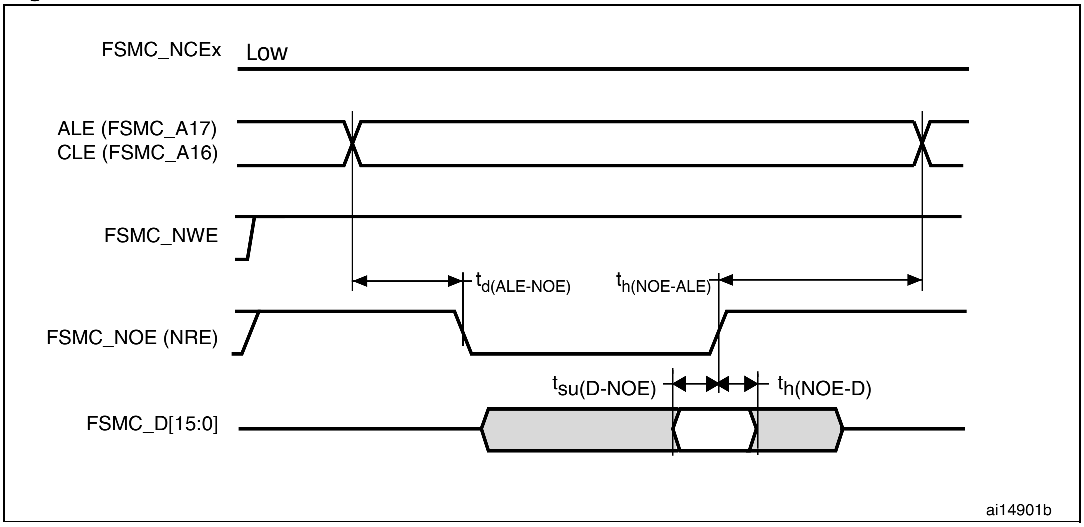


Figure 35. NAND controller waveforms for write access

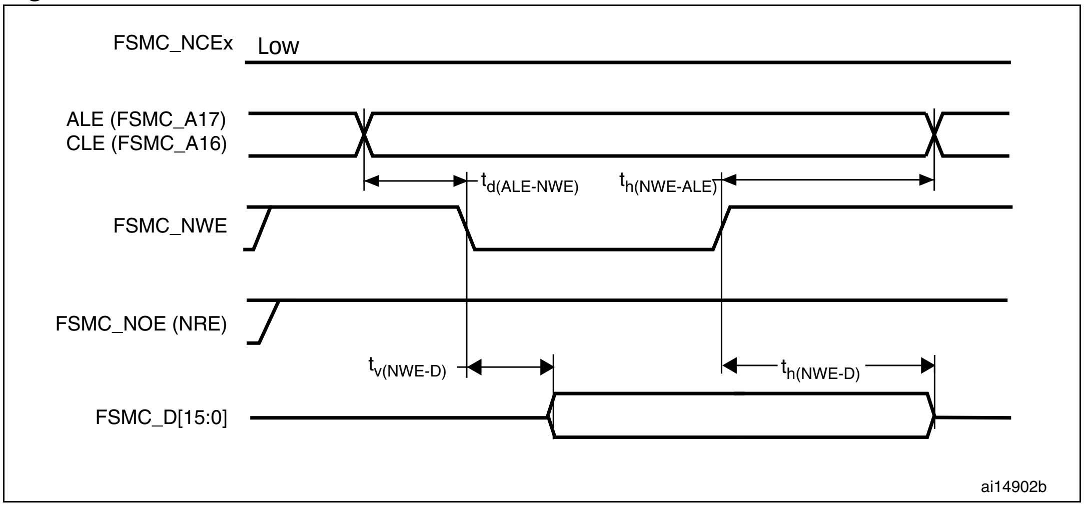


Figure 36. NAND controller waveforms for common memory read access

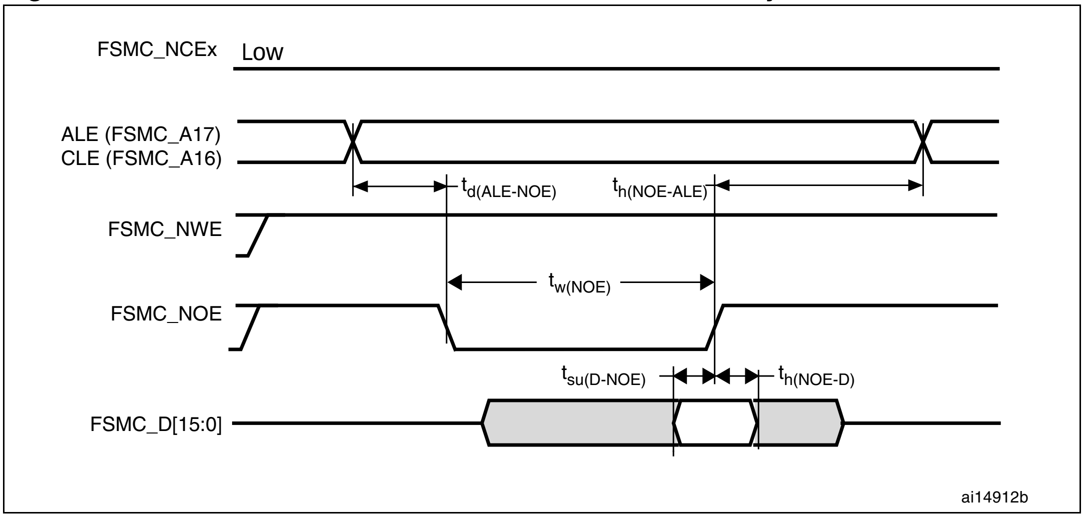


Figure 37. NAND controller waveforms for common memory write access

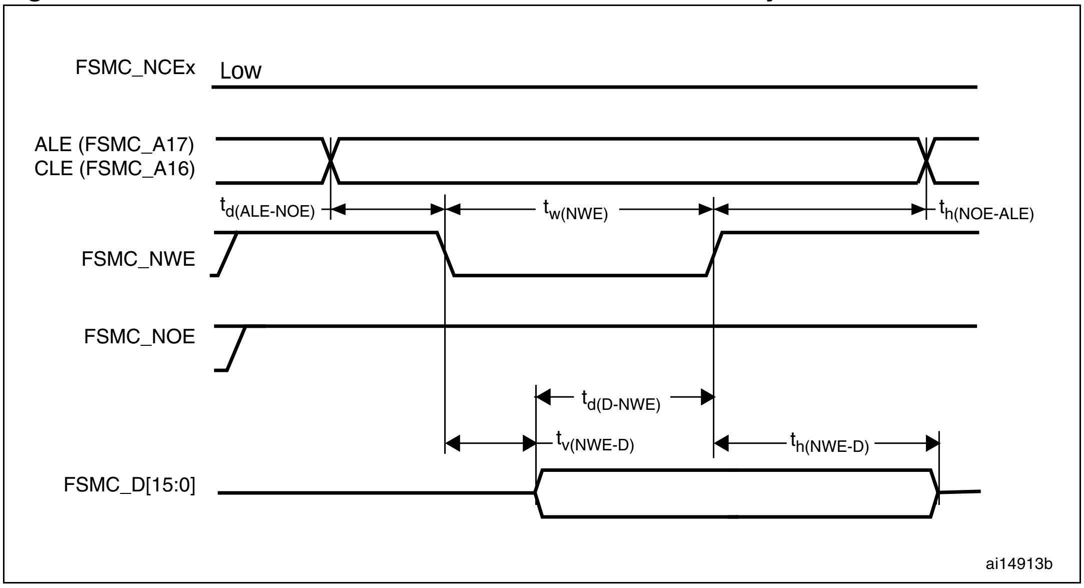


Table 40. Switching characteristics for NAND Flash read and write cycles(1)

Symbol	Parameter	Min	Max	Unit
$t_{d(D-NWE)}$ (2)	FSMC_D[15:0] valid before FSMC_NWE high	$6T_{HCLK} + 12$		ns
$t_{w(NOE)}$ (2)	FSMC_NOE low width	$4T_{HCLK} - 1.5$	$4T_{HCLK} + 1.5$	ns
$t_{su(D-NOE)}$ (2)	FSMC_D[15:0] valid data before FSMC_NOE high	25		ns
$t_{h(NOE-D)}$ (2)	FSMC_D[15:0] valid data after FSMC_NOE high	14		ns
$t_{w(NWE)}$ (2)	FSMC_NWE low width	$4T_{HCLK} - 1$	$4T_{HCLK} + 2.5$	ns
$t_{v(NWE-D)}$ (2)	FSMC_NWE low to FSMC_D[15:0] valid		0	ns
$t_{h(NWE-D)}$ (2)	FSMC_NWE high to FSMC_D[15:0] invalid	$10T_{HCLK} + 4$		ns
$t_{d(ALE-NWE)}$ (3)	FSMC_ALE valid before FSMC_NWE low		$3T_{HCLK} + 1.5$	ns
$t_{h(NWE-ALE)}$ (3)	FSMC_NWE high to FSMC_ALE invalid	$3T_{HCLK} + 4.5$		ns
$t_{d(ALE-NOE)}$ (3)	FSMC_ALE valid before FSMC_NOE low		$3T_{HCLK} + 2$	ns
$t_{h(NOE-ALE)}$ (3)	FSMC_NWE high to FSMC_ALE invalid	$3T_{HCLK} + 4.5$		ns

1. V_{DD_IO} = V and C_L = 15 pF.
2. Based on characterization, not tested in production.
3. Guaranteed by design, not tested in production.

5.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (Electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 1000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 41*. They are based on the EMS levels and classes defined in application note AN1709.

Table 41. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP144, T_A = +25 °C, f_{HCLK}= 36 MHz conforms to IEC 1000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP144, T_A = +25 °C, f_{HCLK} = 36 MHz conforms to IEC 1000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and pre qualification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second. To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device is monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with SAE J 1752/3 standard which specifies the test board and the pin loading.

Table 42. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]	Unit
				8/36 MHz	
S_{EMI}	Peak level	V_{DD} = 3.3 V, T_A = 25 °C, LQFP144 package compliant with SAE J 1752/3	0.1 MHz to 30 MHz	8	dBμV
			30 MHz to 130 MHz	27	
			130 MHz to 1 GHz	26	
			SAE EMI Level	4	-

5.3.12 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 43. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to JESD22-A114	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to JESD22-C101	II	500	

1. Based on characterization results, not tested in production.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78 IC latch-up standard.

Table 44. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +85 °C conforming to JESD78A	II level A

5.3.13 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 45* are derived from tests performed under the conditions summarized in *Table 10*. All I/Os are CMOS and TTL compliant.

Table 45. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage	TTL ports	–0.5		0.8	V
V_{IH}	Standard IO input high level voltage		2		V_{DD}+0.5	
	IO FT[1] input high level voltage		2		5.5V	
V_{IL}	Input low level voltage	CMOS ports	–0.5		0.35 V_{DD}	V
V_{IH}	Input high level voltage		0.65 V_{DD}		V_{DD}+0.5	
V_{hys}	Standard IO Schmitt trigger voltage hysteresis[2]		200			mV
	IO FT Schmitt trigger voltage hysteresis[2]		5% V_{DD}[3]			mV
I_{lkg}	Input leakage current [3]	$V_{SS} \leq V_{IN} \leq V_{DD}$ Standard I/Os			±1	µA
		V_{IN} = 5 V I/O FT			3	
R_{PU}	Weak pull-up equivalent resistor[4]	$V_{IN} = V_{SS}$	30	40	50	kΩ
R_{PD}	Weak pull-down equivalent resistor[5]	$V_{IN} = V_{DD}$	30	40	50	kΩ
C_{IO}	I/O pin capacitance			5		pF

1. FT = Five-volt tolerant.
2. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization, not tested in production.
3. With a minimum of 100 mV.
4. Leakage could be higher than max. if negative current is injected on adjacent pins.
5. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimum (~10% order).

All I/Os are CMOS and TTL compliant (no software configuration required), their characteristics consider the most strict CMOS-technology or TTL parameters:

- For V_{IH}:
  - if V_{DD} is in the [2.00 V - 3.08 V] range: CMOS characteristics but TTL included
  - if V_{DD} is in the [3.08 V - 3.60 V] range: TTL characteristics but CMOS included
- For V_{IL}:
  - if V_{DD} is in the [2.00 V - 2.28 V] range: TTL characteristics but CMOS included
  - if V_{DD} is in the [2.28 V - 3.60 V] range: CMOS characteristics but TTL included

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink +20 mA (with a relaxed V_{OL}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in Section 5.2:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating I_{VDD} (see Table 8).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating I_{VSS} (see Table 8).

Output voltage levels

Unless otherwise specified, the parameters given in Table 46 are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in Table 10. All I/Os are CMOS and TTL compliant.

Table 46. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(1)	Output Low level voltage for an I/O pin when 8 pins are sunk at the same time	TTL port, I_{IO} = +8 mA, 2.7 V < V_{DD} < 3.6 V		0.4	V
V_{OH}(2)	Output High level voltage for an I/O pin when 8 pins are sourced at the same time		V_{DD}–0.4		
V_{OL}(1)	Output low level voltage for an I/O pin when 8 pins are sunk at the same time	CMOS port I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V		0.4	V
V_{OH}(2)	Output high level voltage for an I/O pin when 8 pins are sourced at the same time		2.4		
V_{OL}(1)	Output low level voltage for an I/O pin when 8 pins are sunk at the same time	I_{IO} = +20 mA(3) 2.7 V < V_{DD} < 3.6 V		1.3	V
V_{OH} (2)	Output high level voltage for an I/O pin when 8 pins are sourced at the same time		V_{DD}–1.3		
V_{OL}(1)	Output low level voltage for an I/O pin when 8 pins are sunk at the same time	I_{IO} = +6 mA(3) 2 V < V_{DD} < 2.7 V		0.4	V
V_{OH}(2)	Output high level voltage for an I/O pin when 8 pins are sourced at the same time		V_{DD}–0.4		

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in Table 8 and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in Table 8 and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
3. Based on characterization data, not tested in production.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 38* and *Table 47*, respectively.

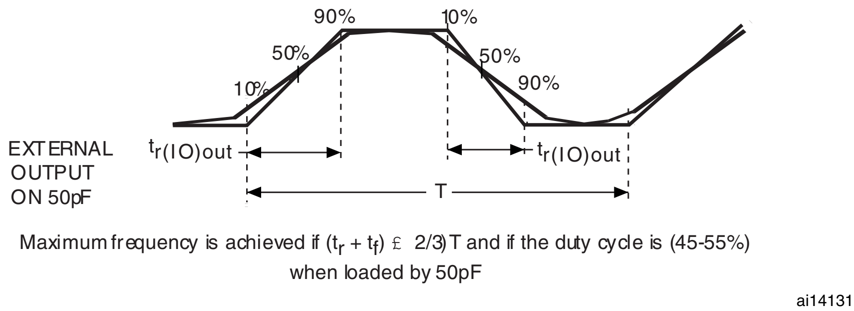
Unless otherwise specified, the parameters given in *Table 47* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

Table 47. I/O AC characteristics(1)

<table>
<tr><th>MODEx [1:0] bit value(1)</th><th>Symbol</th><th>Parameter</th><th>Conditions</th><th>Max</th><th>Unit</th></tr>
<tr><td rowspan="3">10</td><td>$f_{max(IO)out}$</td><td>Maximum frequency(2)</td><td>C_L = 50 pF, V_{DD} = 2 V to 3.6 V</td><td>2</td><td>MHz</td></tr>
<tr><td>$t_{f(IO)out}$</td><td>Output high to low level fall time</td><td rowspan="2">C_L = 50 pF, V_{DD} = 2 V to 3.6 V</td><td>125(3)</td><td rowspan="2">ns</td></tr>
<tr><td>$t_{r(IO)out}$</td><td>Output low to high level rise time</td><td>125(3)</td></tr>
<tr><td rowspan="3">01</td><td>$f_{max(IO)out}$</td><td>Maximum frequency(2)</td><td>C_L= 50 pF, V_{DD} = 2 V to 3.6 V</td><td>10</td><td>MHz</td></tr>
<tr><td>$t_{f(IO)out}$</td><td>Output high to low level fall time</td><td rowspan="2">C_L= 50 pF, V_{DD} = 2 V to 3.6 V</td><td>25(3)</td><td rowspan="2">ns</td></tr>
<tr><td>$t_{r(IO)out}$</td><td>Output low to high level rise time</td><td>25(3)</td></tr>
<tr><td rowspan="9">11</td><td rowspan="3">$F_{max(IO)out}$</td><td rowspan="3">Maximum Frequency(2)</td><td>C_L= 30 pF, V_{DD} = 2.7 V to 3.6 V</td><td>50</td><td>MHz</td></tr>
<tr><td>C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V</td><td>30</td><td>MHz</td></tr>
<tr><td>C_L = 50 pF, V_{DD} = 2 V to 2.7 V</td><td>20</td><td>MHz</td></tr>
<tr><td rowspan="3">$t_{f(IO)out}$</td><td rowspan="3">Output high to low level fall time</td><td>C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V</td><td>5(3)</td><td rowspan="6">ns</td></tr>
<tr><td>C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V</td><td>8(3)</td></tr>
<tr><td>C_L = 50 pF, V_{DD} = 2 V to 2.7 V</td><td>12(3)</td></tr>
<tr><td rowspan="3">$t_{r(IO)out}$</td><td rowspan="3">Output low to high level rise time</td><td>C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V</td><td>5(3)</td></tr>
<tr><td>C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V</td><td>8(3)</td></tr>
<tr><td>C_L = 50 pF, V_{DD} = 2 V to 2.7 V</td><td>12(3)</td></tr>
<tr><td>-</td><td>t_{EXTIpw}</td><td>Pulse width of external signals detected by the EXTI controller</td><td></td><td>10</td><td>ns</td></tr>
</table>

1. The I/O speed is configured using the MODEx[1:0] bits. Refer to the STM32F10x reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in *Figure 38*.
3. Guaranteed by design, not tested in production.

Figure 38. I/O AC characteristics definition



5.3.14 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 45*).

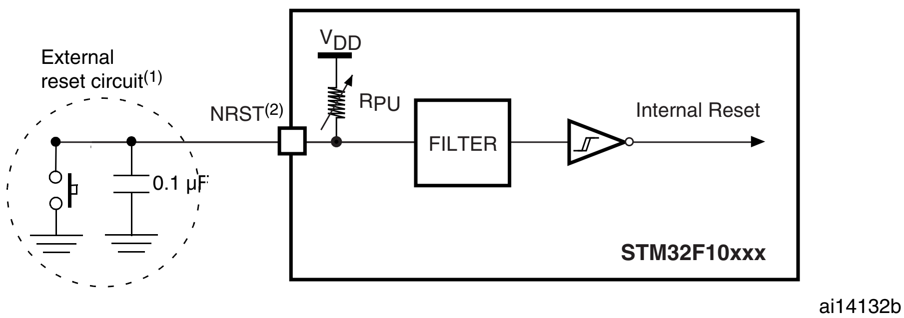
Unless otherwise specified, the parameters given in *Table 48* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

Table 48. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$ (1)	NRST Input low level voltage		–0.5		0.8	V
$V_{IH(NRST)}$ (1)	NRST Input high level voltage		2		V_{DD}+0.5	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis			200		mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F(NRST)}$ (1)	NRST Input filtered pulse				100	ns
$V_{NF(NRST)}$ (1)	NRST Input not filtered pulse		300			ns

1. Guaranteed by design, not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

Figure 39. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 48*. Otherwise the reset will not be taken into account by the device.

5.3.15 TIM timer characteristics

The parameters given in *Table 49* are guaranteed by design.

Refer to *Section 5.3.13: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 49. TIMx[1] characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time		1		$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 36 MHz	27.8		ns
f_{EXT}	Timer external clock frequency on CH1 to CH4		0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 36 MHz	0	18	MHz
Res_{TIM}	Timer resolution			16	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected		1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 36 MHz	0.0278	1820	µs
t_{MAX_COUNT}	Maximum possible count			65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 36 MHz		119.2	s

1. TIMx is used as a general term to refer to the TIM1, TIM2, TIM3 and TIM4 timers.

5.3.16 Communications interfaces

I²C interface characteristics

Unless otherwise specified, the parameters given in *Table 50* are derived from tests performed under ambient temperature, f_{PCLK1} frequency and V_{DD} supply voltage conditions summarized in *Table 10*.

The STM32F101xC, STM32F101xD and STM32F101xE access line I²C interface meets the requirements of the standard I²C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not "true" open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

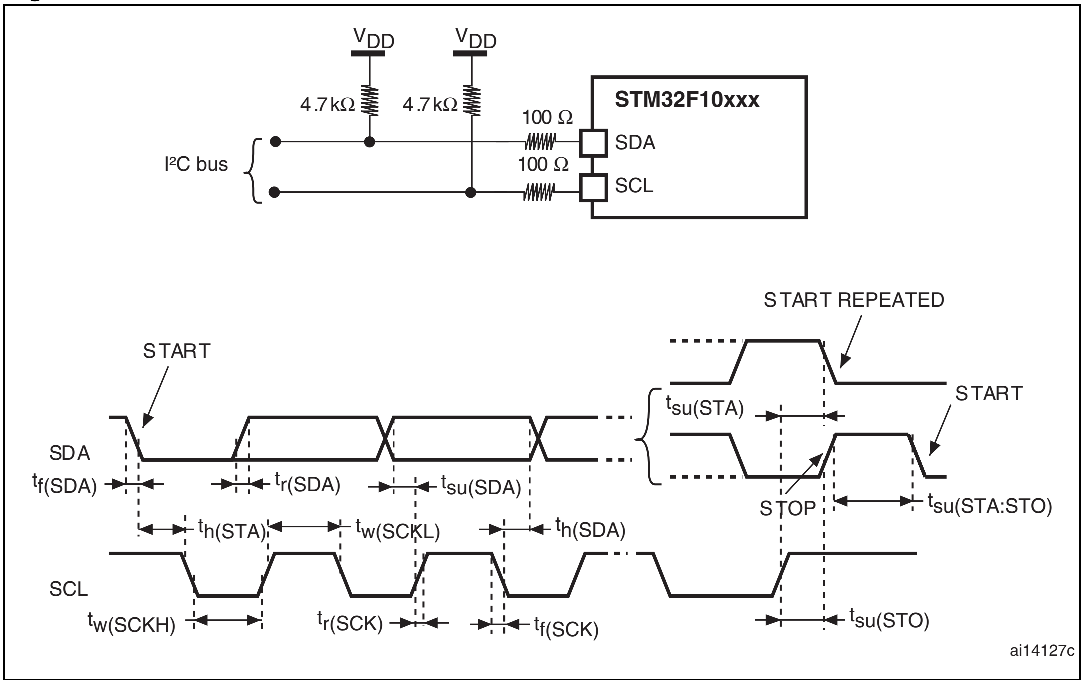
The I²C characteristics are described in *Table 50*. Refer also to *Section 5.3.13: I/O port characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

Table 50. I^2C characteristics

Symbol	Parameter	Standard mode I^2C(1)		Fast mode I^2C(1)(2)		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		µs
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0(3)		0(4)	900(3)	ns
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time		1000	$20+0.1C_b$	300	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time		300		300	ns
$t_{h(STA)}$	Start condition hold time	4.0		0.6		µs
$t_{su(STA)}$	Repeated Start condition setup time	4.7		0.6		µs
$t_{su(STO)}$	Stop condition setup time	4.0		0.6		µs
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7		1.3		µs
C_b	Capacitive load for each bus line		400		400	pF

1. Guaranteed by design, not tested in production.
2. f_{PCLK1} must be higher than 2 MHz to achieve the maximum standard mode I^2C frequency. It must be higher than 4 MHz to achieve the maximum fast mode I^2C frequency.
3. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.

Figure 40. I²C bus AC waveforms and measurement circuit(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Table 51. SCL frequency (f_{PCLK1}= 36 MHz, V_{DD} = 3.3 V)(1)(2)

f_{SCL} (kHz)	I2C_CCR value R_P = 4.7 kΩ
400	0x801E
300	0x8028
200	0x803C
100	0x00B4
50	0x0168
20	0x0384

1. R_P = External pull-up resistance, f_{SCL} = I²C speed,
2. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed ±2%. These variations depend on the accuracy of the external components used to design the application.

SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 52* are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 10*.
Refer to *Section 5.3.13: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 52. SPI characteristics[1]

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode		18	MHz
		Slave mode		18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF		8	ns
$t_{su(NSS)}$[2]	NSS setup time	Slave mode	$4t_{PCLK}$		
$t_{h(NSS)}$[2]	NSS hold time	Slave mode	60		
$t_{w(SCKH)}$[2] $t_{w(SCKL)}$[2]	SCK high and low time	Master mode, f_{PCLK} = 36 MHz, presc = 4	50	60	
$t_{su(MI)}$[2] $t_{su(SI)}$[2]	Data input setup time	Master mode - SPI1	3		
		Master mode - SPI2	5		
		Slave mode	4		
$t_{h(MI)}$[2]	Data input hold time	Master mode - SPI1	4		
		Master mode - SPI2	6		
$t_{h(SI)}$[2]		Slave mode	5		
$t_{a(SO)}$[2][3]	Data output access time	Slave mode, f_{PCLK} = 36 MHz, presc = 4	0	55	
		Slave mode, f_{PCLK} = 20 MHz		$4t_{PCLK}$	
$t_{dis(SO)}$[2][4]	Data output disable time	Slave mode	10		
$t_{v(SO)}$[2][1]	Data output valid time	Slave mode (after enable edge)		25	
$t_{v(MO)}$[2][1]	Data output valid time	Master mode (after enable edge)		6	
$t_{h(SO)}$[2]	Data output hold time	Slave mode (after enable edge)	25		
$t_{h(MO)}$[2]		Master mode (after enable edge)	6		

1. Remapped SPI1 characteristics to be determined.
2. Based on characterization, not tested in production.
3. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
4. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

Figure 41. SPI timing diagram - slave mode and CPHA=0

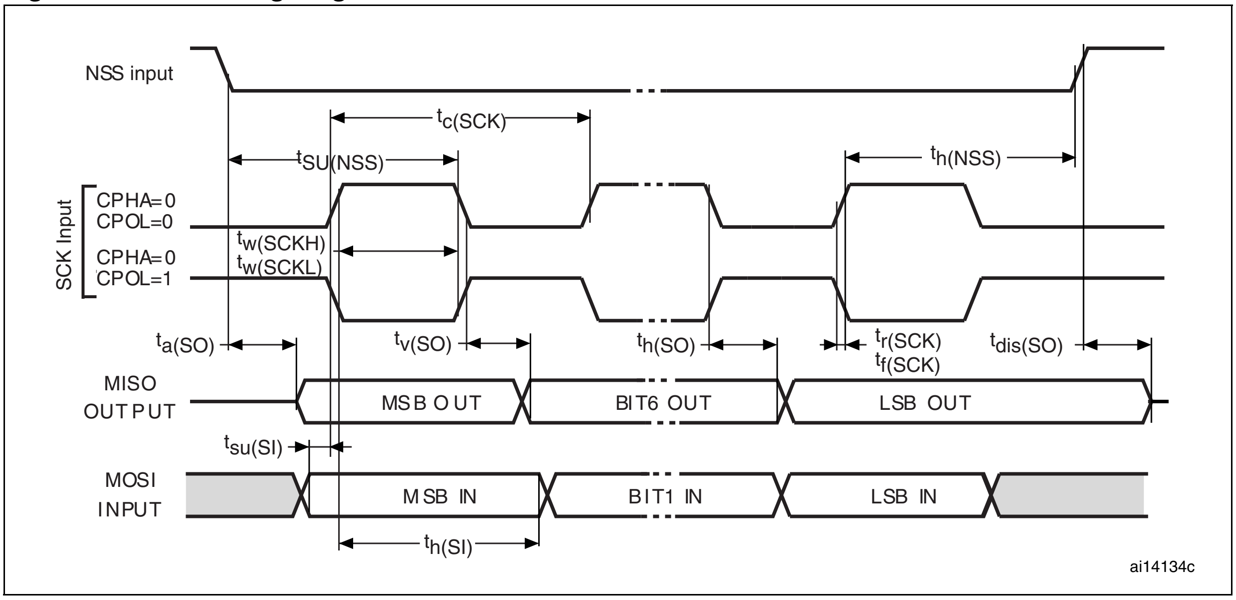
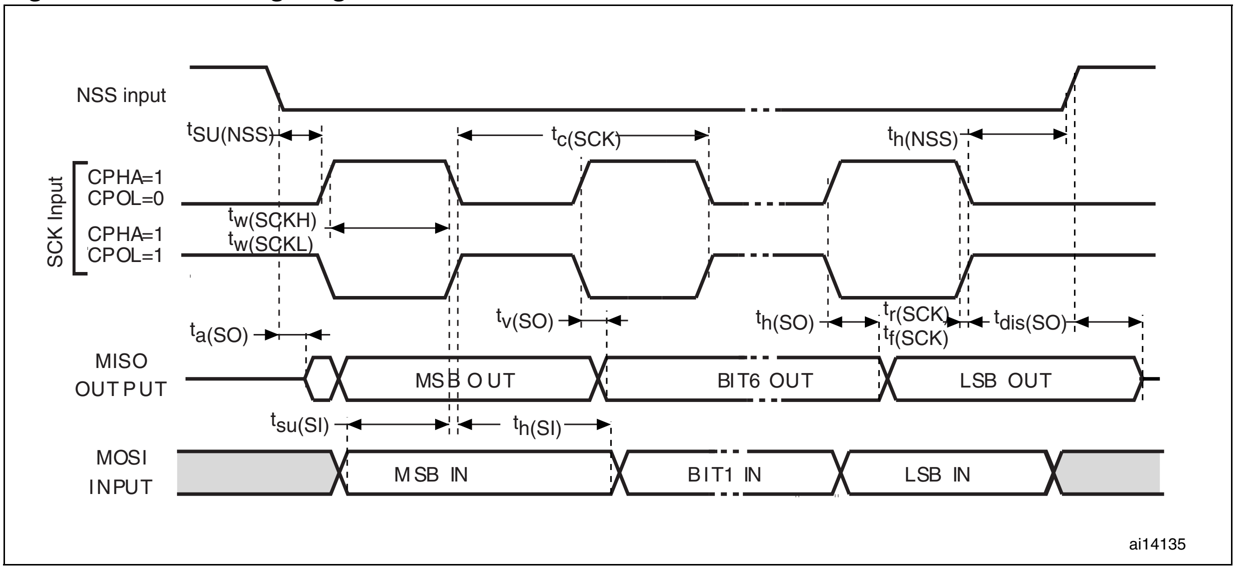
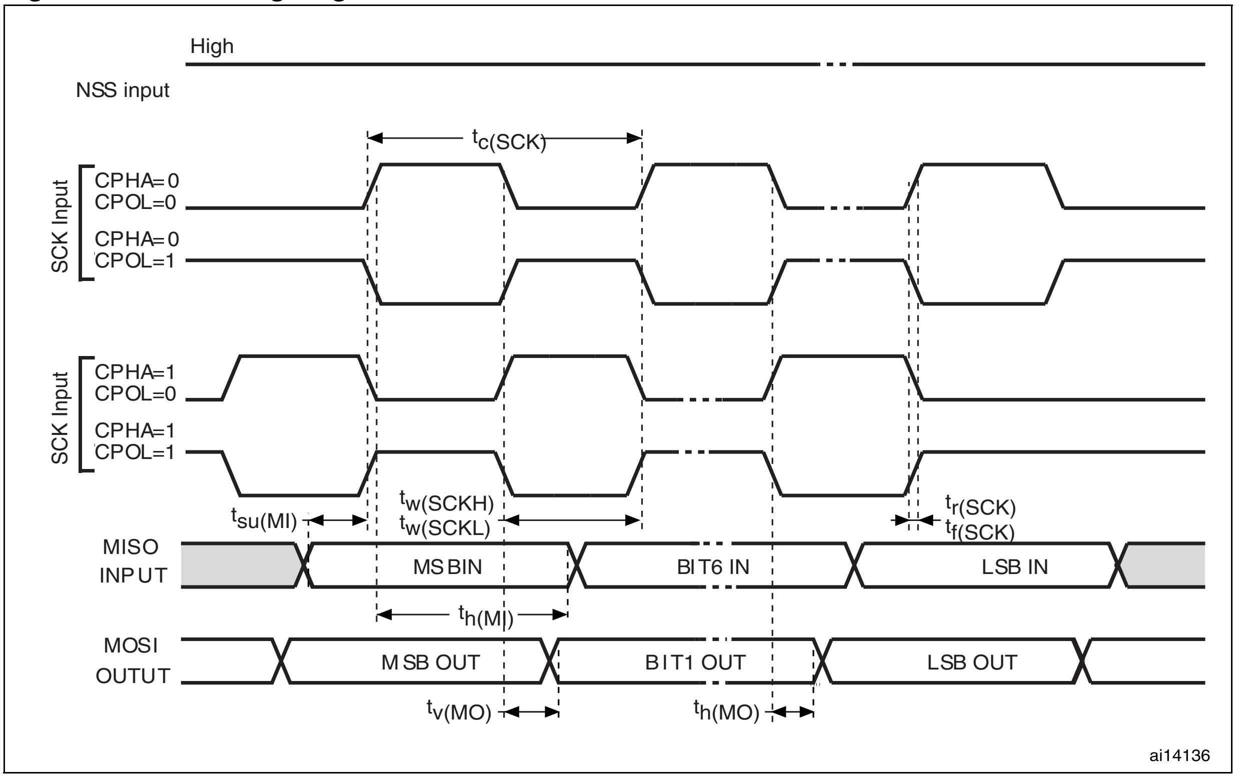


Figure 42. SPI timing diagram - slave mode and CPHA=1(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 43. SPI timing diagram - master mode(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

5.3.17 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 53* are derived from tests performed under ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 10*.

Note: It is recommended to perform a calibration after each power-up.

Table 53. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply		2.4		3.6	V
V_{REF+}	Positive reference voltage		2.4		V_{DDA}	V
I_{VREF}	Current on the V_{REF} input pin			160(1)	220(1)	µA
f_{ADC}	ADC clock frequency		0.6		14	MHz
f_S(2)	Sampling rate		0.05		1	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 14 MHz			823	kHz
					17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range(3)		0 (V_{SSA} or V_{REF-} tied to ground)		V_{REF+}	V
R_{AIN}(2)	External input impedance		See *Equation 1* and *Table 54*			kΩ
R_{ADC}(2)	Sampling switch resistance				1	kΩ
C_{ADC}(2)	Internal sample and hold capacitor				12	pF
t_{CAL}(2)	Calibration time	f_{ADC} = 14 MHz	5.9			µs
			83			$1/f_{ADC}$
t_{lat}(2)	Injection trigger conversion latency	f_{ADC} = 14 MHz			0.214	µs
					3(4)	$1/f_{ADC}$
t_{latr}(2)	Regular trigger conversion latency	f_{ADC} = 14 MHz			0.143	µs
					2(4)	$1/f_{ADC}$
t_S(2)	Sampling time	f_{ADC} = 14 MHz	0.107		17.1	µs
			1.5		239.5	$1/f_{ADC}$
t_{STAB}(2)	Power-up time		0	0	1	µs
t_{CONV}(2)	Total conversion time (including sampling time)	f_{ADC} = 14 MHz	1		18	µs
			14 to 252 (t_S for sampling +12.5 for successive approximation)			$1/f_{ADC}$

1. Based on characterization results, not tested in production.
2. Guaranteed by design, not tested in production.
3. V_{REF+} can be internally connected to V_{DDA} and V_{REF-} can be internally connected to V_{SSA}, depending on the package. Refer to *Section 3: Pinouts and pin descriptions* for further details.
4. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 53*.

Equation 1: R_{AIN} max formula:

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 54. R_{AIN} max for f_{ADC} = 14 MHz[(1)]

T_s (cycles)	t_S (µs)	R_{AIN} max (kΩ)
1.5	0.11	1.2
7.5	0.54	10
13.5	0.96	19
28.5	2.04	41
41.5	2.96	60
55.5	3.96	80
71.5	5.11	104
239.5	17.1	350

1. Guaranteed by design, not tested in production.

Table 55. ADC accuracy - limited test conditions[(1)(2)]

Symbol	Parameter	Test conditions	Typ	Max[(3)]	Unit
ET	Total unadjusted error	f_{PCLK2} = 28 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 3 V to 3.6 V, T_A = 25 °C Measurements made after ADC calibration $V_{REF+} = V_{DDA}$	±1.3	±2	LSB
EO	Offset error		±1	±1.5	
EG	Gain error		±0.5	±1.5	
ED	Differential linearity error		±0.7	±1	
EL	Integral linearity error		±0.8	±1.5	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 5.3.13* does not affect the ADC accuracy.
3. Based on characterization, not tested in production.

Table 56. ADC accuracy[(1) (2)(3)]

Symbol	Parameter	Test conditions	Typ	Max[(4)]	Unit
ET	Total unadjusted error	f_{PCLK2} = 28 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 2.4 V to 3.6 V Measurements made after ADC calibration	±2	±5	LSB
EO	Offset error		±1.5	±2.5	
EG	Gain error		±1.5	±3	
ED	Differential linearity error		±1	±2	
EL	Integral linearity error		±1.5	±3	

1. ADC DC accuracy values are measured after internal calibration.
2. Better performance could be achieved in restricted V_{DD}, frequency, V_{REF} and temperature ranges.
3. ADC accuracy vs. negative injection current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 5.3.13* does not affect the ADC accuracy.
4. Based on characterization, not tested in production.

Figure 44. ADC accuracy characteristics

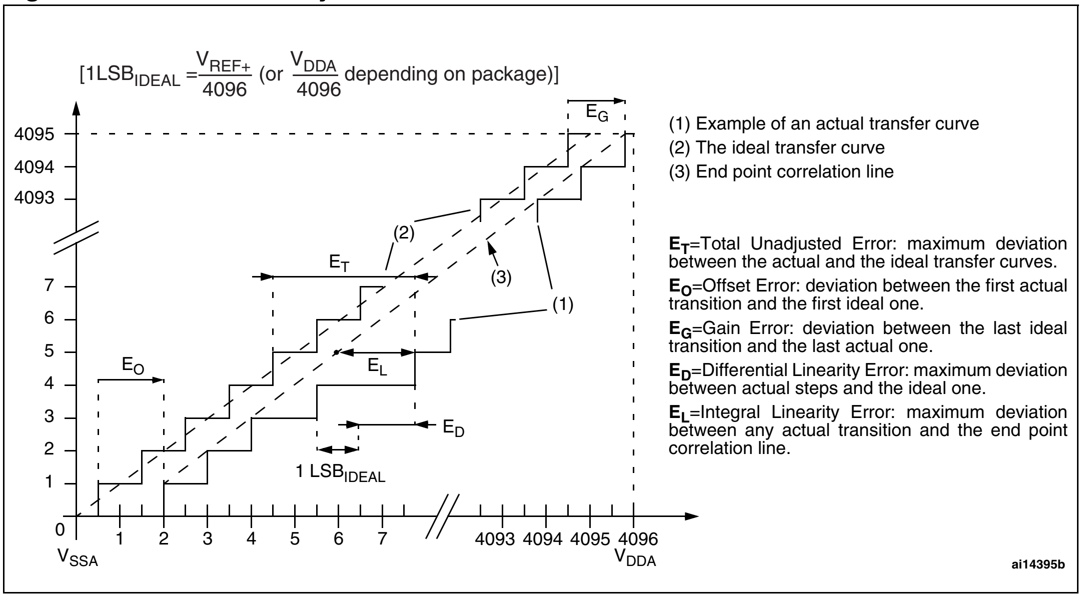
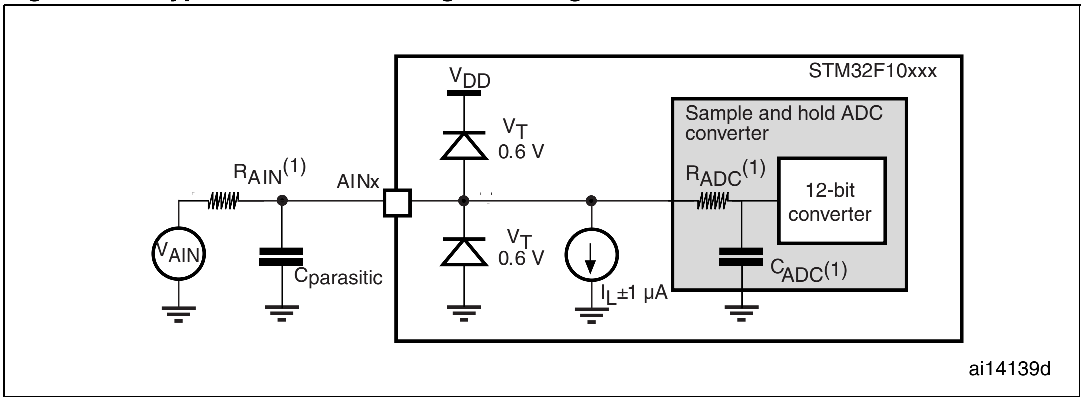


Figure 45. Typical connection diagram using the ADC

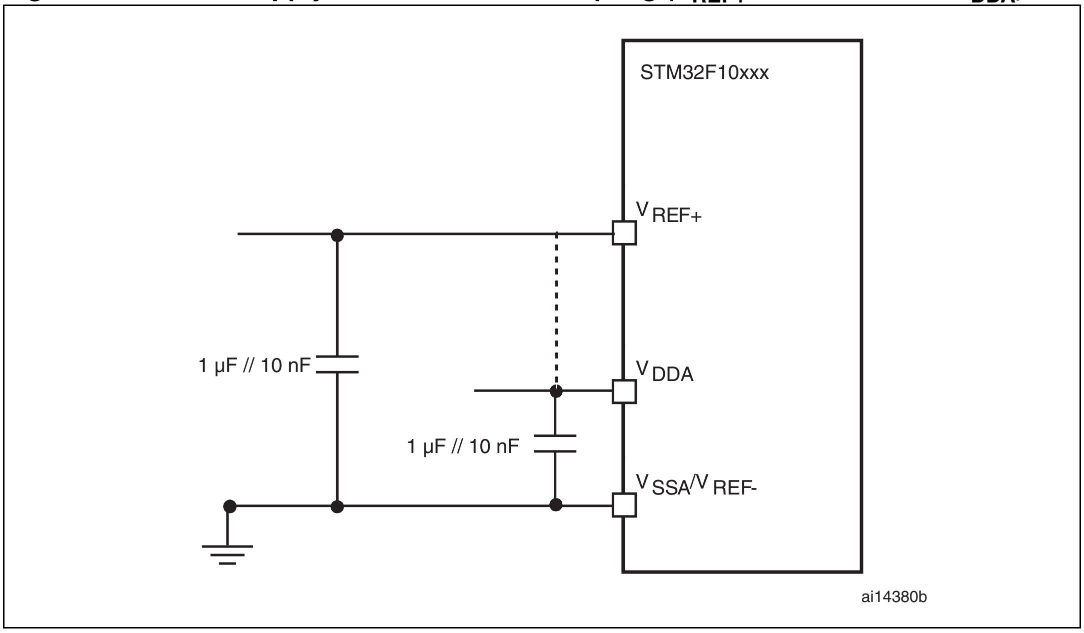


1. Refer to *Table 53* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

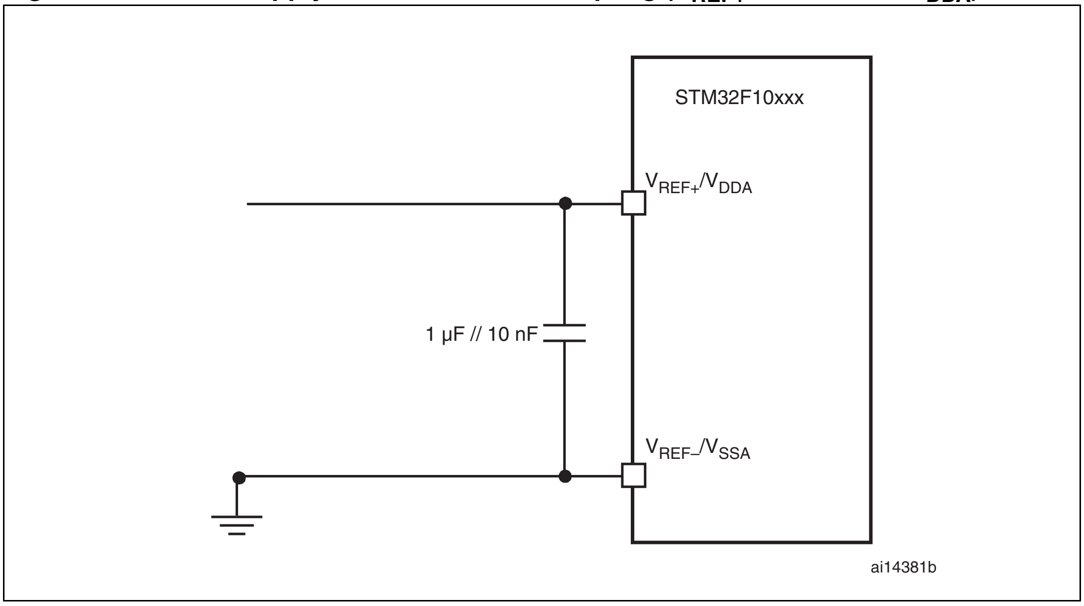
Power supply decoupling should be performed as shown in *Figure 46* or *Figure 47*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

Figure 46. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are available only on 100-pin packages.

Figure 47. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are available only on 100-pin packages.

5.3.18 DAC electrical specifications

Table 57. DAC characteristics

Symbol	Parameter	Min	Typ	Max(1)	Unit	Comments
V_{DD33A}	Analog supply voltage	2.4		3.6	V	
V_{DD18D}	Digital supply voltage	1.6	1.8	2	V	
V_{REF+}	Reference supply voltage	2.4		3.6	V	V_{REF+} must always be below V_{DD33A}
V_{SSA}	Ground	0		0	V	
R_L	Resistive load with buffer ON	5			kΩ	Minimum resistive load between DAC_OUT and V_{SSA}
C_L	Capacitive load			50	pF	Maximum capacitive load at DAC_OUT pin.
DAC_OUTmin	Lower DAC_OUT voltage with buffer ON	0.2			V	It gives the maximum output excursion of the DAC it corresponds to 12-bit input code (0E0)h to (F1C)h @ V_{REF+} = 3.6 V and (155)h and (EAB)h @ V_{REF+} = 2.4 V
DAC_OUTmax	Higher DAC_OUT voltage with buffer ON			V_{REF+} – 0.2 V	V	
I_{DD}	DAC DC current consumption in quiescent mode (Standby mode) (in V_{DD18D}+V_{DD33A}+ V_{REF+})		425	600	µA	With no load, middle code (800)H on the inputs
			500	700	µA	With no load, worst code (F1C)H @ V_{REF+} = 3.6 V in terms of DC consumption on the inputs
I_{DDQ}	DAC DC current consumption in Power Down mode (in V_{DD18D}+V_{DD33A}+V_{REF+})		5	350	nA	With no load.
	DAC DC current consumption in Power Down mode (in V_{DD33A}+V_{REF+})		5	200		
DNL	Differential non linearity (Difference between two consecutive code-1LSB)		±0.5		LSB	Given for the DAC in 10-bit configuration (B1=B0=0 always)
INL	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)		±1		LSB	Given for the DAC in 10-bit configuration (B1=B0=0 always)
Offset	Offset error (difference between measured value at Code (800)H and the ideal value = V_{REF+}/2		±10		mV	Given for the DAC in 10-bit configuration (B1=B0=0 always)
			±3		LSB	Given for the DAC in 10-bit @ V_{REF+} = 3.6 V

Table 57. DAC characteristics (continued)

Symbol	Parameter	Min	Typ	Max[1]	Unit	Comments
Gain error	Gain error		±0.5		%	Given for the DAC in 10-bit configuration (B1=B0=0 always)
Amplifier gain	Gain of the amplifier in open loop	80	85		dB	with a 5 kΩ load (worst case)
$t_{SETTLING}$	Settling time (full scale: for an 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB		3	4	µs	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ
Update rate	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)			1	MS/s	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ
t_{WAKEUP}	Wakeup time from off state (PDV18 from 1 to 0)		6.5	10	µs	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ input code between lowest and highest possible ones.
PSRR+	Power supply rejection ratio (to V_{DD33A}) (static DC measurement		–67	–40	dB	No R_{LOAD}, C_{LOAD} = 50 pF

1. Guaranteed by characterization, not tested in production.

5.3.19 Temperature sensor characteristics

Table 58. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L[1]	V_{SENSE} linearity with temperature		±1	±2	°C
Avg_Slope[1]	Average slope	4.0	4.3	4.6	mV/°C
V_{25}[1]	Voltage at 25°C	1.34	1.43	1.52	V
t_{START}[2]	Startup time	4		10	µs
T_{S_temp}[3][2]	ADC sampling time when reading the temperature			17.1	µs

1. Guaranteed by characterization, not tested in production.
2. Guaranteed by design, not tested in production.
3. Shortest sampling time can be determined in the application by multiple iterations.

6 Package characteristics

6.1 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 48. LQFP144, 20 x 20 mm, 144-pin thin quad flat package outline(1)

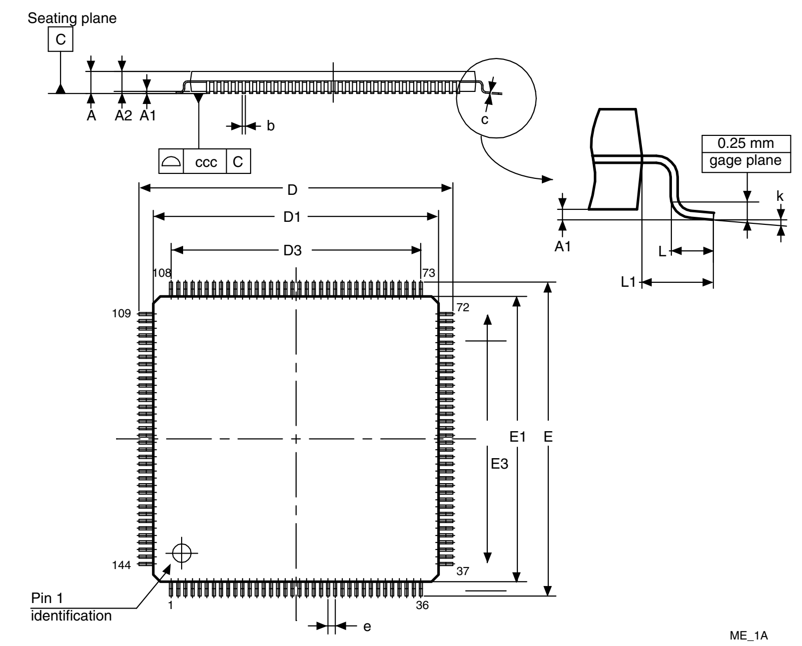
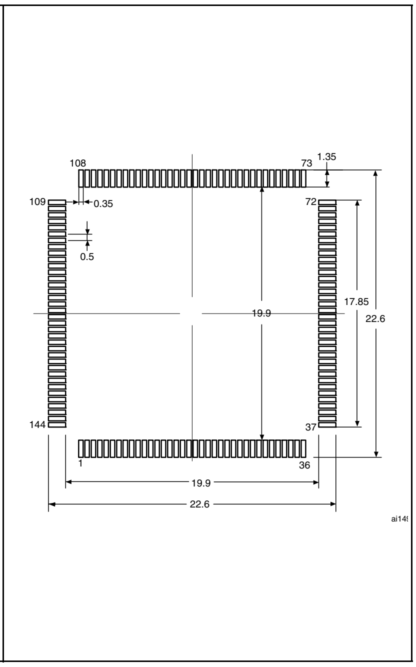


Figure 49. Recommended footprint(1)(2)



1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 59. LQFP144, 20 x 20 mm, 144-pin thin quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Typ	Min	Max	Typ	Min	Max
A			1.60			0.063
A1		0.05	0.15		0.002	0.0059
A2	1.40	1.35	1.45	0.0551	0.0531	0.0571
b	0.22	0.17	0.27	0.0087	0.0067	0.0106
c		0.09	0.20		0.0035	0.0079
D	22.00	21.80	22.20	0.8661	0.8583	0.874
D1	20.00	19.80	20.20	0.7874	0.7795	0.7953
D3	17.50			0.689		
E	22.00	21.80	22.20	0.8661	0.8583	0.874
E1	20.00	19.80	20.20	0.7874	0.7795	0.7953
E3	17.50			0.689		
e	0.50			0.0197		
L	0.60	0.45	0.75	0.0236	0.0177	0.0295
L1	1.00			0.0394		
k	3.5°	0°	7°	3.5°	0°	7°
ccc	0.08			0.0031		

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 50. LQFP100, 100-pin low-profile quad flat package outline(1)

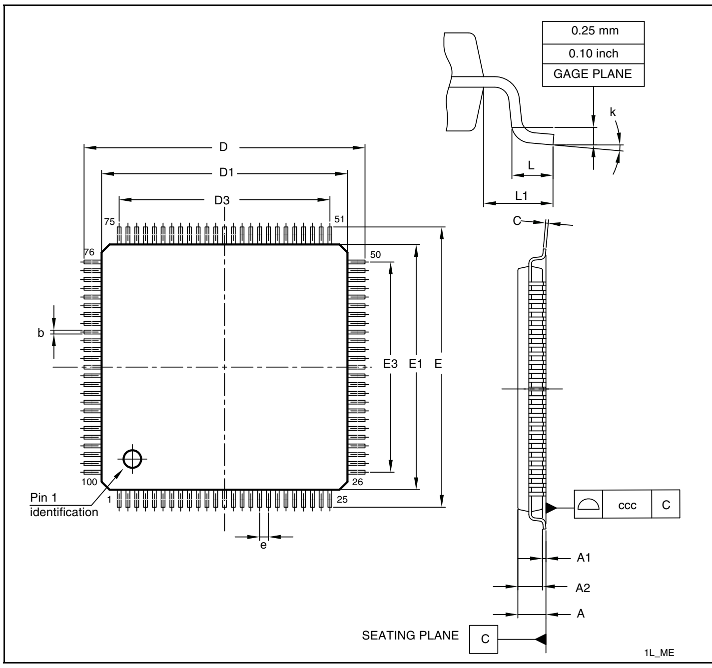
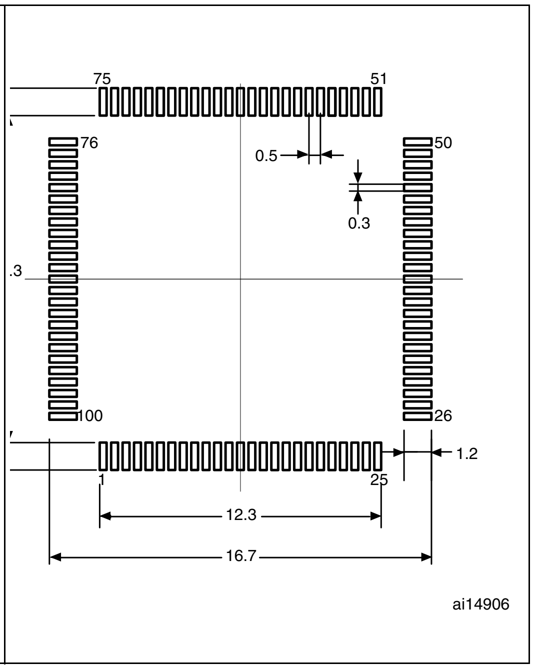


Figure 51. Recommended footprint(1)(2)



1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 60. LQPF100 – 100-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Typ	Min	Max	Typ	Min	Max
A			1.60			0.063
A1		0.05	0.15		0.002	0.0059
A2	1.40	1.35	1.45	0.0551	0.0531	0.0571
b	0.22	0.17	0.27	0.0087	0.0067	0.0106
c		0.09	0.20		0.0035	0.0079
D	16.00	15.80	16.20	0.6299	0.622	0.6378
D1	14.00	13.80	14.20	0.5512	0.5433	0.5591
D3	12.00			0.4724		
E	16.00	15.80	16.20	0.6299	0.622	0.6378
E1	14.00	13.80	14.20	0.5512	0.5433	0.5591
E3	12.00			0.4724		
e	0.50			0.0197		
L	0.60	0.45	0.75	0.0236	0.0177	0.0295
L1	1.00			0.0394		
k	3.5°	0°	7°	3.5°	0°	7°
ccc	0.08			0.0031		

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 52. LQFP64 – 64 pin low-profile quad flat package outline(1)

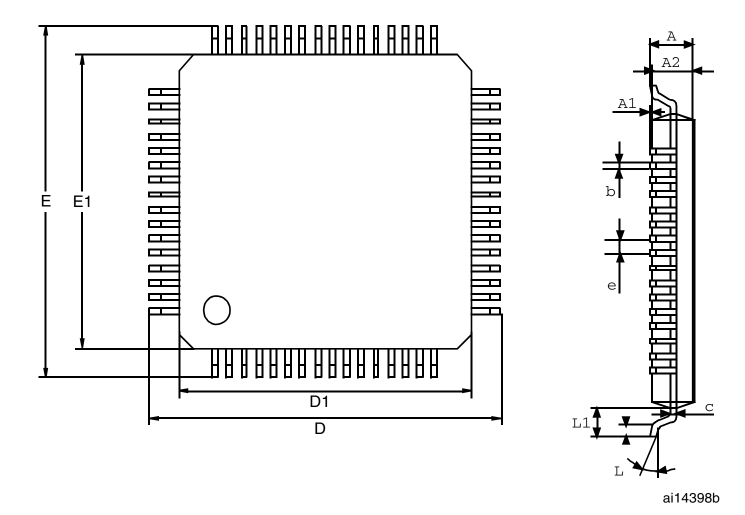
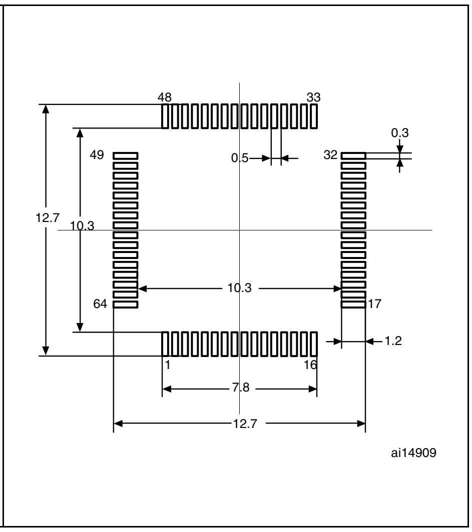


Figure 53. Recommended footprint(1)(2)



1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 61. LQFP64 – 64 pin low-profile quad flat package mechanical data

Dim.	mm			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.0630
A1	0.05		0.15	0.0020		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
c	0.09		0.20	0.0035		0.0079
D		12.00			0.4724	
D1		10.00			0.3937	
E		12.00			0.4724	
E1		10.00			0.3937	
e		0.50			0.0197	
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0394	
N	Number of pins					
	64					

1. Values in inches are converted from mm and rounded to 4 decimal digits.

6.2 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 10: General operating conditions on page 37*.

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \max = T_A \max + (P_D \max \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$P_{I/O} \max = \Sigma (V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH})$,

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 62. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP144 - 20 x 20 mm / 0.5 mm pitch	30	°C/W
	Thermal resistance junction-ambient LQFP100 - 14 x 14 mm / 0.5 mm pitch	46	
	Thermal resistance junction-ambient LQFP64 - 10 x 10 mm / 0.5 mm pitch	45	

6.2.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

6.2.2 Evaluating the maximum junction temperature for an application

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Table 63: Ordering information scheme*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature. Here, only temperature range 6 is available (–40 to 85 °C).

The following example shows how to calculate the temperature range needed for a given application, making it possible to check whether the required temperature range is compatible with the STM32F10xxx junction temperature range.

Example: High-performance application

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 82 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V and maximum 8 I/Os used at the same time in output mode at low level with I_{OL} = 20 mA, V_{OL}= 1.3 V

P_{INTmax} = 50 mA × 3.5 V= 175 mW

P_{IOmax} = 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW

This gives: P_{INTmax} = 175 mW and P_{IOmax} = 272 mW

P_{Dmax} = 175 + 272 = 447 mW

Thus: P_{Dmax} = 447 mW

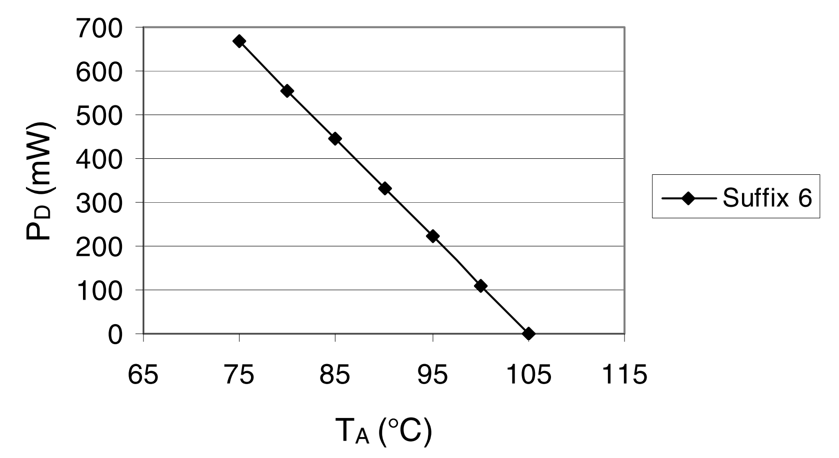
Using the values obtained in *Table 63* T_{Jmax} is calculated as follows:

– For LQFP64, 45 °C/W

T_{Jmax} = 82 °C + (45 °C/W × 447 mW) = 82 °C + 20.1 °C = 102.1 °C

This is within the junction temperature range of the STM32F10xxx (–40 < T_J < 105 °C).

Figure 54. LQFP64 P_D max vs. T_A



7 Part numbering

Table 63. Ordering information scheme

Example: STM32 F 101 R C T 6 xxx

Device family
STM32 = ARM-based 32-bit microcontroller

Product type
F = general-purpose

Device subfamily
101 = access line

Pin count
R = 64 pins
V = 100 pins
Z = 144 pins

Flash memory size
C = 256 Kbytes of Flash memory
D = 384 Kbytes of Flash memory
E = 512 Kbytes of Flash memory

Package
T = LQFP

Temperature range
6 = Industrial temperature range, –40 to 85 °C.

Options
xxx = programmed parts
TR = tape and real

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

8 Revision history

Table 64. Document revision history

Date	Revision	Changes
07-Apr-2008	1	Initial release.
22-May-2008	2	Document status promoted from Target Specification to Preliminary Data. *Section 1: Introduction* and *Section 2.2: Full compatibility throughout the family* modified. Small text changes. *Note 1* added in *Table 2: STM32F101xC, STM32F101xD and STM32F101xE features and peripheral counts on page 11*. LQPF100/BGA100 column added to *Table 6: FSMC pin definition on page 30*. Values added to *Maximum current consumption on page 39* (see *Table 14*, *Table 15*, *Table 16* and *Table 17*). Values added to *Typical current consumption on page 44* (see *Table 18*, *Table 19* and *Table 20* and see *Figure 11*, *Figure 12*, *Figure 13*, *Figure 14* and *Figure 15*). *Table 19: Typical current consumption in Standby mode* removed. *Figure 49: Recommended footprint(1) on page 91* corrected. *Equation 1* corrected. *Section 6.2.2: Evaluating the maximum junction temperature for an application on page 95* added.
21-Jul-2008	3	Document status promoted from Preliminary Data to full datasheet. *FSMC (flexible static memory controller) on page 13* modified. *Power supply supervisor on page 15* modified and V_{DDA} added to *Table 10: General operating conditions on page 37*. Table notes revised in *Section 5: Electrical characteristics*. Capacitance modified in *Figure 9: Power supply scheme on page 34*. *Table 51: SCL frequency (f_{PCLK1}= 36 MHz, V_{DD} = 3.3 V)* updated. *Table 52: SPI characteristics* modified, $t_{h(NSS)}$ modified in *Figure 41: SPI timing diagram - slave mode and CPHA=0 on page 82*. Minimum SDA and SCL fall time value for Fast mode removed from *Table 50: I^2C characteristics on page 79*, note 1 modified. I_{DD_VBAT} values added to *Table 17: Typical and maximum current consumptions in Stop and Standby modes on page 42*. *Table 30: Flash memory endurance and data retention on page 53* updated. f_{HCLK} corrected in *Table 41: EMS characteristics*. $t_{su(NSS)}$ modified in *Table 52: SPI characteristics on page 81*. EO corrected in *Table 56: ADC accuracy on page 85*. f_{PCLK2} corrected in *Table 55: ADC accuracy - limited test conditions* and *Table 56: ADC accuracy*. *Figure 45: Typical connection diagram using the ADC on page 86* and note below corrected. Typical T_{S_temp} value removed from *Table 58: TS characteristics on page 89*. *Section 6.1: Package mechanical data on page 90* updated. Small text changes.

Table 64. Document revision history

Date	Revision	Changes
12-Dec-2008	4	*General-purpose timers (TIMx) on page 17* updated. *Table 3: STM32F101xx family* updated to show the low-density family. *Table 4: Timer feature comparison* added *Figure 1: STM32F101xC, STM32F101xD and STM32F101xE access line block diagram* updated. *Note 8* added, main function after reset and *Note 4* updated in *Table 5: High-density STM32F101xx pin definitions*. *Note 2* modified below *Table 7: Voltage characteristics on page 35*, $\|\Delta V_{DDx}\|$ min and $\|\Delta V_{DDx}\|$ min removed. Measurement conditions specified in *Section 5.3.5: Supply current characteristics on page 39*. *General input/output characteristics on page 74* modified. Max values at T_A = 85 °C updated in *Table 17: Typical and maximum current consumptions in Stop and Standby modes on page 42*. *Section 5.3.10: FSMC characteristics on page 53* revised. Values added to *Table 42: EMI characteristics on page 73*. I_{VREF} added to *Table 53: ADC characteristics on page 84*. *Table 62: Package thermal characteristics on page 94* updated. Small text changes.

Table 64. Document revision history

Date	Revision	Changes
30-Mar-2009	5	I/O information clarified *on page 1*. Number of ADC peripherals corrected in *Table 2: STM32F101xC, STM32F101xD and STM32F101xE features and peripheral counts*. In *Table 5: High-density STM32F101xx pin definitions*: – I/O level of pins PF11, PF12, PF13, PF14, PF15, G0, G1 and G15 updated – PB4, PB13, PB14, PB15, PB3/TRACESWO moved from Default column to Remap column. PG14 pin description modified in *Table 6: FSMC pin definition*. *Figure 6: Memory map on page 32* modified. Note modified in *Table 14: Maximum current consumption in Run mode, code with data processing running from Flash* and *Table 16: Maximum current consumption in Sleep mode, code running from Flash or RAM*. *Figure 13*, *Figure 14* and *Figure 15* show typical curves (titles changed). *Table 21: High-speed external user clock characteristics* and *Table 22: Low-speed user external clock characteristics* modified. ACC_{HSI} max values modified in *Table 25: HSI oscillator characteristics* FSMC configuration modified for *Asynchronous waveforms and timings*. Notes modified below *Figure 20: Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms* and *Figure 21: Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms*. $t_{w(NADV)}$ values modified in *Table 31: Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings* and *Table 34: Asynchronous multiplexed NOR/PSRAM write timings*. $t_{h(Data\_NWE)}$ modified in *Table 32: Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings*. In *Table 36: Synchronous multiplexed PSRAM write timings* and *Table 38: Synchronous non-multiplexed PSRAM write timings*: – $t_{v(Data-CLK)}$ renamed as $t_{d(CLKL-Data)}$ – $t_{d(CLKL-Data)}$ min value removed and max value added – $t_{h(CLKL-DV)}$ / $t_{h(CLKL-ADV)}$ removed *Figure 24: Synchronous multiplexed NOR/PSRAM read timings*, *Figure 25: Synchronous multiplexed PSRAM write timings* and *Figure 27: Synchronous non-multiplexed PSRAM write timings* modified. Small text changes.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com