STM32TS60

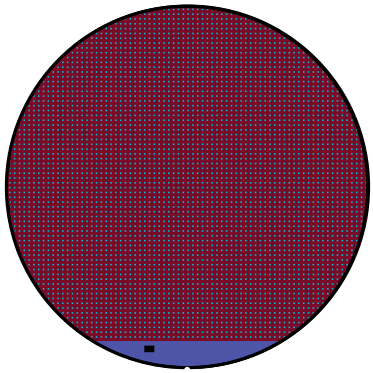
ARM®-based 32-bit MCU with resistive multitouch engine, 32 KB Flash, USB, 5 timers, 2 ADCs, and 6 communication interfaces

Data brief

Features

- Core: ARM 32-bit Cortex™-M3 CPU
  - 72 MHz maximum frequency, 1.25 DMIPS/MHz (Dhrystone 2.1) performance at 0 wait state memory access
  - Single-cycle multiplication and hardware division
- Memories
  - 32 Kbytes of Flash memory
  - 10 Kbytes of SRAM
- Clock, reset and supply management
  - 2.4 to 3.6 V application supply and I/Os
  - POR, PDR, and programmable voltage detector (PVD)
  - 4 to 16 MHz crystal oscillator
  - Internal 8-MHz factory-trimmed RC
  - Internal 40-kHz RC
  - PLL for CPU clock
- Low power
  - Sleep, Stop and Standby modes
- 2 x 12-bit, 1 µs A/D converters (with up to 64 channels)
  - Conversion range: 0 to 3.6 V
  - Dual-sample and hold capability
  - Temperature sensor
- DMA
  - 8-channel DMA controller
  - Peripherals supported: timers, ADC, SPIs, I^2Cs, USART, PMSE and PMAD.
- Up to 138 fast I/O ports
- PMatrix™ scanning engine (PMSE) and PMatrix™ area detection (PMAD)
  - Up to 81 columns and 64 rows
- Debug mode
  - Serial wire debug (SWD) & JTAG interfaces

UFBGA144
7 × 7 mm



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Unsawn wafer

- 5 timers
  - 2 x 16-bit timers, each with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
  - 2 x watchdog timers (independent and window)
  - SysTick timer: a 24-bit downcounter
- 6 communication interfaces
  - 2 x I^2C interfaces (SMBus/PMBus)
  - 1 x USART (ISO 7816 interface, LIN, IrDA capability, modem control)
  - 2 x SPIs (18 Mbit/s and 9 Mbit/s)
  - USB 2.0 full-speed interface
- CRC calculation unit, 96-bit unique ID
- Packages are ECOPACK®

Contents

List of tables

List of figures

1 Introduction

This data brief provides the ordering information and mechanical device characteristics of the STM32TS60 microcontrollers.

The STM32TS60 is specifically designed for multitouch touch screen applications based on Stantum's patented digital resistive multitouch technology. It features two dedicated touch sensing peripherals (PMatrix™ scanning engine and PMatrix™ area detection) offering a highly integrated solution and improved performances compared to existing market solutions. The STM32TS60 supports a touch panel with a matrix of up to 81 columns and 64 rows.

For further information on any aspect of this device or to get access to the corresponding datasheet, reference manual, die specification, and programming manual, please contact your nearest ST Sales Office.

For information on the Cortex-M3 core please refer to the Cortex™-M3 Technical Reference Manual, available from the www.arm.com website at the following address: http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ddi0337e/.

Note: PMatrix™ is a trademark of Stantum SAS.

2 Description

The STM32TS60 device incorporates the high-performance ARM, Cortex-M3, 32-bit RISC core, operating at a 72-MHz frequency, with high-speed embedded memories (32 Kbytes Flash memory and 10 Kbytes SRAM), and an extensive range of enhanced I/Os and peripherals connected to two APB buses. It offers two 12-bit ADCs, two general purpose 16-bit timers, as well as standard and advanced communication interfaces: two I^2Cs, two SPIs, one USART, and a USB.

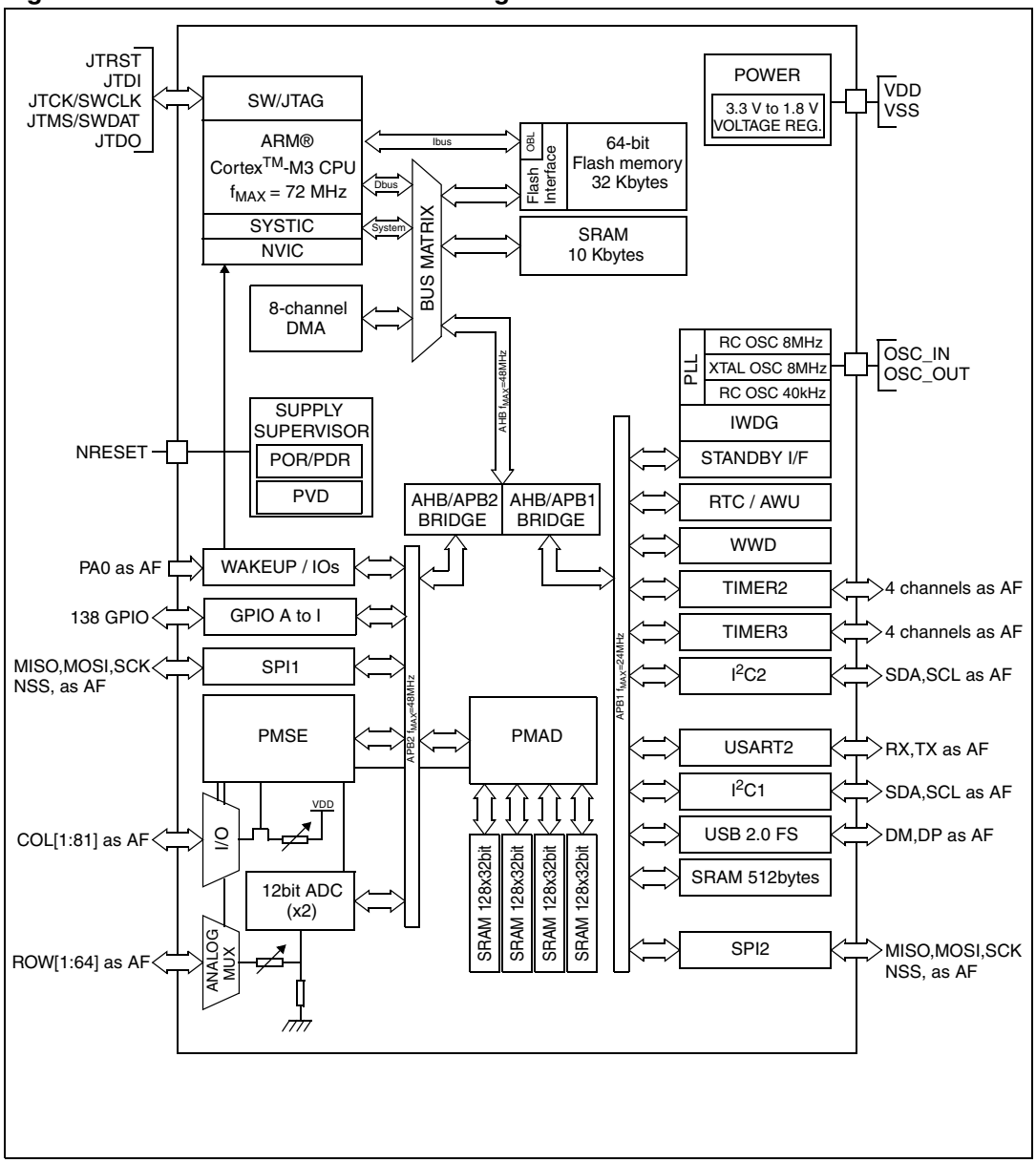
The device operates from a 2.4 to 3.6 V power supply. It is available in the –40 to +85 °C temperature range. A comprehensive set of power-saving modes allow the design of low-power applications.The STM32TS60 device is available in a UFBGA144 7 mm x 7 mm package and die form (unsawn wafer).

2.1 Device overview

Table 1. STM32TS60 device features and peripheral counts

Peripheral		Device
Flash (Kbytes)		32
SRAM (Kbytes)		10
General-purpose timers		2
Communication	SPI	2
	I^2C	2
	USART	1
	USB	1
GPIOs		138
12-bit synchronized ADC (number of channels)		2 (64)
CPU frequency		72 MHz
Operating voltage		2.4 to 3.6 V
Operating temperatures	Ambient	–40 to 85 °C (see *Table 5*)
	Junction	–40 to 125 °C (see *Table 5*)
Packages		UFBGA144
		Unsawn wafer

Figure 1. STM32TS60 device block diagram



2.2 Peripheral overview

2.2.1 ARM Cortex-M3 core with embedded Flash and SRAM

The ARM Cortex-M3 processor is the latest generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM Cortex-M3 32-bit RISC processor features exceptional code efficiency, delivering the high performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The STM32TS60 device, having an embedded ARM core, is therefore compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the device family.

2.2.2 Embedded Flash memory

32 Kbytes of embedded Flash is available for storing programs and data.

2.2.3 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

2.2.4 Embedded SRAM

The 10 Kbytes of embedded SRAM can be accessed (read/write) at CPU clock speed with 0 wait states.

2.2.5 Nested vectored interrupt controller (NVIC)

The STM32TS60 embeds a nested vectored interrupt controller which can handle up to 43 maskable interrupt channels (not including the 16 interrupt lines of Cortex-M3) and 16 priority levels. Features include:

- Closely coupled NVIC which gives low-latency interrupt processing
- Interrupt entry vector table address which is passed directly to the core
- Closely coupled NVIC core interface
- Early processing of interrupts is allowed
- Processing of “late arriving” higher priority interrupts
- Support for tail-chaining
- Processor state is automatically saved
- Interrupt entry is restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

2.2.6 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 19 edge detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both edges) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the internal APB2 clock period. Up to 138 GPIOs can be connected to the 9 external interrupt lines.

2.2.7 Clocks and startup

System clock selection is performed at startup, however the internal RC 8-MHz oscillator is selected as the default CPU clock on reset. An external 4-16 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example, on failure of an indirectly used external crystal, resonator or oscillator).

Several prescalers allow the configuration of the AHB frequency, the high-speed APB (APB2), and the low-speed APB (APB1) domains. The maximum frequency of the AHB and the high-speed APB domains is 72 MHz. The maximum allowed frequency of the low-speed APB domain is 36 MHz.

2.2.8 Boot modes

At startup, boot pins are used to select one of three boot options:

- The boot from the user Flash
- The boot from the system memory
- The boot from the embedded SRAM

The boot loader is located in the system memory. It is used to reprogram the Flash memory by using USART2. For further details please refer to AN2606.

2.2.9 Power supply supervisor

The device has an integrated power-on reset (POR)/power-down reset (PDR) circuitry. It is always active, and ensures correct operation starting from/down to 2 V. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD} drops below the V_{PVD} threshold and/or when V_{DD} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

2.2.10 Voltage regulator

The regulator has three operating modes: Main (MR), Low power (LPR) and Power-down.

- MR is used in the nominal regulation mode (Run)
- LPR is used in Stop mode
- Power-down is used in Standby mode: the regulator output is in high impedance where the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost).

This regulator is always enabled after reset. It is disabled in Standby mode, providing high impedance output.

2.2.11 Low power modes

The STM32TS60 device supports three Low power modes to achieve the best compromise between Low power consumption, short startup time, and available wakeup sources:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop** mode

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and the registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put in either Normal or in Low power mode. The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 9 external lines, the PVD output, the RTC alarm, or the USB wakeup.

- **Standby** mode

  Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, the SRAM and register contents are lost except for registers in the backup domain and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

2.2.12 PMatrix scanning engine (PMSE)

The PMSE handles the acquisition of the touch panel with a reduced CPU load. It automatically controls the column and row I/Os and generates the trigger signals for the ADCs and for the PMAD. Up to 81 columns and 64 rows are supported by the PMSE. Its powerful implementation allows high frequency rates (up to 250 kHz) to be targeted with a reduced power consumption. Several power consumption schemes are available to improve system operation:

- Normal scanning mode
- Fast scanning mode
- Standby mode

The PMSE can be served by the DMA controller.

2.2.13 PMatrix area detection (PMAD)

The PMAD works in combination with the PMSE. It reduces the CPU load by processing the information provided by the PMSE. It returns information on the touched areas.

The PMAD can be served by the DMA controller.

2.2.14 Direct memory access (DMA)

The flexible 8-channel general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory, and memory-to-peripheral transfers. The DMA controller supports circular buffer management avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for a software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPIx, I^2Cx, USART2, general-purpose timers TIMx, ADCx, PMSE, and PMAD.

2.2.15 Real-time clock (RTC) and backup registers

The real-time clock provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provide an alarm interrupt and a periodic interrupt. It is clocked by the internal low-power RC oscillator having a typical frequency of 40 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural crystal deviation. A 20-bit prescaler is used for the time base clock and is, by default, configured to generate a time base of 1 second from a clock at 32.768 kHz. The backup registers include ten 16-bit registers which are used to store 20 bytes of user application data.

2.2.16 Timers and watchdogs

The STM32TS60 device includes two general-purpose timers, two watchdog timers and a SysTick timer.

Table 2 compares the features of the advanced-control and general-purpose timers.

Table 2. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TIM2 and TIM3	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No

General-purpose timers (TIMx)

There are up to two synchronizable general-purpose timers embedded in the STM32TS60 device. These timers are based on a 16-bit auto-reload up/down counter and a 16-bit prescaler. They feature four independent channels each for input capture/output compare, PWM or one-pulse mode output. Their counters can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs. They all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from one to three hall-effect sensors.

Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and an 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and, as it operates independently of the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes. The counter can be frozen in debug mode.

Window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

SysTick timer

This timer is dedicated for OS, but could also be used as a standard downcounter. It features:

- A 24-bit downcounter
- Auto-reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

2.2.17 I²C bus

I²C bus interfaces can operate in multimaster and slave modes. They can support standard and fast modes.

They support dual slave addressing (7-bit only) and both 7/10-bit addressing in master mode. A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SM Bus 2.0/PM Bus.

2.2.18 Universal synchronous/asynchronous receiver transmitter (USART)

The USART interface is able to communicate at up to 2.25 Mbit/s. It provides hardware management of the CTS and RTS signals and IrDA SIR ENDEC support. It is also ISO 7816 compliant and has LIN master/slave capability.

The USART interface can be served by the DMA controller.

2.2.19 Serial peripheral interface (SPI)

The SPI interfaces are able to communicate up to 18 Mbits/s (SPI1) and 9 Mbits/s (SPI2) in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives eight master mode frequencies and the frame is configurable to 8 or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

Both SPI interfaces can be served by the DMA controller.

2.2.20 Universal serial bus (USB)

The STM32TS60 device embeds a USB device peripheral compatible with the USB full-speed 12 Mbs. The USB interface implements a full-speed (12 Mbit/s) function interface. It has a software-configurable endpoint setting and suspend/resume support. The dedicated 48-MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator).

2.2.21 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-down), or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current-capable except for analog inputs.

The I/Os alternate function configuration can be locked, if needed, following a specific sequence to avoid spurious writing to the I/Os registers. I/O toggling speed is up to 18 MHz.

2.2.22 Analog-to-digital converter (ADC)

Two 12-bit analog-to-digital converters are embedded into STM32TS60 device and each ADC shares up to 64 external channels, performing conversions in single-shot mode only (scan mode is not supported by the STM32TS60).

The ADC can be served by the DMA controller.

2.2.23 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 2.4 V < V_{DD} < 3.6 V. The temperature sensor is internally connected to the ADC1_IN16 input channel which is used to convert the sensor output voltage into a digital value.

2.2.24 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded. It is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3 Ballout and pin description

Figure 2. STM32TS60 device UFBGA144 ballout

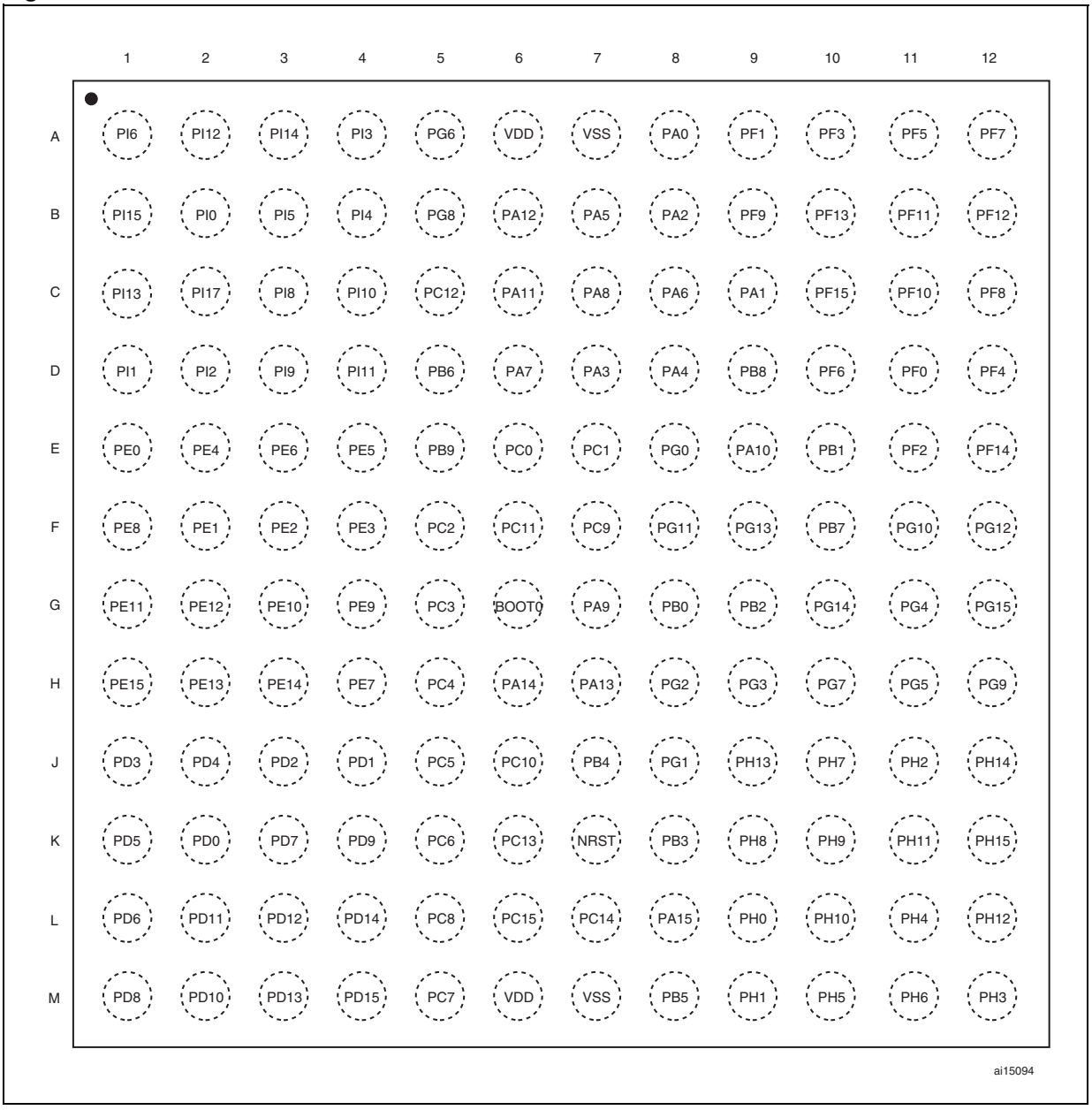


Table 3. STM32TS60 pin definitions

Pin no.	Pin type(1)(2)	Pin level(3)	PIn name	Pin function
A1	I/O		PI6/COL	Touch panel column
A2	I/O		PI12/COL	Touch panel column
A3	I/O		PI14/COL	Touch panel column
A4	I/O		PI3/COL	Touch panel column
A5	I/O		PG6/COL	Touch panel column
A6	S		VDD_1	Supply voltage pin
A7	S		VSS_1	Ground pin 1
A8	I/O		PA0/WAKE-UP/SPI1_NSS	Device wake-up capability SPI1 slave select (active low)
A9	I/O		PF1/COL/ROW	Touch panel column Touch panel row
A10	I/O		PF3/COL/ROW	Touch panel column Touch panel row
A11	I/O		PF5/COL/ROW	Touch panel column Touch panel row
A12	I/O		PF7/COL/ROW	Touch panel column Touch panel row
B1	I/O		PI15/COL	Touch panel column
B2	I/O		PI0/COL	Touch panel column
B3	I/O		PI5/COL	Touch panel column
B4	I/O		PI4/COL	Touch panel column
B5	I/O		PG8/COL	Touch panel column
B6	I/O		PA12/OSC_OUT/COL	Crystal/resonator oscillator output Touch panel column
B7	I/O	FT	PA5/I2C2_SCL/USART2_CTS/SPI2_SCK(remap)/TIM3_CH1/TIM3_ETR/TIM2_CH1(remap)	I^2C2 clock input/output USART2 clear to send SPI2 clock input/output (remap) TIM3 CH1 TIM3 external trig TIM2 CH1 (remap)
B8	I/O		PA2/USBDM/I2C1_SMBAI	USB data- I^2C1 SMBAI
B9	I/O		PF9/COL/ROW	Touch panel column Touch panel row
B10	I/O		PF13/COL/ROW	Touch panel column Touch panel row
B11	I/O		PF11/COL/ROW	Touch panel column Touch panel row
B12	I/O		PF12/COL/ROW	Touch panel column Touch panel row

Table 3. STM32TS60 pin definitions (continued)

Pin no.	Pin type(1)(2)	Pin level(3)	PIn name	Pin function
C1	I/O		PI13/COL	Touch panel column
C2	I/O		PI7/COL	Touch panel column
C3	I/O		PI8/COL	Touch panel column
C4	I/O		PI10/COL	Touch panel column
C5	I/O		PC12/ROW	Touch panel row
C6	I/O		PA11/OSC_IN/COL	Crystal / resonator oscillator input Touch panel column
C7	I/O	FT	PA8	
C8	I/O		PA6/I2C2_SDA/SPI2_MISO(remap)/USART2_RTS/TIM3_CH2/TIM2_CH2(remap)/MCO	I^2C2 data SPI2 master in/slave out (remap) USART2 request to send TIM3 CH2 TIM2_CH2 remap MCO
C9	I/O		PA1/USBDP/I2C2_SMBAI	USB data+ I^2C2 SMBAI
C10	I/O		PF15/COL/ROW	Touch panel column Touch panel row
C11	I/O		PF10/COL/ROW	Touch panel column Touch panel row
C12	I/O		PF8/COL/ROW	Touch panel column Touch panel row
D1	I/O		PI1/COL	Touch panel column
D2	I/O		PI2/COL	Touch panel column
D3	I/O		PI9/COL	Touch panel column
D4	I/O		PI11/COL	Touch panel column
D5	I/O		PB6/TIM2_CH1/TRACED0/COL	TIM2 CH1 Trace data 0 Touch panel column
D6	I/O		PA7/SPI1_MOSI/USART2_RX	SPI1 master out/slave in USART2 data receive
D7	I/O	FT	PA3/SPI1_SCK/I2C1_SCL/USART2_CK	SPI1 clock input/output I^2C1 clock input/output USART2 clock input/output
D8	I/O	FT	PA4/SPI1_MISO/I2C1_SDA/USART2_TX	SPI1 master in/slave out I^2C1 data USART2 data transmit
D9	I/O		PB8/TIM2_CH3/TRACED2/COL	TIM2 CH3 Trace data 2 Touch panel column

Table 3. STM32TS60 pin definitions (continued)

Pin no.	Pin type(1)(2)	Pin level(3)	PIn name	Pin function
D10	I/O		PF6/COL/ROW	Touch panel column Touch panel row
D11	I/O		PF0/COL/ROW	Touch panel column Touch panel row
D12	I/O		PF4/COL/ROW	Touch panel column Touch panel row
E1	I/O		PE0/ROW	Touch panel row
E2	I/O		PE4/ROW	Touch panel row
E3	I/O		PE6/ROW	Touch panel row
E4	I/O		PE5/ROW	Touch panel row
E5	I/O		PB9/TIM2_CH4/TRACED3/COL	TIM2 CH4 Trace data 3 Touch panel column
E6	I/O		PC0/ROW	Touch panel row
E7	I/O		PC1/ROW	Touch panel row
E8	I/O		PG0/COL	Touch panel column
E9	I/O		PA10/SPI2_MOSI(remap)/TIM3_CH3/TIM2_CH3 (remap)/COL	SPI2 master out/slave in (remap) TIM3 CH3 TIM2 CH3 (remap) Touch panel column
E10	I/O		PB1/SPI2_MISO/COL	SPI2 master in/slave out Touch panel column
E11	I/O		PF2/COL/ROW	Touch panel column Touch panel row
E12	I/O		PF14/COL/ROW	Touch panel column Touch panel row
F1	I/O		PE8/ROW	Touch panel row
F2	I/O		PE1/ROW	Touch panel row
F3	I/O		PE2/ROW	Touch panel row
F4	I/O		PE3/ROW	Touch panel row
F5	I/O		PC2/ROW	Touch panel row
F6	I/O		PC11/ROW	Touch panel row
F7	I/O		PC9/ROW	Touch panel row
F8	I/O		PG11/COL	Touch panel column
F9	I/O		PG13/COL	Touch panel column
F10	I/O		PB7/TIM2_CH2/TRACED1/COL	TIM2 CH2 Trace data 1 Touch panel column
F11	I/O		PG10/COL	Touch panel column

Table 3. STM32TS60 pin definitions (continued)

Pin no.	Pin type(1)(2)	Pin level(3)	PIn name	Pin function
F12	I/O		PG12/COL	Touch panel column
G1	I/O		PE11/ROW	Touch panel row
G2	I/O		PE12/ROW	Touch panel row
G3	I/O		PE10/ROW	Touch panel row
G4	I/O		PE9/ROW	Touch panel row
G5	I/O		PC3/ROW	Touch panel row
G6	I		BOOT0	
G7	I/O		PA9/BOOT1/COL	BOOT1 Touch panel column
G8	I/O		PB0/SPI2_SCK/COL	SPI2 clock output/input Touch panel column
G9	I/O		PB2/SPI2_MOSI/COL	SPI2 master out/slave in Touch panel column
G10	I/O		PG14/COL	Touch panel column
G11	I/O		PG4/COL	Touch panel column
G12	I/O		PG15/COL	Touch panel column
H1	I/O		PE15/ROW	Touch panel row
H2	I/O		PE13/ROW	Touch panel row
H3	I/O		PE14/ROW	Touch panel row
H4	I/O		PE7/ROW	Touch panel row
H5	I/O		PC4/ROW	Touch panel row
H6	I/O		PA14/JTCK/SWCLK/COL	JTAG clock Serial wire clock Touch panel column
H7	I/O		PA13/JTMS/SWDIO/COL	JTAG mode selection Serial wire data input/output Touch panel column
H8	I/O		PG2/COL	Touch panel column
H9	I/O		PG3/COL	Touch panel column
H10	I/O		PG7/COL	Touch panel column
H11	I/O		PG5/COL	Touch panel column
H12	I/O		PG9/COL	Touch panel column
J1	I/O		PD3/ROW	Touch panel row
J2	I/O		PD4/ROW	Touch panel row
J3	I/O		PD2/ROW	Touch panel row
J4	I/O		PD1/ROW	Touch panel row
J5	I/O		PC5/ROW	Touch panel row

Table 3. STM32TS60 pin definitions (continued)

Pin no.	Pin type(1)(2)	Pin level(3)	PIn name	Pin function
J6	I/O		PC10/ROW	Touch panel row
J7	I/O		PB4/COL/JTRST	Touch panel column JTAG reset
J8	I/O		PG1/COL	Touch panel column
J9	I/O		PH13/COL	Touch panel column
J10	I/O		PH7/COL	Touch panel column
J11	I/O		PH2/COL	Touch panel column
J12	I/O		PH14/COL	Touch panel column
K1	I/O		PD5/ROW	Touch panel row
K2	I/O		PD0/ROW	Touch panel row
K3	I/O		PD7/ROW	Touch panel row
K4	I/O		PD9/ROW	Touch panel row
K5	I/O		PC6/ROW	Touch panel row
K6	I/O		PC13/ROW	Touch panel row
K7	I/O		NRST	Reset (active low)
K8	I/O		PB3/SPI2_NSS/COL/JTDO/TRACESWO	SPI2 slave select Touch panel column JTAG data output Trace output
K9	I/O		PH8/COL	Touch panel column
K10	I/O		PH9/COL	Touch panel column
K11	I/O		PH11/COL	Touch panel column
K12	I/O		PH15/COL	Touch panel column
L1	I/O		PD6/ROW	Touch panel row
L2	I/O		PD11/ROW	Touch panel row
L3	I/O		PD12/ROW	Touch panel row
L4	I/O		PD14/ROW	Touch panel row
L5	I/O		PC8/ROW	Touch panel row
L6	I/O		PC15/ROW	Touch panel row
L7	I/O		PC14/ROW	Touch panel row
L8	I/O		PA15/SPI2_NSS(remap)/TIM3_CH4/TIM2_CH4 (remap)/JTDI/COL	SPI2 slave select (remap) TIM3 CH4 TIM2 CH4 (remap) JTAG data input Touch panel column
L9	I/O		PH0/COL	Touch panel column
L10	I/O		PH10/COL	Touch panel column

Table 3. STM32TS60 pin definitions (continued)

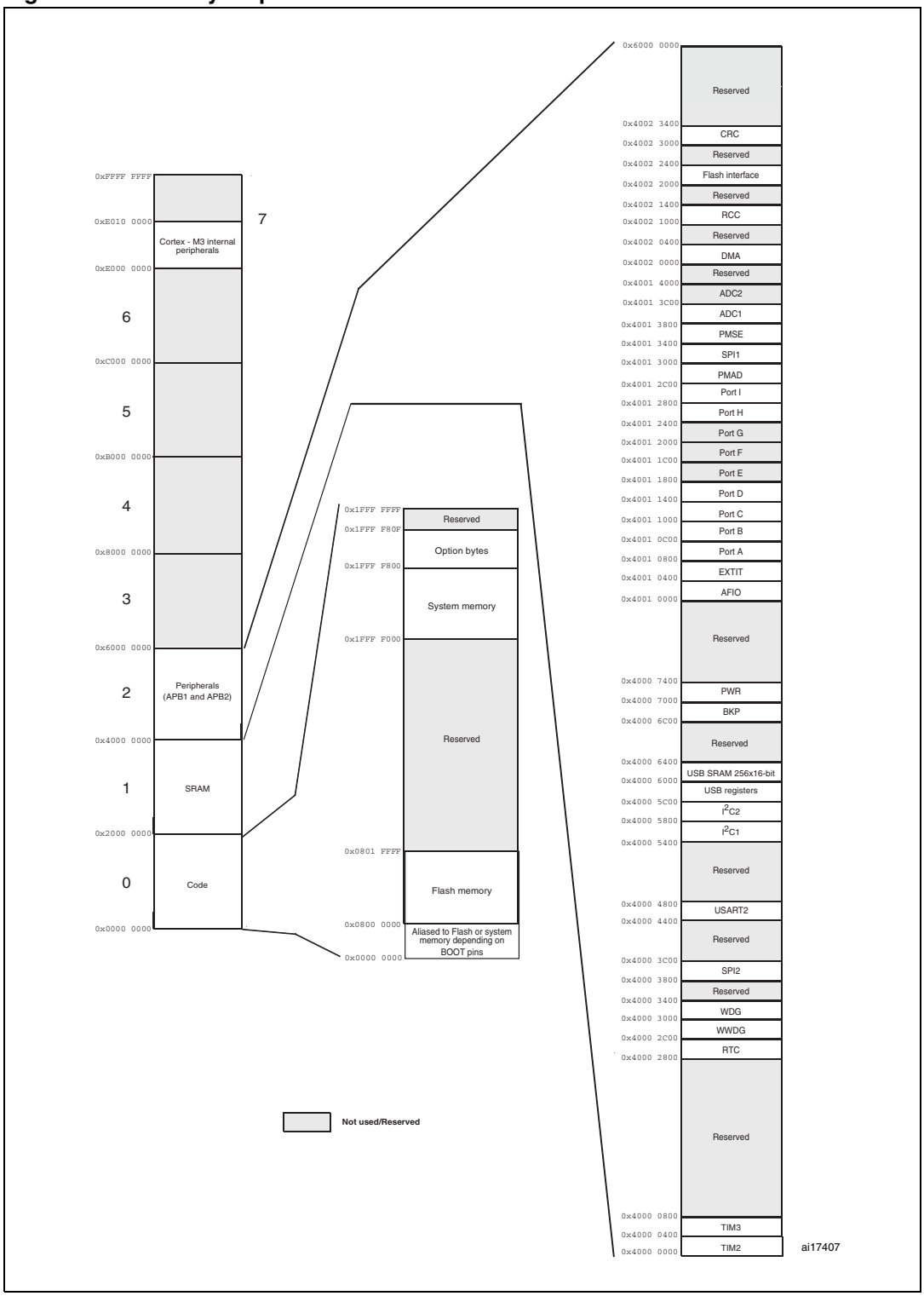
Pin no.	Pin type(1)(2)	Pin level(3)	PIn name	Pin function
L11	I/O		PH4/COL	Touch panel column
L12	I/O		PH12/COL	Touch panel column
M1	I/O		PD8/ROW	Touch panel row
M2	I/O		PD10/ROW	Touch panel row
M3	I/O		PD13/ROW	Touch panel row
M4	I/O		PD15/ROW	Touch panel row
M5	I/O		PC7/ROW	Touch panel row
M6	S		VDD_2	Supply voltage pin 2
M7	S		VSS_2	Ground pin 2
M8	I/O		PB5/TIM2_ETR/TRACECLK/COL	TIM2 external trigger Trace clock Touch panel column
M9	I/O		PH1/COL	Touch panel column
M10	I/O		PH5/COL	Touch panel column
M11	I/O		PH6/COL	Touch panel column
M12	I/O		PH3/COL	Touch panel column

1. I = input pin, O = output push-pull, I/O = input/output, OD = output open drain, S = supply pin
2. Under reset, I0s are configured in input floating mode.
3. FT = 5 V tolerant

4 Memory mapping

The memory map is shown in *Figure 3*.

Figure 3. Memory map



5 Package characteristics

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at *www.st.com*.

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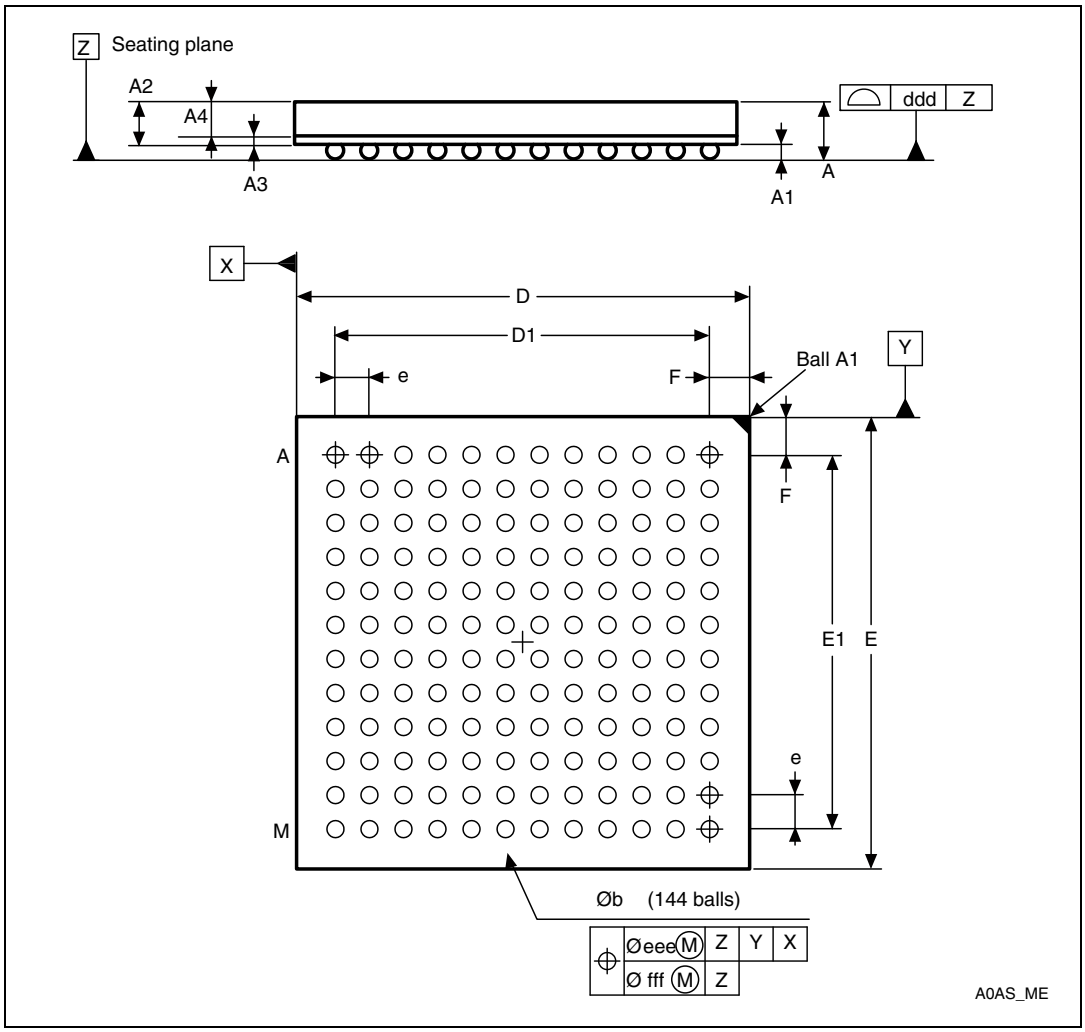
Figure 4. UFBGA144 - 7 x 7 mm ultra low profile fine pitch ball grid array package outline



1. Drawing is not to scale.

Table 4. UFBGA144 - 7 x 7 mm ultra low profile fine pitch ball grid array package mechanical data

Symbol	millimeters			inches[1]		
	Typ	Min	Max	Typ	Min	Max
A	0.530	0.460	0.600	0.0209	0.0181	0.0236
A1	0.080	0.060	0.100	0.0031	0.0024	0.0039
A2	0.450	0.400	0.500	0.0177	0.0157	0.0197
A3	0.130	0.080	0.180	0.0051	0.0031	0.0071
A4	0.320	0.270	0.370	0.0126	0.0106	0.0146
b	0.250	0.200	0.300	0.0098	0.0079	0.0118
D	7.000	6.950	7.050	0.2756	0.2736	0.2776
D1	5.500	5.450	5.550	0.2165	0.2146	0.2185
E	7.000	6.950	7.050	0.2756	0.2736	0.2776
E1	5.500	5.450	5.550	0.2165	0.2146	0.2185
e	0.500	0.450	0.550	0.0197	0.0177	0.0217
F	0.750	0.700	0.800	0.0295	0.0276	0.0315
ddd	0.100			0.0039		
eee	0.150			0.0059		
fff	0.050			0.0020		

1. Values in inches are converted from mm and rounded to four decimal digits.

6 Ordering information

Table 5. Ordering information scheme for package devices

Example: STM32 TS 60 Z H 6

Device family

STM32 = ARM-based 32-bit microcontroller

Device sub-family

TS = touchscreen family

Touch sensing technology

60 = multitouch resistive

Pin count

Z = 144 pins

Package

H = UFBGA

Temperature range

6 = industrial temperature range –40°C to 85°C

For further information on any aspect of this device, please contact your nearest ST Sales Office.

The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

Table 6. Ordering information for die devices

Die part number	Memory (Kbytes)	Package	Temperature
STM32TS60DIE1	32	Unsawn wafer	-40 °C to 85 °C

7 Revision history

Table 7. Document revision history

Date	Revision	Changes
16-Dec-2009	1	Initial release
02-Feb-2010	2	Added unsawn wafer to *Features*. Updated *Table 1: STM32TS60 device summary*. Updated *Figure 1* and added *Figure 2* and *Figure 3* ballouts. Replaced *Table 2: STM32TS60 single-chip pin definitions*. Added *Table 3: STM32TS60 dual-chip pin definitions*. *Figure 4: Single-chip typical application schematic for 2.5" to 6" panels*: updated title and pins; added footnote. *Figure 5: Dual-chip typical application schematic for 6" to 10.1" panels*: updated title, added SPI2_NSS pin, and added footnote. Passive component list *Table 4* and *Table 5*: updated title and footnotes. Added *Section 5: Package characteristics*. Renamed *Section 6: Ordering information*.
31-Mar-2011	3	The STM32TS60 is no longer an ASIC MCU but a standard STM32 MCU. Consequently, the title of this document has been changed and the *Features* and *Description* were updated, re-written, and/or edited. Added *Section 1: Introduction*, *Figure 1: STM32TS60 device block diagram*. Removed *Section 2.2: Main benefits*. Added *Section 2.2: Peripheral overview*. Removed ballout diagrams "STM32TS60 single-chip UFBGA144 ballout top view", "STM32TS60 dual-chip (master) UFBGA144 ballout top view", and "STM32TS60 dual-chip (slave) device UFBGA144 ballout top view" and replaced them with *Figure 2: STM32TS60 device UFBGA144 ballout*. Added *Section 4: Memory mapping*. Removed "Application diagrams" section. Replaced the title "*Package mechanical data*" with *Package characteristics*. *Table 5: Ordering information scheme for package devices*: updated title; removed 'xx' (firmware configuration) and 'y' (firmware revision) which are no longer part of the ordering scheme. Added *Table 6: Ordering information for die devices*.

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