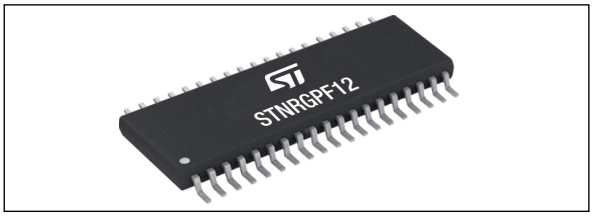
STNRGPF12

2-channel interleaved PFC driver with embedded digital inrush current limiter function

Datasheet - production data



Features

- Digital inrush current limiter function
- Interleaved PFC digital controller
- Two interleaved channels PFC
- Continuous conduction mode
- Fixed frequency operation
- Average current mode control
- Mixed signal architecture
- Soft start-up management
- Burst mode support
- Load feed forward
- Input voltage feed forward
- Channel current balance function
- Programmable phase shedding
- Status indicator signaling for cooling system, PFC Fault and PFC OK
- Configurable driver by means of dedicated graphic tool
- Programmable fast overcurrent and thermal protection
- Serial communication port available for:
  - Device programming;
  - Monitoring of the PFC parameters
- Suitable for >600 W applications:
  - Welding, air conditioner
  - Industrial motors
  - UPS, chargers, high power systems
- Customizable firmware
- Configuration via eDesign suite
- Embedded memory
  - Program memory: 32 Kbytes flash
  - Data retention 15 years at 85 °C after 10 kcycles at 25 °C
  - Data memory: 1 Kbyte true data E^2PROM; data retention: 15 years at 85 °C after 100 kcycles at 85 °C
  - Flash and E^2PROM with read while write (RWW) and error correction code (ECC)
  - RAM: 6 Kbytes
- Communication interfaces
  - UART asynchronous protocol for bootloader support and monitoring of the PFC parameters
- Operating temperature: -40 °C up to 105 °C

Description

The STNRGPF12 digital controller is designed for interleaved PFC boost topologies and intended for use in high power applications.

It features a digital inrush current control implemented with a solid state solution based on a silicon controlled rectifier. The controller can drive up to 2 interleaved channels.

The device works in CCM at fixed frequency with average current mode control, in applications based on a mixed signal (analog/digital) architecture.

The controller can be configured through a dedicated software tool (eDesignSuite) to match a wide range of specific applications. The tool generates a full schematic including a complete list of material and the final binary object code (FW) to be downloaded to the IC.

Table 1. Device summary

Part number	Package
STNRGPF12	TSSOP38

Contents

List of tables

List of figures

Documentation

This datasheet contains the description of features, pinout, pin assignment, electrical characteristics, mechanical data and ordering information.

- For information on programming, erasing and protection of the internal Flash memory, please refer to the RM0446 User Manual.

1 General description

The STNRGPF12 is a digital controller designed specifically for interleaved CCM boost PFC topologies that include also the active inrush current limiter function.

The Interleaving technique splits the PFC management into two or more parallel channels depending on the load condition. The driving signal is out of phase of a proper value.

This phase shift is calculated based on the number of paralleled channels according to the following formula:

Equation 1

$$Phase\ shift = \frac{360°}{number\ of\ channels}$$

The benefits of the interleaved topology, compared to traditional single stage PFC, are measured in terms of reduction of EMI filter and inductor volume, and a reduction of RMS capacitor current.

The STNRGPF12 contains all the control functions for designing a high efficiency-mode power supply with sinusoidal line current consumption.

It works in CCM, fixed frequency with average current mode control, implementing a mixed signal (analog/digital) control, joining the advantages of very high end digital solution without the typical limits of analog ones.

In the mixed signal approach the inner current loop is performed in hardware realizing an analog Proportional-Integral (PI) compensator, and the outer voltage loop is performed by a digital PI controller with fast dynamic response.

The STNRGPF12 can be configured by a dedicated software tool (eDesignSuite) in order to be customized for a specific application. So the user has to open the software tool, enter the converter specs and run the configurator. The results are: Schematic, BoM, and Binary code containing the parameters calculated by the tool.

The binary code can be downloaded into the STNRGPF12 through the programming section (by means of a serial interface) having a customized device that can be used like an analog device ready to use in application.

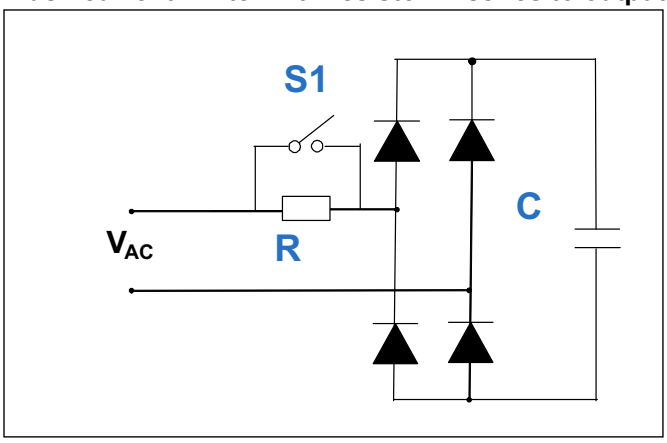
1.1 Inrush current limiter function description

The STNRGPF12 has embedded the Digital Inrush Current Limiter function. As soon as power supplies are connected to AC line, they are subjected to short-duration, high amplitude, input current called “Inrush Current”. The inrush current continues until the voltage across the internal capacitors reaches approximately the peak amplitude of the input AC line. If uncontrolled, the inrush current can damage the components of power supply. Several solutions can be adopted to limit this current and our devices are able to manage two control methods.

1.1.1 Inrush current limiter function with resistive element

The simplest method to limit the Inrush Current is to add a resistive element R (resistors, thermistors, etc.) in series with DC capacitors. *Figure 1* shows one implementation of this technique. As soon as the capacitor C is charged, no current flows, and the STNRGPF12 initiates the ON signal to switch S1 in order to short R. In this way the losses during normal operation are minimized.

Figure 1. Inrush current limiter with resistor in series to output capacitor

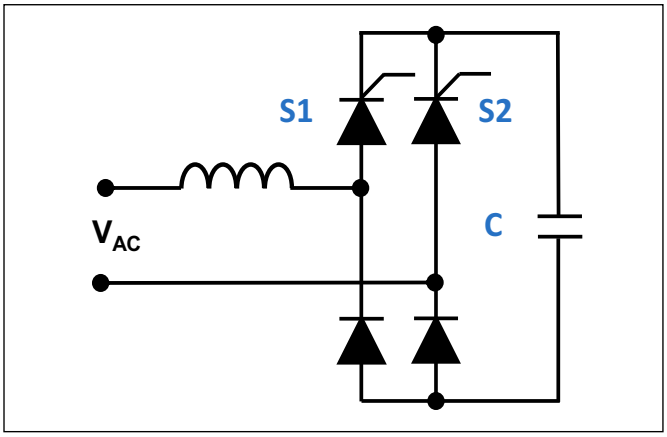


The S1 switch can be a silicon device as Triac or a mechanical switch of a relay.

1.1.2 Inrush current limiter function with controlled bridge

The second method to control the charge current of the output capacitor is to replace the input bridge rectifier with a controlled one and modulate progressively the conduction time of the switches S1 and S2 (see *Figure 2*). In this way the output capacitor can be charged smoothly avoiding overcurrent in the systems. One implementation of this method circuit may use Silicon Controlled Rectifier (SCR) as shown in the circuit in *Figure 2*. The high side of the input rectifier bridge is made up of SCRs S1, S2 and the low side are diodes.

Figure 2. Inrush current limiter with controlled rectifier bridge



This methodology can be applied only when an inductor is present on the line. In this case an inductor is already present because the application is an Interleaved PFC.

2 STNRGPF12 control architecture

As described above, the STNRGPF12 implements a mixed signal (analog/digital) control. The inner current loop is performed in hardware and the outer voltage loop is performed by a digital PI controller.

The device performs a cascaded control for voltage and current loops to regulate the output voltage by acting on the total average inductor current.

Figure 3. STNRGPF12 control scheme

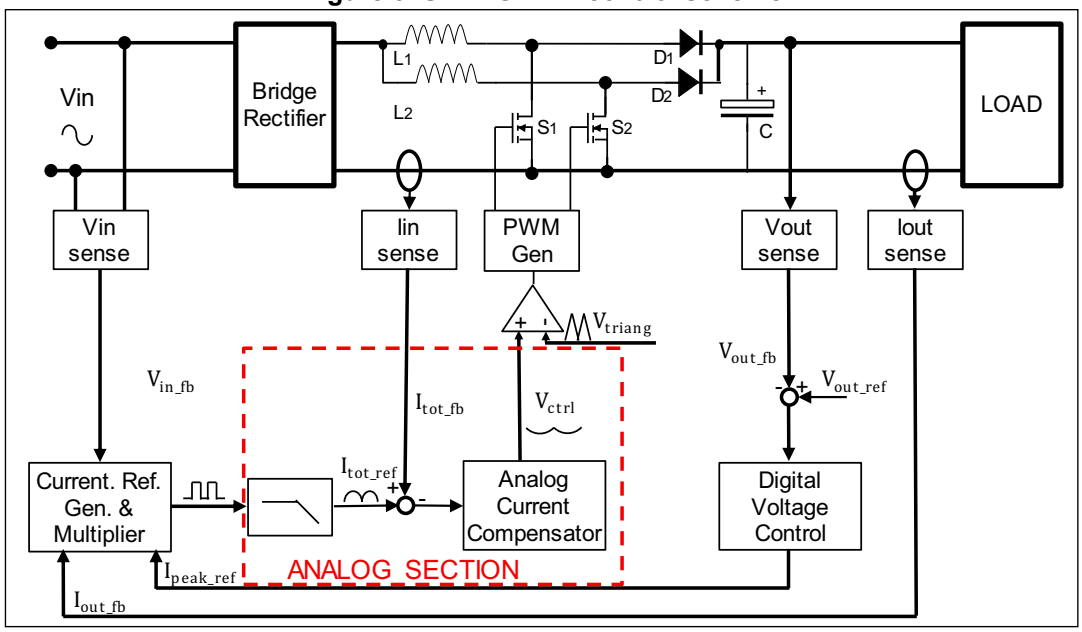


Figure 3 shows the STNRGPF12 control scheme. As can be seen, the difference between output voltage feedback vout_fb and reference vout_ref is sent to the Digital Voltage Control block (PI regulator) which calculates the peak of input average total current ipk_ref.

The PFC current reference is internally generated and comes out from the Multiplier block as PWM signal. After filtering, it became the total average sinusoidal input current reference itot_ref for inner current loop (analog section, red line). The difference between the current reference itot_ref and the input current feedback Itot_fb is sent to the Analog Current compensator PI.

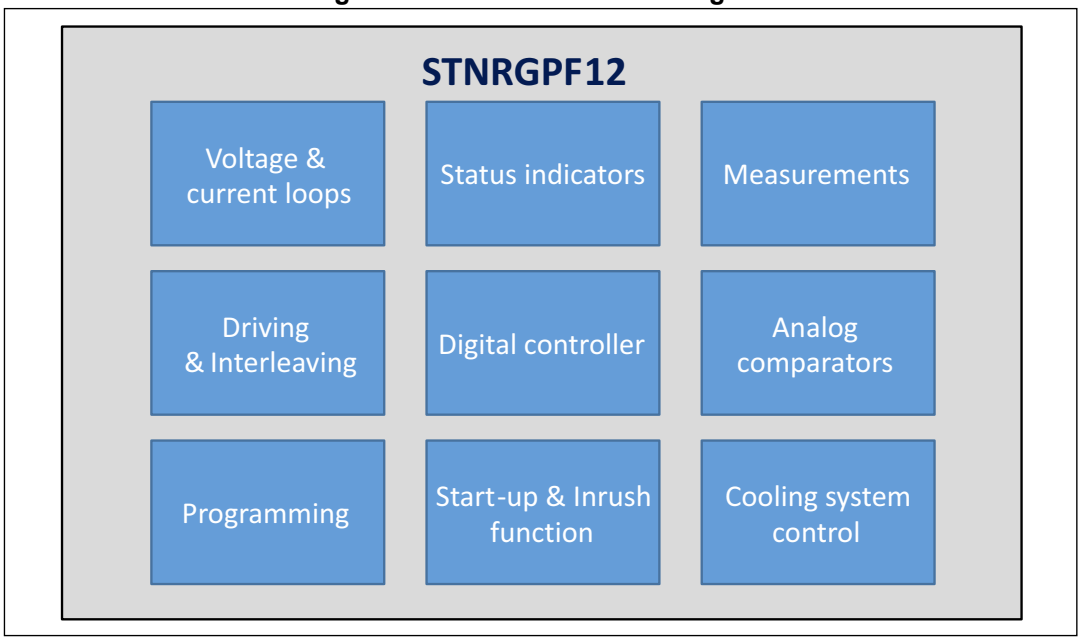
So the master PWM signal is generated by comparing the analog PI output Vctrl and a triangular wave Vtriang at switching frequency. Finally, an interleaving operation is performed and two PWM signals 180° phase shifted drive S1 and S2 power switches.

Moreover, the digital section includes an input voltage and load feedforward for fast transient response when main voltage changes suddenly or a load step current occurs, avoiding large over or under-voltage on output capacitor C.

3 STNRGPF12 block diagram

The block diagram of the STNRGPF12 device is shown in *Figure 4*.

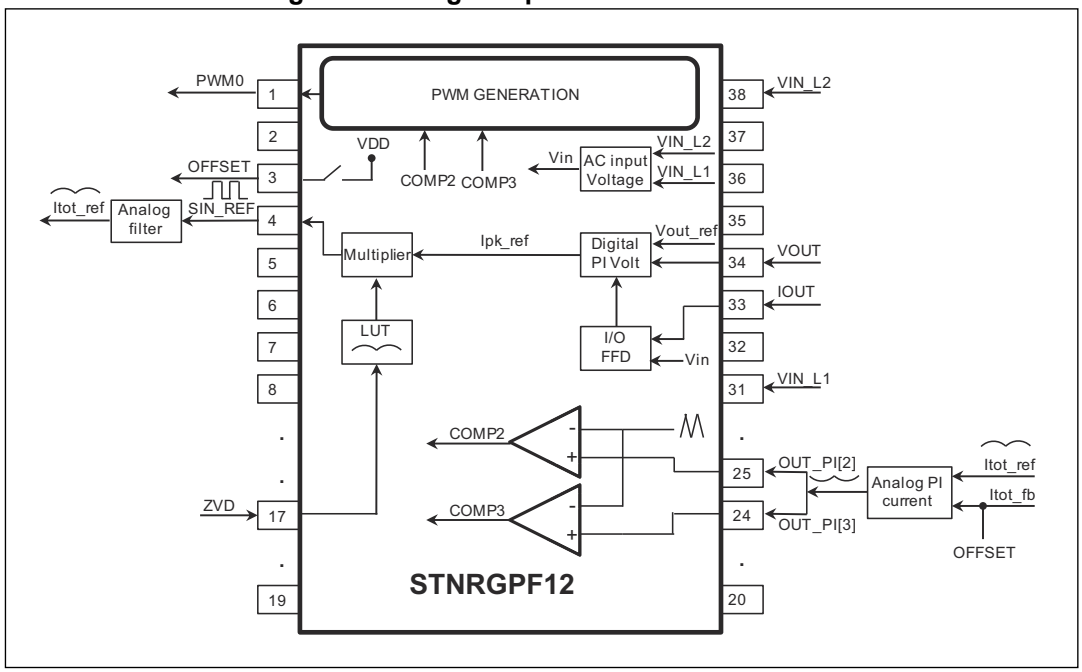
Figure 4. STNRGPF12 block diagram



3.1 Voltage and current loops

The STNRGPF12 implements a mixed signal average current control. The task of the digital voltage loop is to regulate the output voltage of the PFC. Vin and Iout measurements are used to implement Input/Output Feed-Forward (I/O FFD), so load steps or input voltage variations are quickly compensated by acting on digital PI output calculations. This function allows to keep the output voltage to the setpoint value and as constant as possible (see *Figure 5*).

Figure 5. Voltage loop and current reference



The output of digital PI is the peak current reference. In order to obtain a sinusoidal current reference, Ipk_ref is multiplied by a Look-Up Table (LUT). The LUT is synchronized with the input voltage thanks to the ZVD signal (pin 17). The output of the multiplier is a PWM signal having sinusoidal Duty Cycle that is configured on pin 19 SIN REF.

An analog filter is used to obtain the final sinusoidal current reference for the external current loop (Itot_ref). The analog current PI compares the reference Itot_ref with the total input current feedback (Itot_fb) and generates the duty cycle wave for PWM modulation. The master PWM signal is obtained by comparing (COMP2,3) the output of current PI with a triangular wave at switching frequency (see Analog comparators section and PWM section).

3.2 Measurements section

The STNRGPF12 includes 4 input measurement channels. These inputs are defined from pin 31 to pin 38 and they are specified below.

- Pin 31. Vin_L1: AC input voltage measurement Line 1;
- Pin 32. Temp: ambient temperature;
- Pin 33. Iout: PFC output current;
- Pin 34. Vout: PFC output voltage;
- Pin 35. I[0]: RMS current channel [0];
- Pin 36. I[1]: RMS current channel [1];
- Pin 38 AVin_L2: AC input voltage measurement Line 2.

3.2.1 AC input voltage measurement

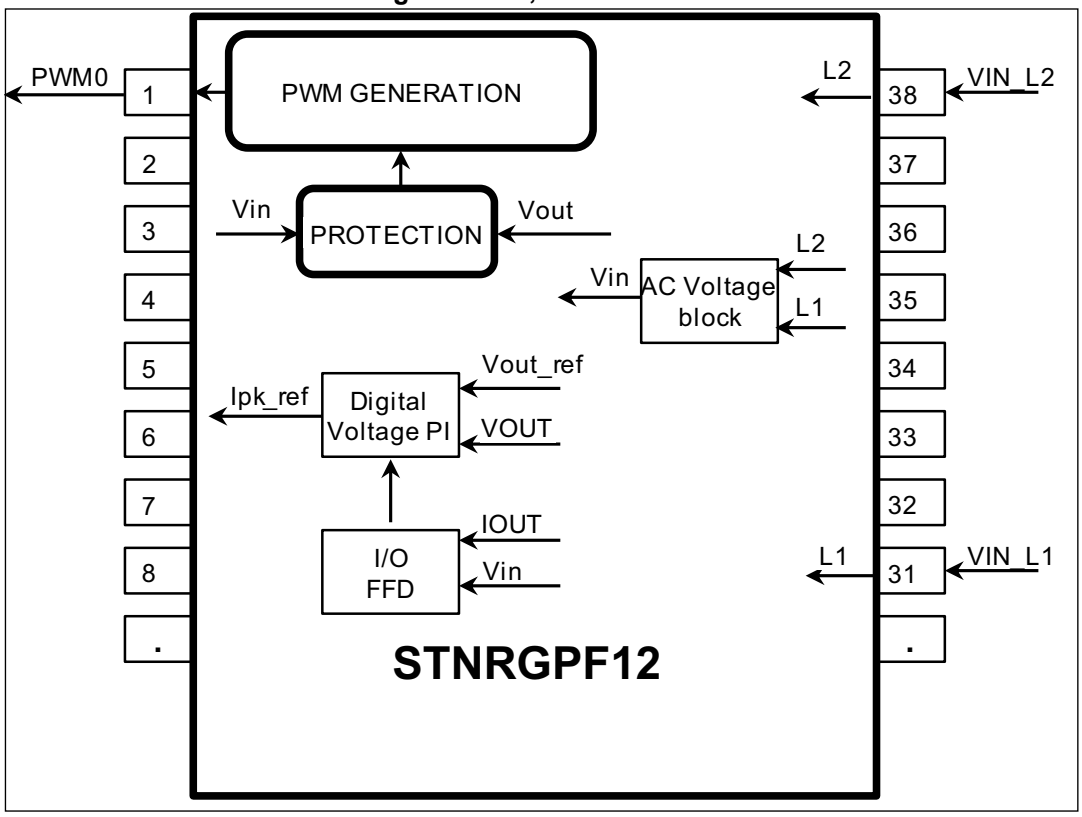
The STNRGPF12 has two dedicated pins, pin 31 and pin 38, for AC RMS line voltage measurement. The device, by means of two resistor dividers, measures simultaneously the

instantaneous voltage on both pins, performs the difference between them and calculates the RMS value (see *Figure 6* Vin_fb signal). Vin_fb (RMS AC input voltage) is used for the following functions:

a) Normal operation. Used to generate the sinusoidal current reference signal.

b) AC input voltage variation. This signal is used to implement the voltage input feed forward. The input voltage feed forward modifies the PI output, compensating rapidly the effect of the line voltage changes. See *Figure 6*.

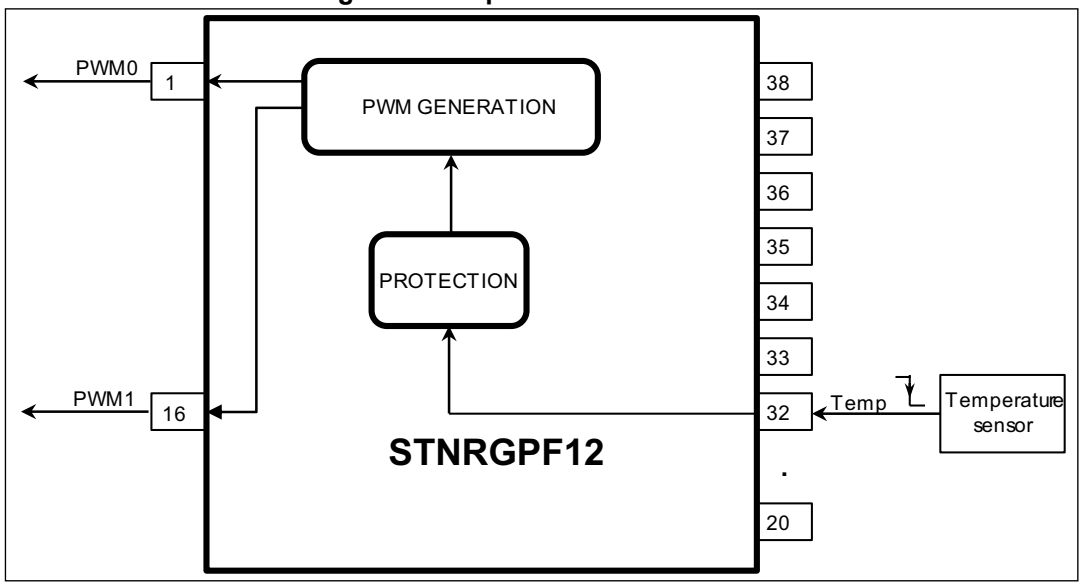
Figure 6. Vin, measurement



3.2.2 Ambient temperature measurements

Pin 32, Temp. Input for board temperature measurement. The PWM activity is stopped when the temperature exceeds the user defined threshold. See *Figure 7*. If the voltage on the Temp pin falls below a defined threshold, the device stops the system.

Figure 7. Temperature measurement



The admissable voltage that the pin can accept is between 0 and 1023 V.

3.2.3 Output current measurement

Pin 33, Iout. PFC output current. The measurement of this current allows to implement the following functions.

- Load feedforward. The input current reference is modified proportionally to the load, in order to give a faster response versus load transient.
- Channels power management. Each channel can be enabled or disabled based on output current level. For example, up to 50% of the load, only one channel may be enabled, above 50% two channel configurations can be selected.

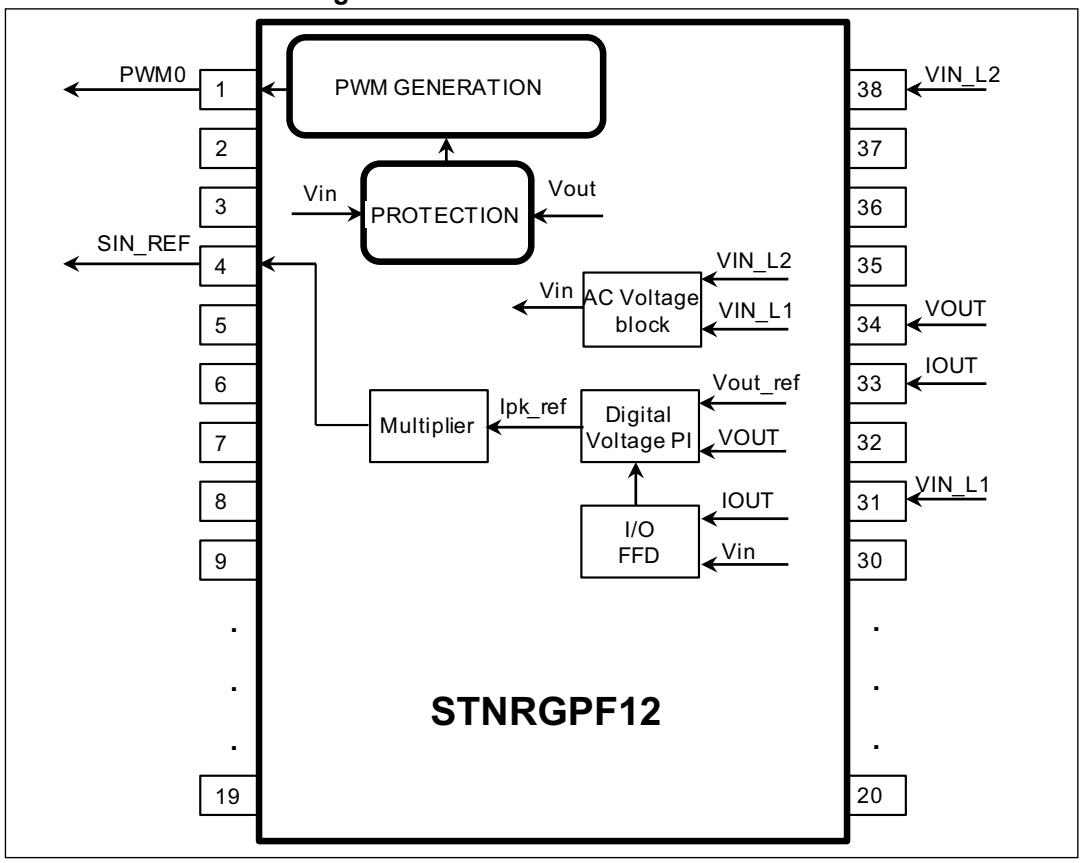
3.2.4 Output voltage sensing

Pin 34, Vout. Output voltage sensing. This feedback input is connected via a voltage divider to the boost output voltage. The voltage divider gives the Vout_fb to the Digital Voltage Control Block and is used in order to implement the following functions.

- Output voltage regulation
- Overvoltage protection

In *Figure 8* the block scheme of Vin Iout and Vout is reported.

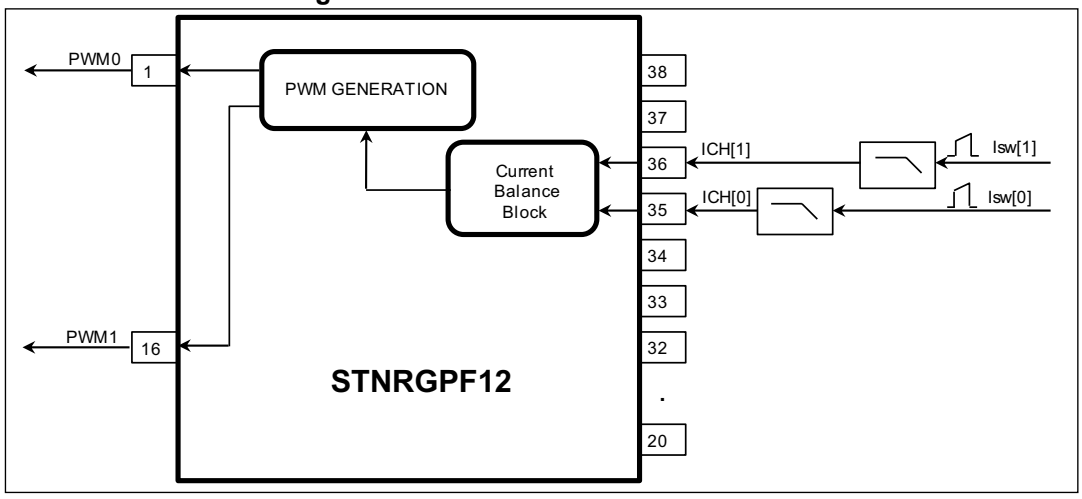
Figure 8. Iout and Vout measurement



3.2.5 Channel current measurement

Pin 35, pin 36. ICH[0], ICH[1]: channel current measurements. These pins measure the currents flowing in each channel. The signal coming from sensing resistors is sent to a low pass filter and finally it's connected to pin 35 and pin 36. The low pass filter must be sized so that its passband is about ten times lower than the switching frequency of the single channel. The result of this measurement is internally used to perform the current balance between the two channels.

Figure 9. Channel current measurement



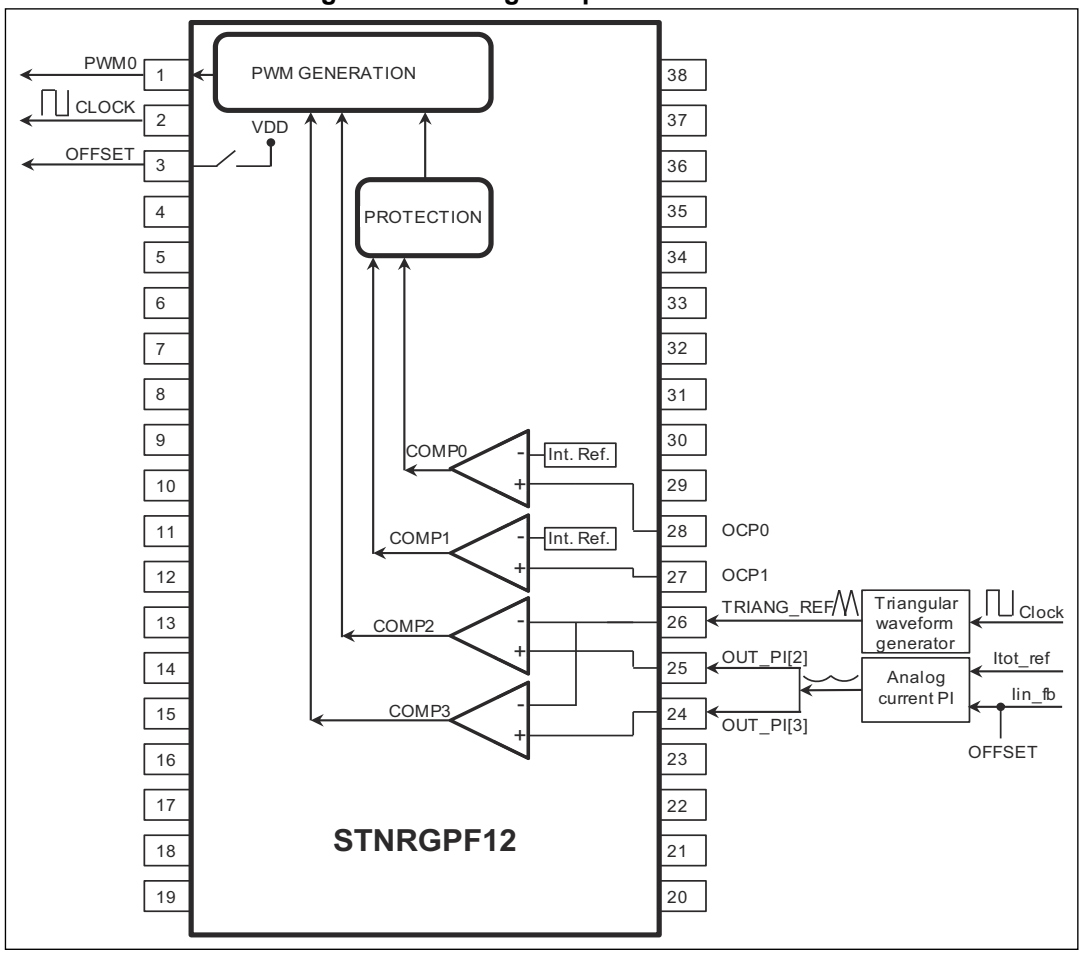
3.3 Analog comparators section

The STNRGPF12 includes four fast analog comparators, COMP0 … 3.

COMP3 and COMP2 have external reference voltage and are used to define the duty cycle of PWM0 master.

COMP1 and COMP0 have internal reference voltage and are used to realize overcurrent protections.

Figure 10. Analog comparators section



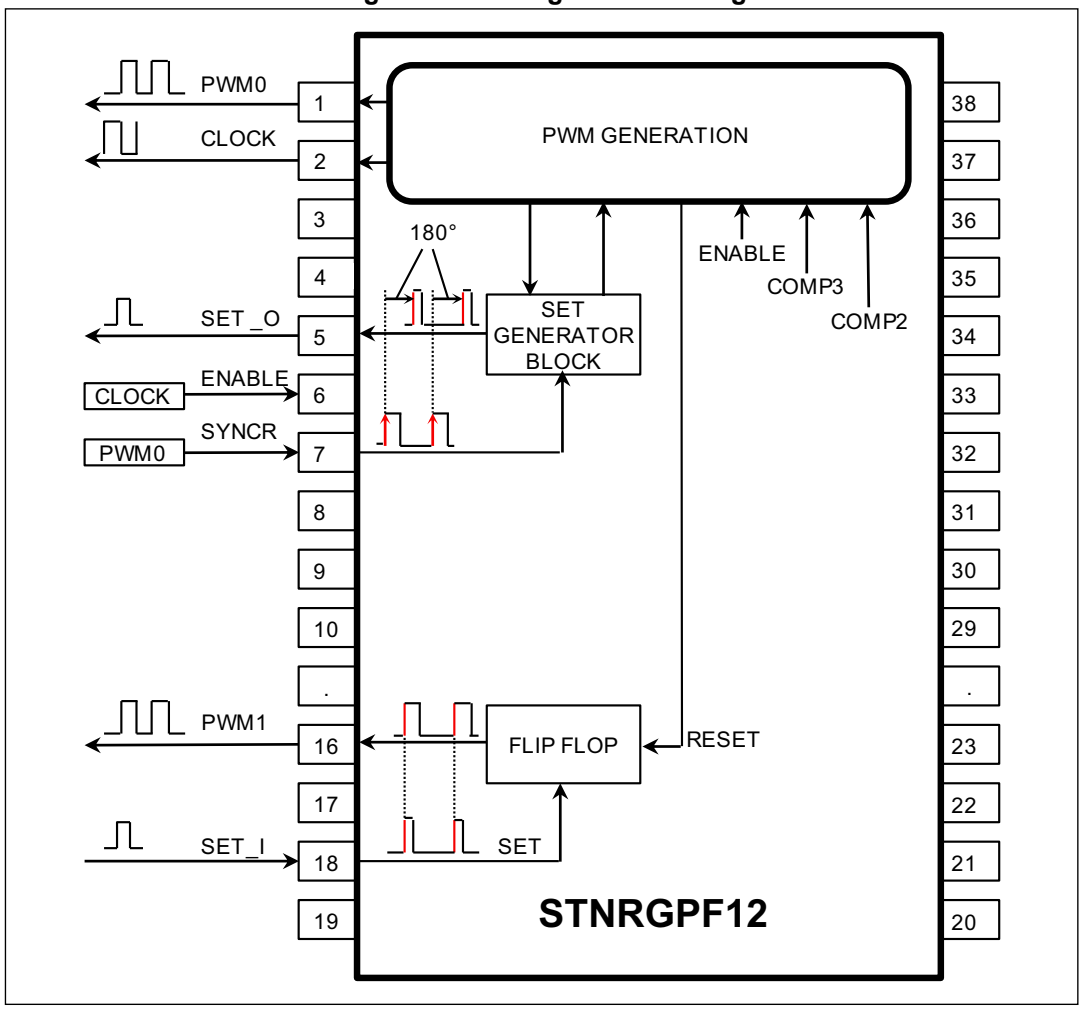
A description of the comparator pins is reported below.

- Pin 24 OUT_PI[3]: Positive input of COMP3. It receives the out of analog PI current.
- Pin 25 OUT_PI[2]: Positive input of COMP2. It receives the out of analog PI current.
- Pin 26 TRIANG_REF: Negative common input analog COMP2,3. It receives the reference triangular waveform.
- Pin 27: Positive input of COMP1. It receives the sensing signal of total input current.
- Pin 28: Positive input of COMP0. It receives the sensing signal of all switch currents. COMP0 stops the driving when an overcurrent occurs in any switch.

3.4 Driving & Interleaving

The STNRGPF12 PWMs for channel driving are pins: 1 and 16. Below *Figure 11* shows the configuration for PWM generation.

Figure 11. Driving & interleaving



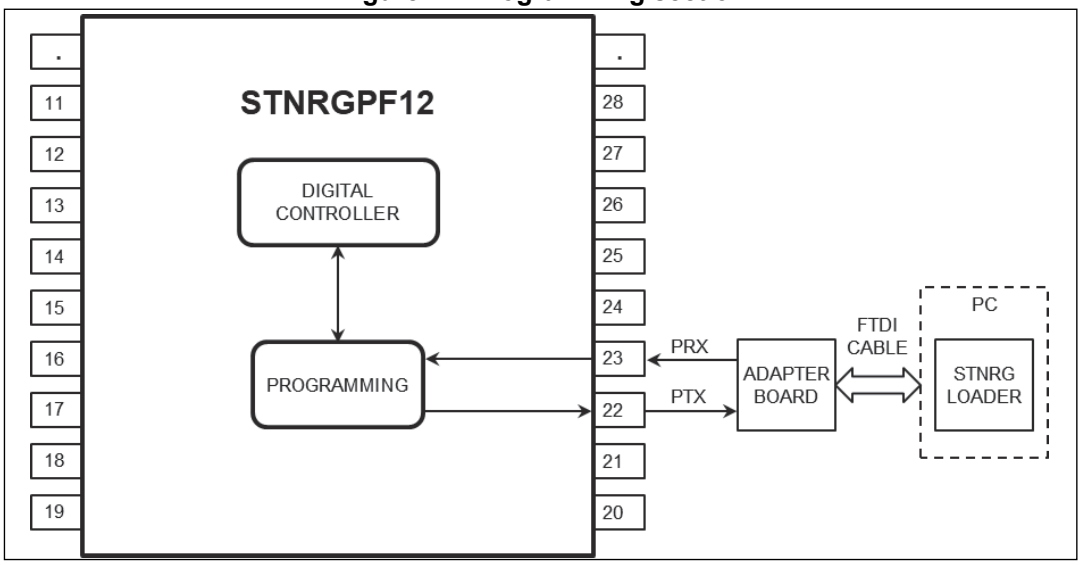
Once the device is programmed as soon as the device is supplied, the following sequence to generate the PWM starts:

1. Pin n. 2 emits CLOCK signal at selected switching frequency. This pin must be connected to the ENABLE pin (n. 6) and the clock signal is internally used in order to enable the PWM GENERATION block. The ENABLE signal, moreover, is used to avoid undesired commutations also when high level of noise is present.
2. The PWM0 signal triggers the SYNCR pin (n. 7) and internally the SET GENERATOR BLOCK generates the SET pulse with an out of phase of 180º (for a correct interleaving) with respect to the PWM0 signal. The SET fixes the “ON” instant of the PWM1 signal.
3. The SET signal comes out from the SET_O pin and enters into the SET inputs (pin 18 SET_I) of an internal FLIP FLOP.
4. The internal FLIP FLOP receives the SET from pin 18 and the RESET signal from the PWM GENERATOR BLOCK and in this way it is able to generate the PW1 with the right out of phase with respect to PWM0. The PWM1 comes out from pin 16 “PWM1”.

3.5 Programming section

Device programming is done by using: a PC with a dedicated loader software (STNRG LOADER), an FTDI cable and an adapter board (See *Figure 12*.)

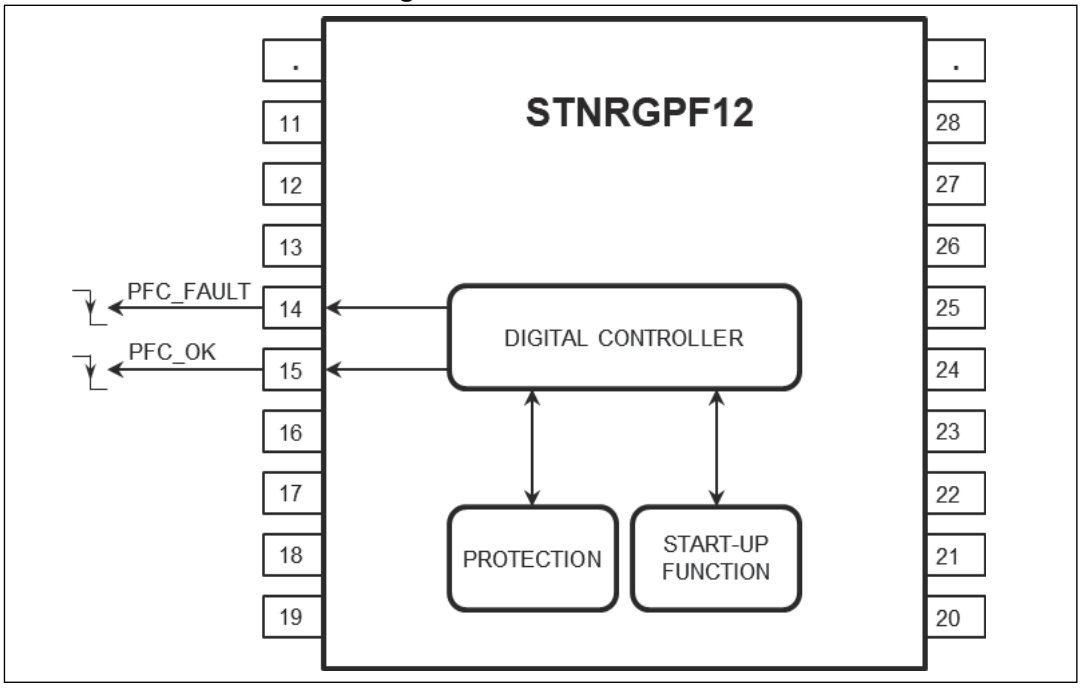
Figure 12. Programming section



3.6 Status indicator

The STNRGPF12 includes two pins to identify the running or fault status. These functions are defined on pin 14 and pin 15 (See *Figure 13*).

Figure 13. Status indicator

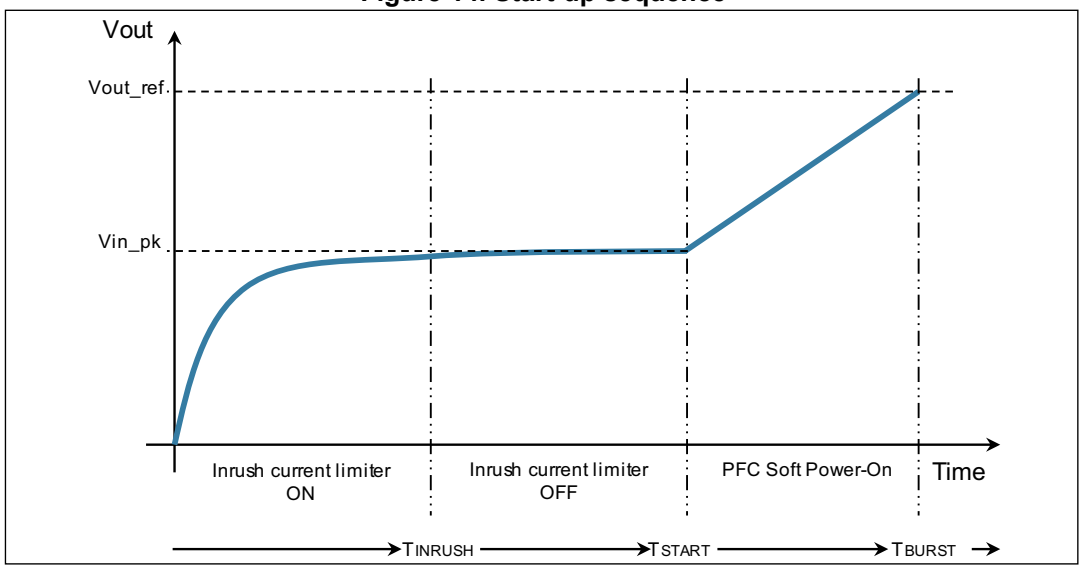


3.7 Startup & inrush current limiter function

The start-up function can be divided into two phases. The first phase is the Inrush Current Limiter and the second phase is the PFC Soft Power-On.

In *Figure 14*, the timing of the start-up sequence is reported.

Figure 14. Start-up sequence



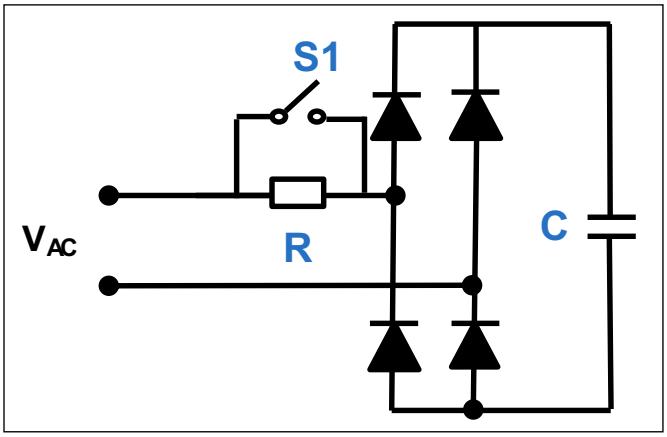
Initially the device performs the function of "Inrush Current Limiter" and after the Tinrush time it stops this phase. Sequentially it applies a short delay and at the end starts the PFC Soft Power-On procedure increasing the Vout voltage up to the nominal voltage (Vout ref).

3.7.1 Inrush current limiter function

The device embeds the Inrush Current Limiter Function. There are several topologies to perform this function but the most used are the following:

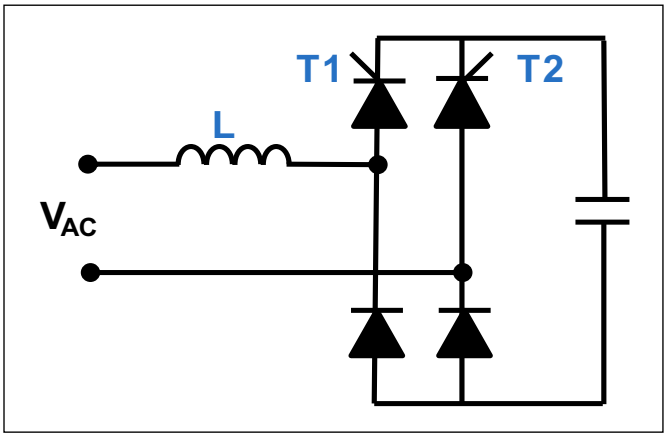
1. Inrush Current Limiter function with limiter resistor and bypass relay. This solution consist to insert a resistor in series with the output capacitors. The capacitor Inrush current is limited by a resistor or a thermistor. As soon as the capacitor is charged in order to reduce the power losses a switch in parallel to resistor will be closed. This switch can be a silicon based switch or mechanical contact of a relay.

Figure 15. Inrush current limiter function with limiter resistor and bypass relay



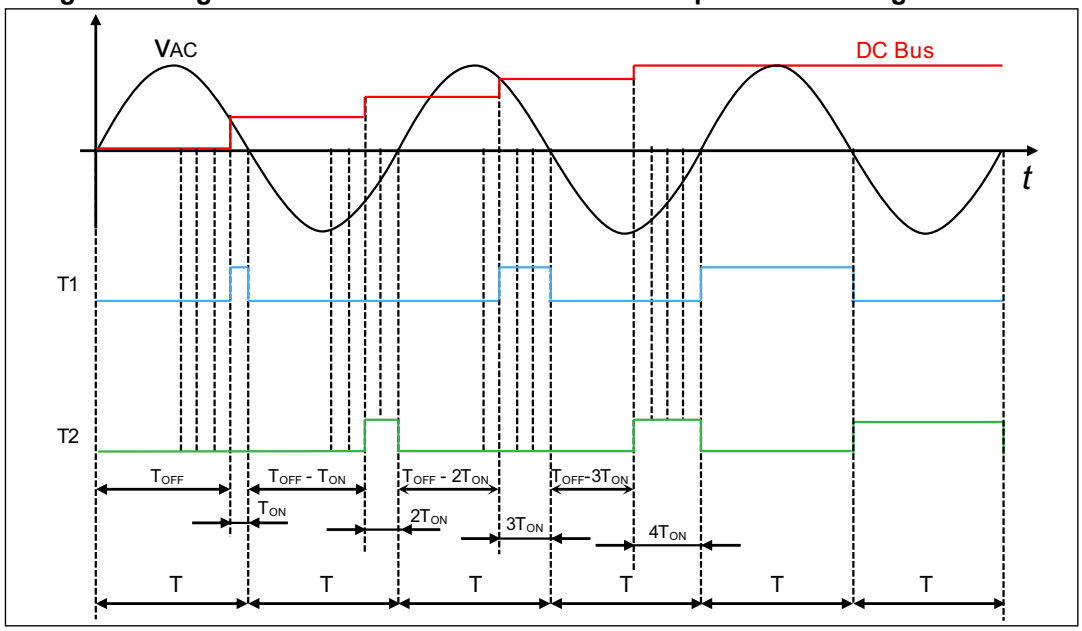
2. Digital Inrush Current Limiter function with a semi-controlled input bridge: Another topology use a semi-controlled bridge. This circuit use two silicon switches T1, T2 (Triac, SCR, Mosfet, IGBT….) and two separate diodes for the inrush path. The Switches T1, T2 are modulated ON and OFF by the controller in order to limit the peak current but this can work if an inductor is present in series with the line. (see *Figure 16*).

Figure 16. Digital inrush current limiter function with a semi-controlled input bridge



STNRGPF12 has embedded this technique, and it drives T1 and T2 alternately according the polarity of the mains and applying a short ON time. To reduce the inrush current the switches are triggered at the end of the line voltage. In this way the output capacitors initially are charged at low voltage and after it will increase smoothly allowing also a better control of the Inrush current.

Figure 17. Digital inrush current limiter function: sequence of driving of the SCR



In order to charge the output capacitors up to the peak voltage of AC mains, the switches T1 and T2 must be triggered on the following cycle with TON phase shift respect the previous one. (See *Figure 16*). If this Step Phase Shift is very short (few microseconds) from half cycle to half cycle, thanks to the presence of the PFC inductors, the capacitors will be charged maintaining low the line current. Usually this delay is constant and we call this technique “Constant Progressive Step Phase Control”.

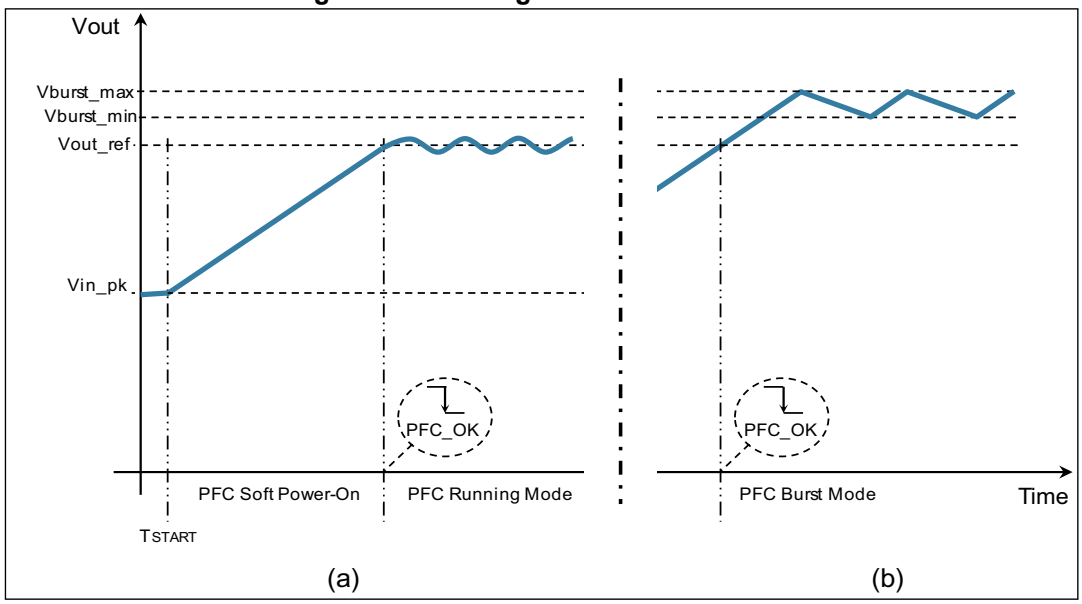
3.7.2 PFC soft power-ON

After the Inrush Current Limiter phase the device performs the Soft Power-On phase. The current reference generates a constant reference signal and both PWM0 and PWM1 channels are activated. In this phase the PFC output voltage increases up to the setpoint (Vout_ref).

As soon as the PFC Soft Power ON procedure is completed and the voltage reaches the setpoint Vout_ref (See *Figure*), the device performs the following operations:

- **The PFC_OK pin is pulled low**. When this pin is low, it indicates that the PFC is ready for load connection on the output.
- **The device enters in Burst Mode regulation**. The PFC output voltage oscillates between two settable levels (Vburst_min and Vburst_max). These levels can be defined during device customization.

Figure 18. Running mode or burst mode



As soon as the PFC_OK pin becomes low, two conditions may occur:

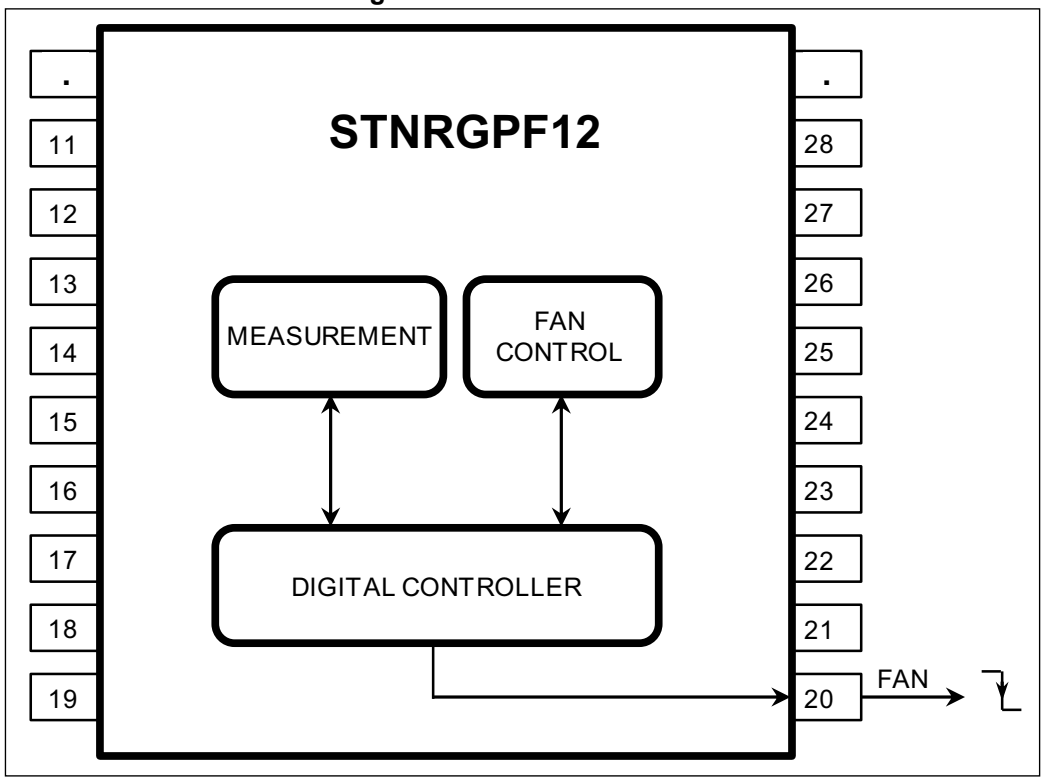
a) The load is applied. The device immediately regulates the output voltage at Vout_ref value. *Figure 18* (a)

b) The PFC remains in no-load condition: the output voltage ranges between Vburst_min and Vburst_max until the load is applied (*Figure 18*) (b).

3.8 Fan control

The device offers the possibility to realize a control on the cooling system. The customer defines the power level for the function activation. Pin 20, FAN gives a CMOS/TTL signal that became low for a power level higher than the specified threshold. See *Figure 19*.

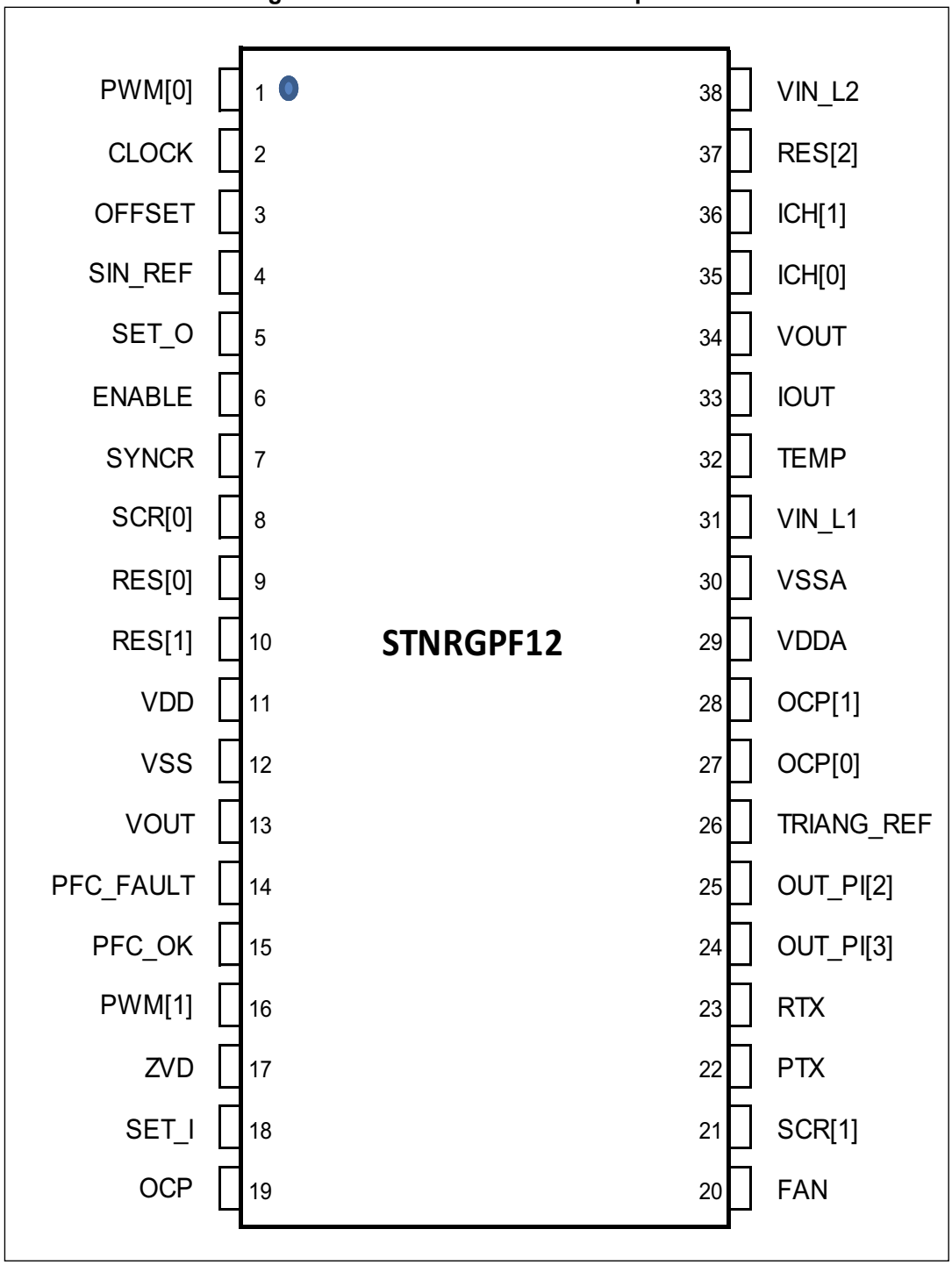
Figure 19. Fan Control function



4 Pinout and pin description

4.1 Pinout

Figure 20. STNRGPF12 - TSSOP38 pinout



4.2 Pin description

Table 2. Pin description

N	TYPE(*)	NAME	PIN DESCRIPTION
1	OP	PWM[0]	This pin generates the PWM0 for the channel CH0
2	O	CLOCK	This pin generates a PWM signal at selected working frequency having duty cycle of 50%. This signal is used to generate a triangular waveform at switching frequency by means of an external op_amp. The CLOCK signal is also used to realize a protection against undesired commutations
3	O	OFFSET	This pin generated a PWM signal in order to compensate the offset of the external operational amplifier that performs the current loop PI compensator.
4	OP	SIN_REF	This pin generates a PWM signal with sinusoidal duty cycle. This PWM signal must be filtered in order to have the current sinusoidal reference that is synchronized with input voltage mains.
5	OP	SET_O	This pin generates a pulse in order to trigger set ON the CH1 channel with the right out of phase. This pin must be connected to pin 18
6	I	ENABLE	This pin receives the CLOCK signal in order to avoid undesired commutation
7	I	SYNCR[2]	This pin receives the PWM0 signal in order to synchronize the others channels. The falling edge of the PWM0 signal is used to trigger OFF the slave channels CH1 and CH2
8	OP	SCR[0]	This pin generates the PWM in order to drive one of the Inrush Current Limiter switches. Usually an SCR is used to perform this function.
9	NC	RES[0]	Reserved
10	NC	RES[1]	Reserved
11	PS	VDD	Supply voltage
12	PS	VSS	Ground
13	PS	VOUT	Supply voltage of digital section. An external capacitor must be connected to the VOUT pin.
14	O	PFC_FAULT	During normal operation this pin is high. If a fault condition occurs, it's forced low.
15	O	PFC_OK	During fault condition this pin is high. When the PFC is ready for load connection, it's forced low.
16	OP	PWM[1]	This pin generates the PWM for the channel CH1
17	I	ZVD	This pin receives a square wave signal synchronized with input AC voltage. The rising edge of square wave signal is used by the STNRGPF12 to detect the ZVD instant.

Table 2. Pin description (continued)

N	TYPE(*)	NAME	PIN DESCRIPTION
18	I	SET_I	This pin receives a pulse in order to trigger ON the CH1 channel. This pin must be connected to pin 5
19	O	OCP	During normal operation this pin is high. If an overcurrent occurs, it's forced low instantaneously
20	O	FAN	It generates a CMOS/TTL signal that is low until the PFC output power is below a threshold defined during device customization
21	OP	SCR[1]	This pin generates the PWM in order to drive one of the Inrush Current Limiter switches. Usually an SCR is used to perform this function
22	O	PTX	Programming data transmit
23	I	PRX	Programming data receive
24	AI	OUT_PI[3]	Positive input of internal analog comparator 3. It receives the out of analog PI current
25	AI	OUT_PI[2]	Positive input of internal analog comparator 3. It receives the out of analog PI current
26	AI	TRIANG REF	Negative input analog comparators 3 and 2. It receives voltage triangular waveform
27	AI	OCP[0]	Input overcurrent protection
28	AI	OCP[1]	Inductor overcurrent protection
29	PS	VDDA	Analog supply voltage
30	PS	VSSA	Analog ground
31	MI	VIN	This pin is one of the two inputs for the RMS input voltage measurements. A divider resistor is connected to line/neutral input wire
32	MI	TEMP	This pin measures the ambient board temperature. As soon as the voltage decreases below a settable threshold the switching activity is stopped
33	MI	IOUT	This pin measures the PFC output current
34	MI	VOUT	This pin measures the PFC output voltage
35	MI	ICH[0]	This pin measure the RMS current for channel CH[0]
36	MI	ICH[0]	This pin measure the RMS current for channel CH[1]
37	RI		Reserved. This pin must be pulled down by means of a 10k resistor
38	MI	VIN	This pin is one of the two inputs for the RMS input voltage measurements. A divider resistor is connected to line/neutral input wire

(*) Legend

In the following table the legend of pin type is shown.

Table 3. Legend of the pins

TYPE	Pin identification
OP	PWM driver
O	Digital output
I	Digital input
I/O	Digital bidirectional
PS	Power supply
AI	Analog input
MI	Measure input

4.3 Input/output specification

The STNRGPF12 family includes three different I/O types:

- Normal I/Os (O or I);
- Fast I/O (OP);
- High speed I/O (CLOCK).

The STNRGPF12 I/Os are designed to withstand current injection. For a negative injection current of 4 mA, the resulting leakage current in the adjacent input does not exceed 1 µA.

5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}. V_{DDA} and V_{DD} must be connected to the same voltage value. V_{SS} and V_{SSA} must be connected together with the shortest wire loop.

5.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with the ambient temperature at T_A = 25 °C and T_A = T_A max. (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated according to each table's specific notes and are not tested in production.

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} and V_{DDA} = 3.3 V. They are given only as design guidelines and are not tested. For the measurement section the accuracy is determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range.

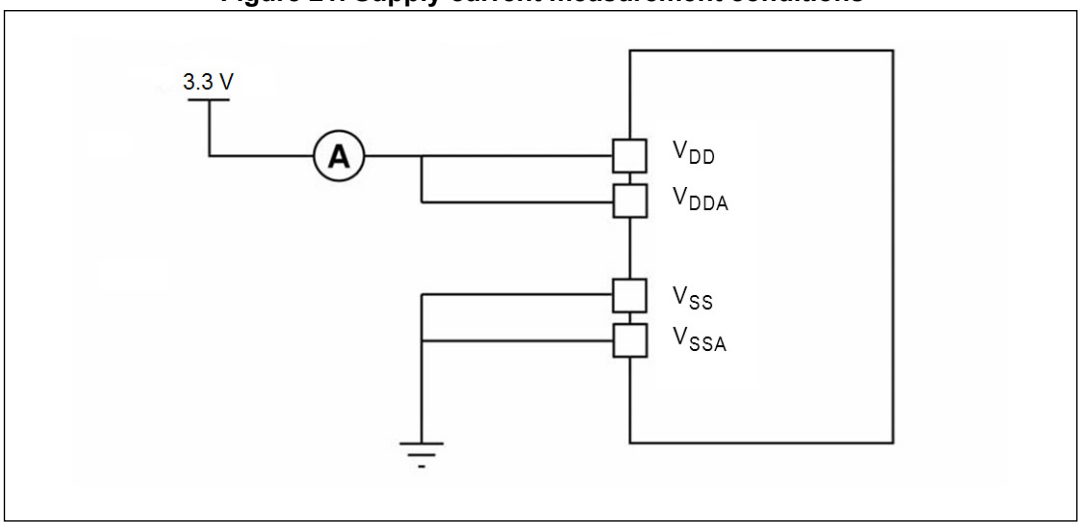
5.1.3 Typical curves

Unless otherwise specified, all typical curves are given as design guidelines only and are not tested.

5.1.4 Typical current consumption

For typical current consumption measurements, V_{DD} and V_{DDA} are connected as shown in *Figure 21*.

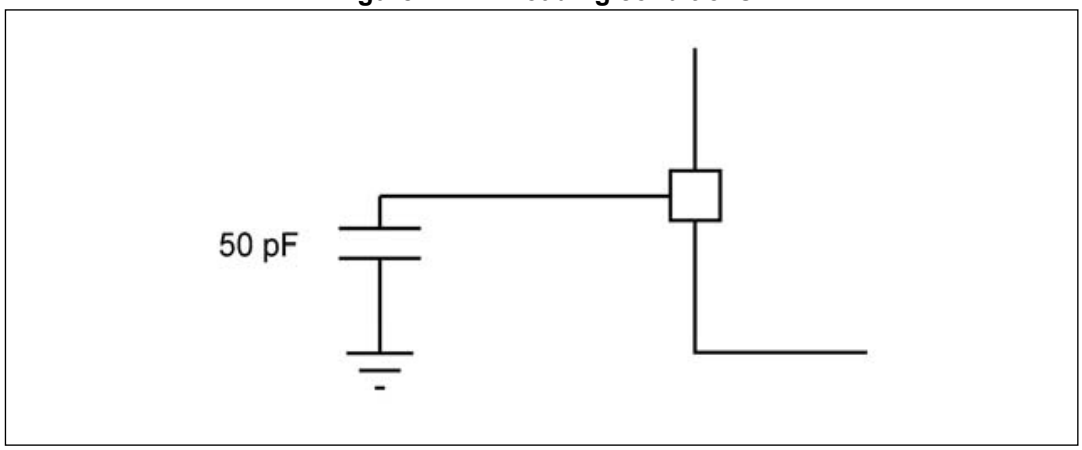
Figure 21. Supply current measurement conditions



5.1.5 Loading capacitors

The loading conditions used for pin parameter measurement are shown in *Figure 22*.

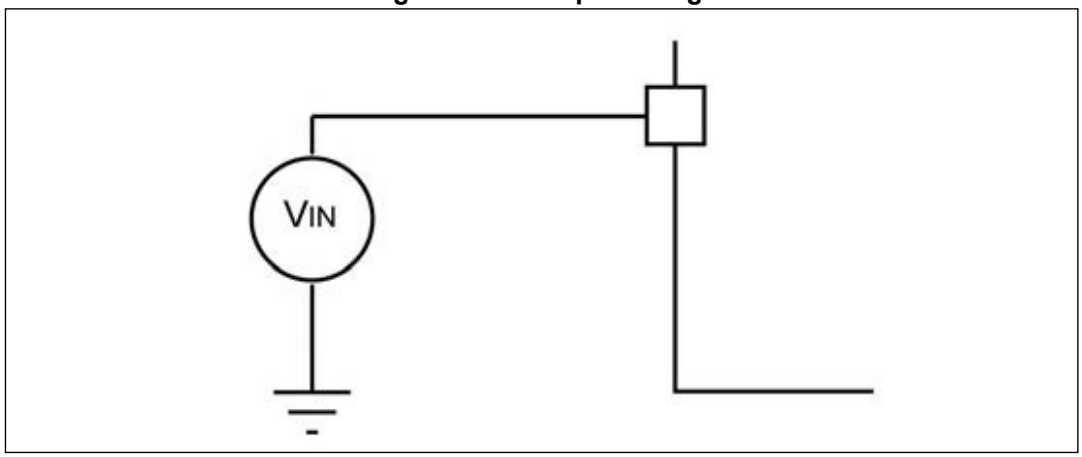
Figure 22. Pin loading conditions



5.1.6 Pin output voltage

The input voltage measurement on a pin is described in *Figure 23*.

Figure 23. Pin input voltage



5.2 Absolute maximum ratings

Stresses above those listed as 'absolute maximum ratings' may cause permanent damage to the device. This is a stress rating only and the functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect the device reliability.

Table 4. Voltage characteristics

Symbol	Ratings	Min.	Max.	Unit
V_{DDX} - V_{SSX}	Supply voltage(1)	-0.3	6.5	V
V_{IN}	Input voltage on any other pin(2)	V_{SS} - 0.3	V_{DD} + 0.3	
V_{DD} - V_{DDA}	Variation between different power pins	-	50	mV
V_{SS} - V_{SSA}	Variation between all the different ground pins(3)	-	50	
V_{ESD}	Electrostatic discharge voltage	Refer to 39.		

1. All power V_{DDX} (V_{DD}, V_{DDA}) and ground V_{SSX} (V_{SS}, V_{SSA}) pins must always be connected to the external power supply.
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$.
3. V_{SS} and V_{SSA} signals must be interconnected together with a short wire loop.

Table 5. Current characteristics

Symbol	Ratings	Max.(1)	Unit
I_{VDDX}	Total current into VDDX power lines(2)	100	mA
I_{VSSX}	Total current out of VSSX power lines(2)	100	
I_{IO}	Output current sunk by any I/Os and control pin	Ref. to 34	
	Output current source by any I/Os and control pin		
$I_{INJ(PIN)}$(3), (4)	Injected current on any pin	± 4	
$I_{INJ(TOT)}$(3), (4), (5)	Sum of injected currents	± 20	

1. Data based on characterization results, not tested in production.
2. All power V_{DDX} (V_{DD}, V_{DDA}) and ground V_{SSX} (V_{SS}, V_{SSA}) pins must always be connected to the external power supply.
3. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$.
4. Negative injection disturbs the analog performance of the device.
5. When several inputs are submitted to a current injection, the maximum $I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with the $I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

Table 6. Thermal characteristics

Symbol	Ratings	Max.	Unit
TSTG	Storage temperature range	-65 to 150	°C
T_J	Maximum junction temperature	150	

5.3 Operating conditions

The device must be used in operating conditions that respect the parameters listed in *Table 7*. In addition, a full account must be taken for all physical capacitor characteristics and tolerances.

Table 7. General operating conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD1}, V_{DDA1}	Operating voltages	-	3	-	5.5	V
V_{DD}, V_{DDA}	Nominal operating voltages	-	-	5	-	
V_{COUT}	Core digital power supply	-	-	1.8(1)	-	
	C_{VCOUT}: capacitance of external capacitor(2)	at 1 MHz	470	-	3300	nF
	ESR of external capacitor(1)		0.05	-	0.2	Ω
	ESL of external capacitor(1)		-	-	15	nH
Θ_{JA}(3)	FR4 multilayer PCB	TSSOP38	-	80	-	°C/W
T_A	Ambient temperature	Pd = 100 mW	-40	-	105	°C

1. Internal core power supply voltage.
2. Care should be taken when the capacitor is selected due to its tolerance, its dependency on temperature, DC bias and frequency.
3. To calculate P_{Dmax} (T_A), use the formula $P_{Dmax} = (T_{Jmax} - T_A)/\Theta_{JA}$.

Table 8. Operating conditions at power-up/power-down

Symbol	Parameter	Conditions	Min.(1)	Typ.	Max.(1)	Unit
t_{VDD}	VDD rise time rate		2 µs/V		1 s/V(2)	
	VDD fall time rate		2 µs/V		1 s/V(2)	
t_{TEMP}	Reset release delay	VDD rising		3		ms
V_{IT+}	Power-on reset threshold		2.65	2.8	2.98	V
V_{IT-}	Brownout reset threshold		2.58	2.73	2.88	
$V_{HYS(BOR)}$	Brownout reset hysteresis			70		mV

1. Guaranteed by design, not tested in production.
2. Power supply ramp must be monotone.

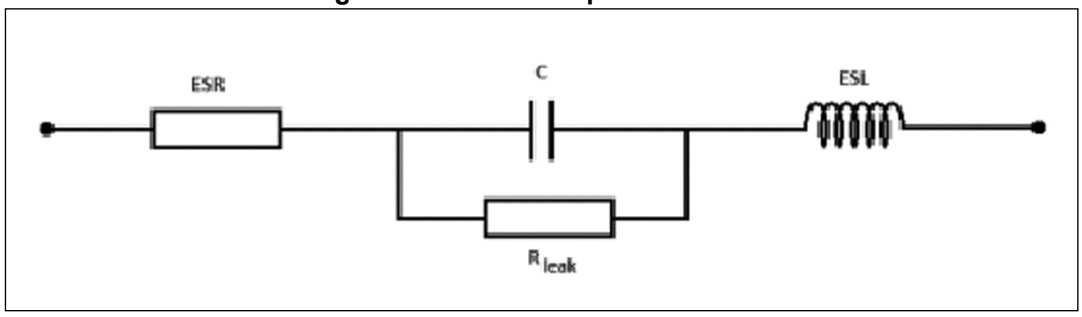
5.3.1 VOUT external capacitor

The stabilization of the main regulator is achieved by connecting an external capacitor C_{VCOUT}(a) to the VCOUT pin. C_{VCOUT} is specified in *Table 7: General operating conditions*.

Care should be taken to limit the series inductance to less than 15 nH.

a. ESR is the equivalent series resistance and ESL is the equivalent inductance.

Figure 24. External capacitor CVOUT



5.3.2 Supply current characteristics

The STNRGPF12 current consumption is declared based on, for example, an application where the application firmware is loaded and running.

Table 9. Supply current characteristics

Symbol	Parameter	Test condition	Min.	Typ.(1)	Max.(1)	Unit
V_{DD}/V_{DDA} SECTION: current consumption						
$IDD_{(RUN)}$	Total current consumption	V_{DD}/V_{DDA} = 5 V	-	28	34	mA

1. Test conditions:

   Data based on characterization results not tested in production.

   Temperature operating: T_A = 25 °C.

   Device in run mode.

5.3.3 Memory characteristics

Flash program and memory/data E^2PROM.

General conditions: T_A = -40 °C to 105 °C.

Table 10. Flash program memory/data E^2PROM

Symbol	Parameter	Conditions	Min.(1)	Typ.(1)	Max.(1)	Unit
t_{PROG}	Standard programming time (including erase) for byte/word/block (1 byte/4 bytes/128 bytes)	-	-	6	6.6	ms
	Fast programming time for 1 block (128 bytes)	-	-	3	3.3	
t_{ERASE}	Erase time for 1 block (128 bytes)	-	-	3	3.3	
N_{WE}	Erase/write cycles(2) (program memory)	T_A = 25 °C	10 K	-	-	Cycles
	Erase/write cycles(2) (data memory)	T_A = 85 °C	100 K	-	-	
		T_A = 105 °C	35 K	-	-	
t_{RET}	Data retention (program memory) after 10 K erase/write cycles at T_A = 25 °C	T_{RET} = 85 °C	15	-	-	Years
	Data retention (program memory) after 10 K erase/write cycles at T_A = 25 °C	T_{RET} = 105 °C	11	-	-	
	Data retention (data memory) after 100 K erase/write cycles at T_A = 85 °C	T_{RET} = 85 °C	15	-	-	
	Data retention (data memory) after 35 K erase/write cycles at T_A = 105 °C	T_{RET} = 105 °C	6	-	-	
I_{DDPRG}	Supply current during program and erase cycles	-40 ºC ≤ T_A ≤ 105 ºC	-	2	-	mA

1. Data based on characterization results, not tested in production.
2. The physical granularity of the memory is 4 bytes, so cycling is performed on 4 bytes even when a write/erase operation addresses a single byte.

5.3.4 Input/output specifications

The STNRGPF12 device includes three different I/O types:

- Normal I/Os (O or I);
- Fast I/O (OP);
- High speed I/O (CLOCK).

The STNRGPF12 I/Os are designed to withstand the current injection. For the negative injection current of 4 mA, the resulting leakage current in the adjacent input does not exceed 1 µA.

5.3.5 I/O port pin characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified. Unused input pins should not be left floating.

Table 11. Voltage DC characteristics

Symbol	Description	Min.(1)	Typ.	Max.(1)	Unit
V_{IL}	Input low voltage	-0.3	-	0.3 x V_{DD}	V
V_{IH}	Input high voltage(2)	0.7 x V_{DD}	-	V_{DD}	
V_{OL1}	Output low voltage at 5 V(3), (4)	-	-	0.5	
V_{OL3}	Output low voltage high sink at 5 V(2), (5)	-	-	0.6	
V_{OH1}	Output high voltage at 5 V(3), (4)	V_{DD} - 0.5	-	-	
V_{OH3}	Output high voltage high sink at 5 V(2), (5)	V_{DD} - 0.6	-	-	
H_{VS}	Hysteresis input voltage(6)	0.1 x V_{DD}	-	-	
R_{PU}	Pull-up resistor	30	45	60	kΩ

1. Data based on characterization result, not tested in production.
2. Input signals can't be exceeded V_{DDX} (V_{DDX} = V_{DD}, V_{DDA}).
3. The parameter applicable to signals on pins 14, 15, 20, 21, 22 and 23.
4. The parameter applicable to signals on pins 1, 4, 5, 8 16 and 19.
5. The parameter applicable to the signal on pin 2.
6. Applicable to pins 3, 6, 7, 17 and 18.

Table 12. Current DC characteristics

Symbol	Description	Min.	Typ.	Max.(1)	Unit
I_{OL1}	Standard output low level current at 5 V and V_{OL1}(2), (3)	-	-	3	mA
I_{OLhs1}	High sink output low level current at 5 V and V_{OL3}(2), (4)	-	-	7.75	
I_{OH1}	Standard output high level current at 5 V and V_{OH1}(2), (3)	-	-	3	
I_{OHhs1}	High sink output high level current at 5 V and V_{OH3}(2), (4)	-	-	7.75	
I_{LKg}	Input leakage current digital - analog $V_{SS} \le V_{IN} \le V_{DD}$(5)	-	-	± 1	µA
$I_{\_Inj}$	Injection current(6), (7)	-	-	± 4	mA
Σ_{I_Inj}	Total injection current sum of all I/O and control pins)(6)	-	-	± 20	

1. Data based on characterization result, not tested in production.
2. The parameter applicable to signals on pins 14, 15, 20, 21, 22 and 23.
3. The parameter applicable to signals on pins 1, 4, 5, 8 16 and 19.
4. The parameter applicable to the signal on pin 2.
5. Applicable to pins 3, 6, 7, 17 and 18.
6. Maximum value must never be exceeded.
7. Negative injection current on pins 31, 32, 33 and 34 must be avoided. It has impact on the measurement section.

5.3.6 Typical output level curves

This section shows the typical output voltage level curves measured on a single output pin for the three-pad family present in the STNRG device.

Normal I/Os

These pads are associated with the O type pins.

Figure 25. V_{OH} normal pin

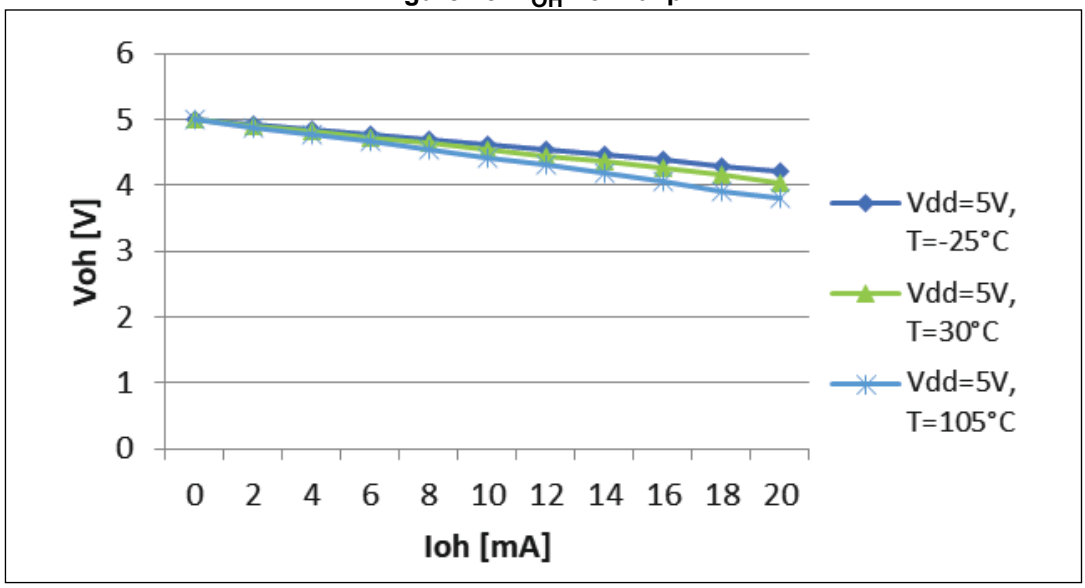
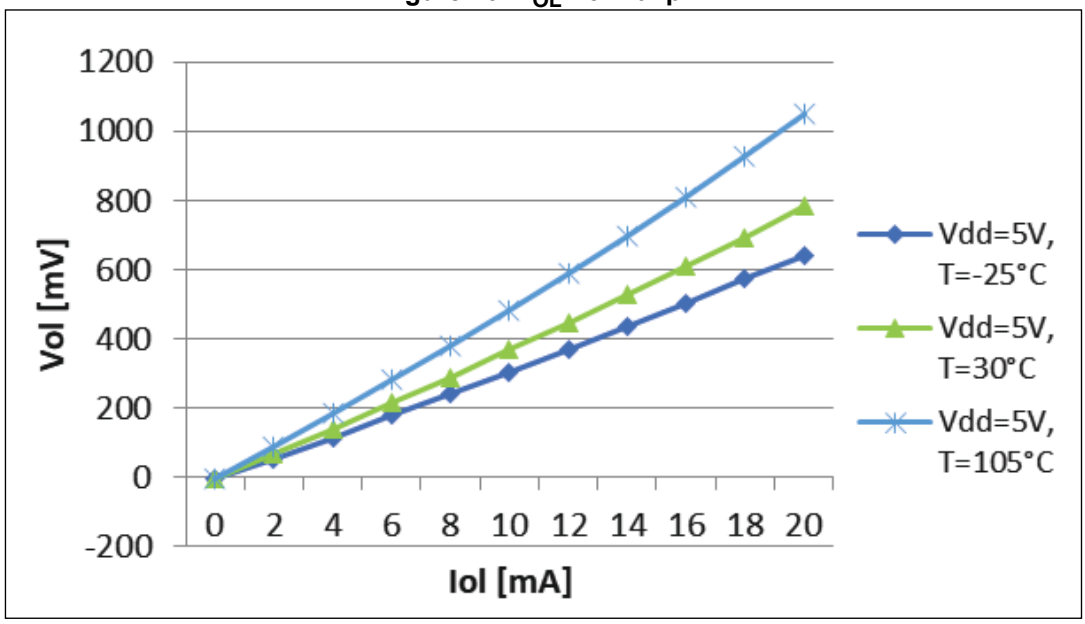


Figure 26. V_{OL} normal pin



Fast I/Os

These pads are associated with the OP type pins.

Figure 27. V_{OH} fast I/Os pins

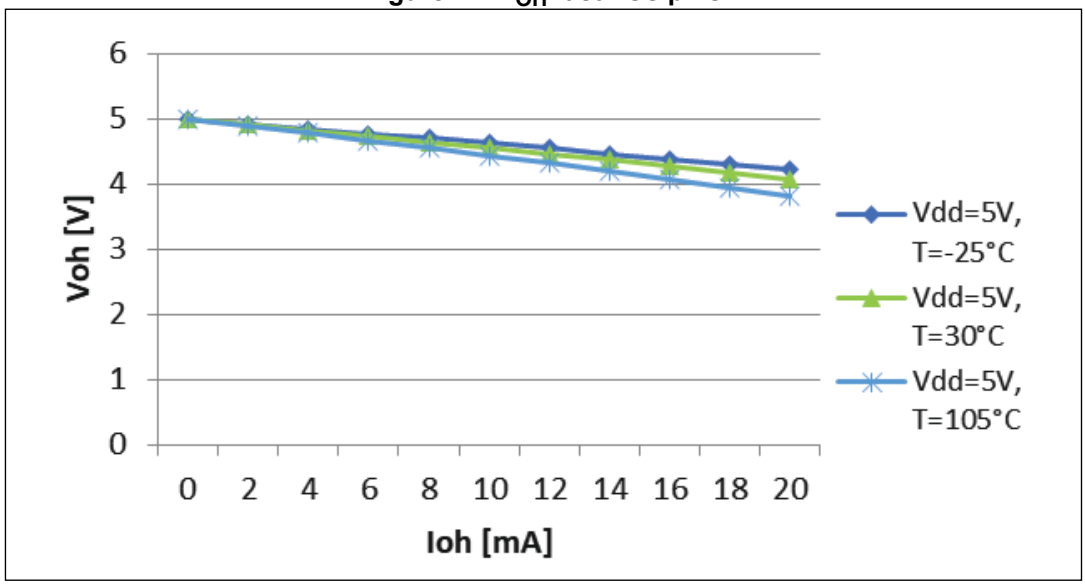
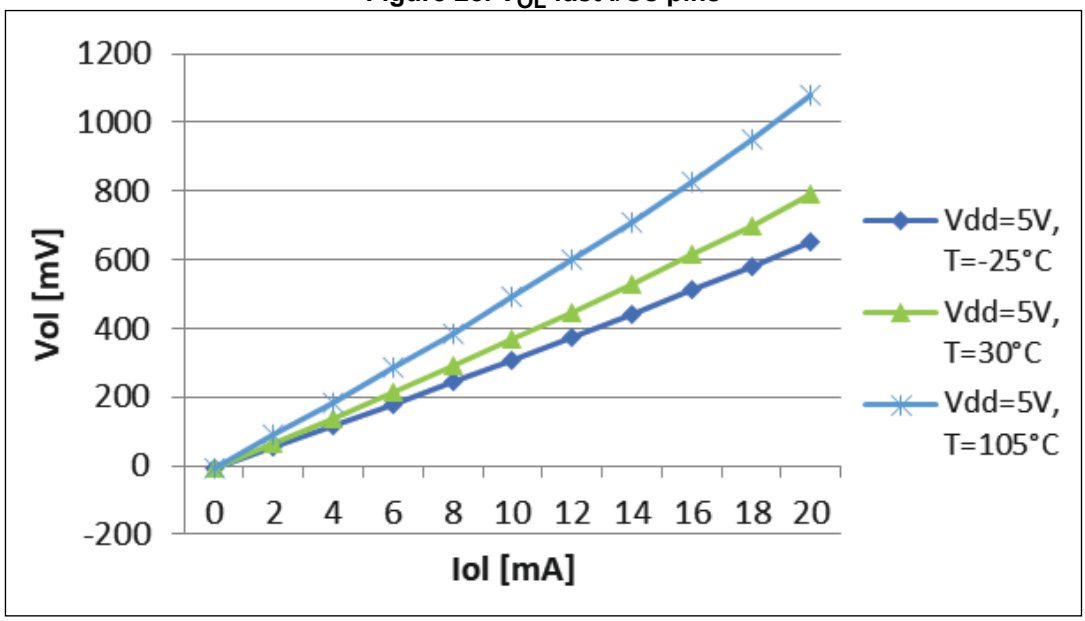


Figure 28. V_{OL} fast I/Os pins



Output CLOCK

This pad is associated with the OUTPUT CLOCK pin.

Figure 29. V_{OH} CLOCK pin

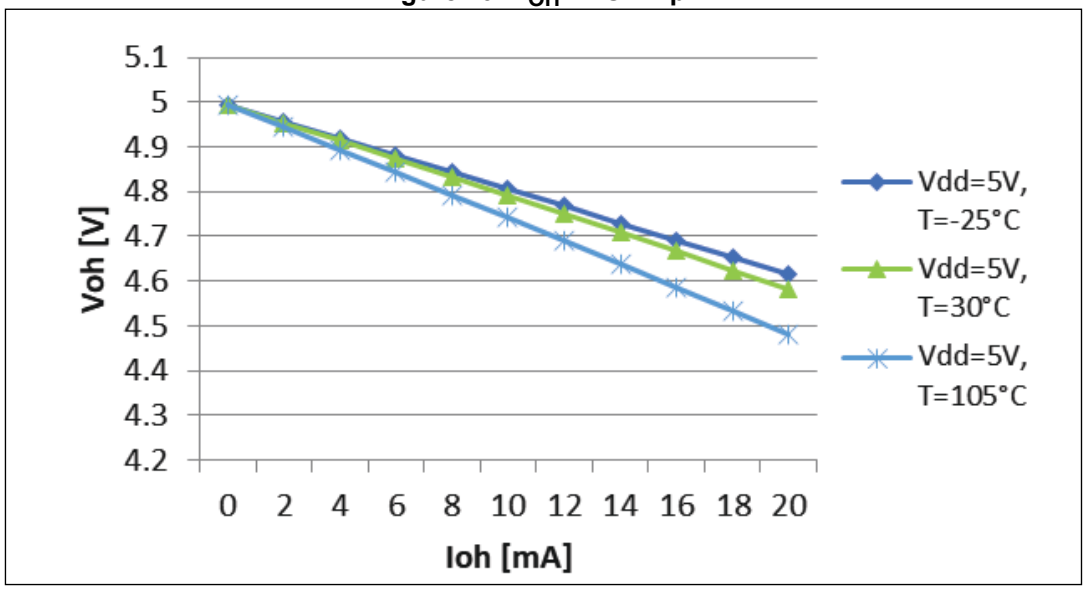
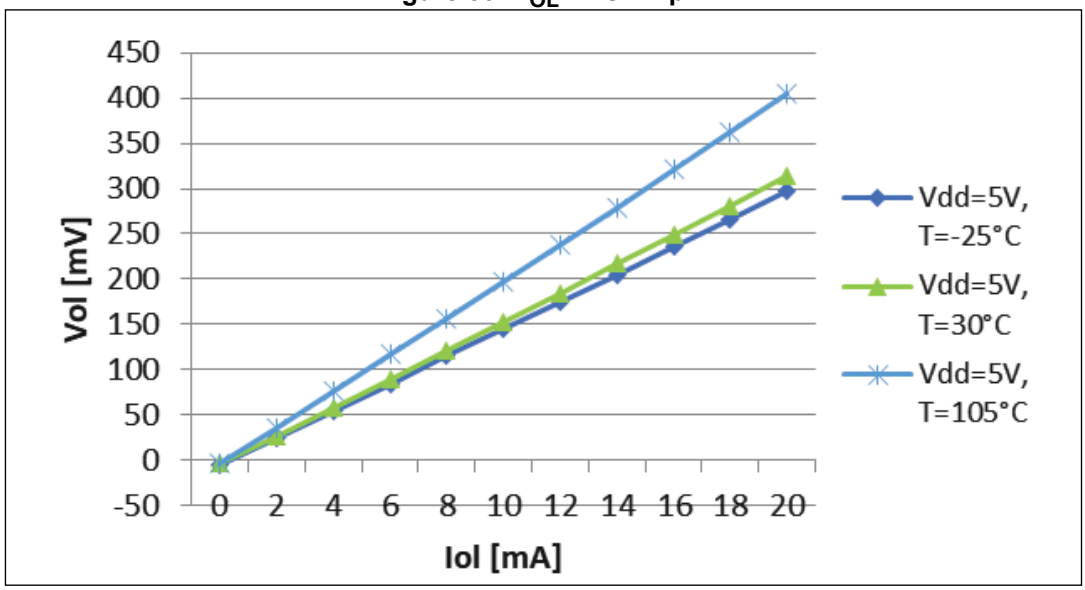


Figure 30. V_{OL} CLOCK pin



5.3.7 Reset pin characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 13. NRST pin characteristics

Symbol	Parameter	Conditions	Min.(1)	Typ.	Max.(1)	Unit
$V_{IL(NRST)}$	NRST input low level voltage(1)	-	-0.3	-	0.3 x V_{DD}	V
$V_{IH(NRST)}$	NRST input high level voltage(1)	-	0.7 x V_{DD}	-	V_{DD} + 0.3	
$V_{OL(NRST)}$	NRST output low level voltage(1)	I_{OL} = 2 mA	-	-	0.5	
$R_{PU(NRST)}$	NRST pull-up resistor(2)	-	30	40	60	kΩ
$t_{IFP(NRST)}$	NRST input filtered pulse(3)	-	-	-	75	ns
$t_{INFP(NRST)}$	NRST not input filtered pulse(3)	-	500	-	-	
$t_{OP(NRST)}$	NRST output filtered pulse(3)	-	15	-	-	µs

1. Data based on characterization results, not tested in production.
2. The RPU pull-up equivalent resistor is based on a resistive transistor.
3. Data guaranteed by design, not tested in production.

5.4 Analog input characteristics

5.4.1 Measurement section

Subject to general operating conditions for V_{DDA} and T_A unless otherwise specified.

It applies to the [MI] class.

Table 14. Measurement pin characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
RIN	Input impedance	-	1	-	-	M
VIN	Measurement range	-	0	-	1.25(1)	V
Vref	Measure reference voltage(2)	-	-	1.25	-	

1. Maximum input analog voltage cannot exceed V_{DDA}.
2. Reference voltage at T_A = 25 °C.

5.4.2 Analog section

In *Table 15* analog comparator characteristics are reported.

It applies to the [AI] class.

Table 15. Analog comparator characteristics

Symbol	Parameter	Conditions	Min.(1)	Typ.	Max(1)	Unit
V_{CPP01}	Comparator CP0,1 positive input voltage range	-40 ºC ≤ T_A ≤ 105 ºC	0	-	1.23(2)	V
V_{CPP23}	Comparator CP2,3 positive input voltage range	-40 ºC ≤ T_A ≤ 105 ºC	0	-	2(3)	V
V_{CPM23}	Comparator CP2,3 negative external input voltage range	-40 ºC ≤ T_A ≤ 105 ºC	0	-	2(3)	V
C_{IN}	Input capacitance	-	-	3	-	pF
V_{offset}	Comparator offset error	-	-	-	15	mV
t_{COMP}	Comparison delay time	-	-	-	50(4)	ns

1. Data based on characterization results, not tested in production.
2. Maximum analog input voltage for comparators CP0 and CP1.
3. Maximum analog input voltage for comparators CP2 and CP3.
4. The overdrive voltage is ± 50 mV.

5.5 EMC characteristics

5.5.1 Electrostatic discharge (ESD)

Electrostatic discharges (3 positive then 3 negative pulses separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device [3 parts * (n + 1) supply pin].

Table 16. ESD absolute maximum ratings(1)

Symbol	Ratings	Conditions	Maximum value	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = 25 °C, conforming to JEDEC/JESD22-A114E	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = 25 °C, conforming to ANSI/ESD STM 5.3.1 ESDA	500	
$V_{ESD(MM)}$	Electrostatic discharge voltage (machine model)	T_A = 25 °C, conforming to JEDEC/JESD-A115-A	200	

1. Data based on characterization results, not tested in production.

5.5.2 Static latch-up

Two complementary static tests are required on 10 parts to assess the latch-up performance.

A supply overvoltage (applied to each power supply pin) and a current injection (applied to each input, output and configurable I/O pin) are performed on each sample. This test conforms to the EIA/JESD78 IC latch-up standard.

Table 17. Electrical sensitivity

Symbol	Parameter	Conditions	Level
LU	Static latch-up class	T_A = 105 °C	A

6 Thermal data

The STNRG functionality cannot be guaranteed when the device, in operation, exceeds the maximum chip junction temperature (T_{Jmax}).

Equation 2

$$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta J_A)$$

Where:

T_{Amax} is the maximum ambient temperature in °C

Θ_{JA} is the package junction to ambient thermal resistance in °C/W

P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$)

P_{INTmax} is the product of I_{DD} and V_{DD}, expressed in watts. This is the maximum chip internal power.

$P_{I/Omax}$ represents the maximum power dissipation on output pins where:

$$P_{I/Omax} = (V_{OL} \times I_{OL}) + \Sigma [(V_{DD} - V_{OH}) \times I_{OH}],$$

taking into account the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the I/Os at the low and high level.

Table 18. Package thermal characteristics

Symbol	Parameter	Value	Unit
JA	TSSOP38 - thermal resistance junction to ambient(1)	80	°C/W

1. Thermal resistance is based on the JEDEC JESD51-2 with the 4-layer PCB in natural convection.

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

7.1 TSSOP38 package information

Figure 31. TSSOP38 package outline

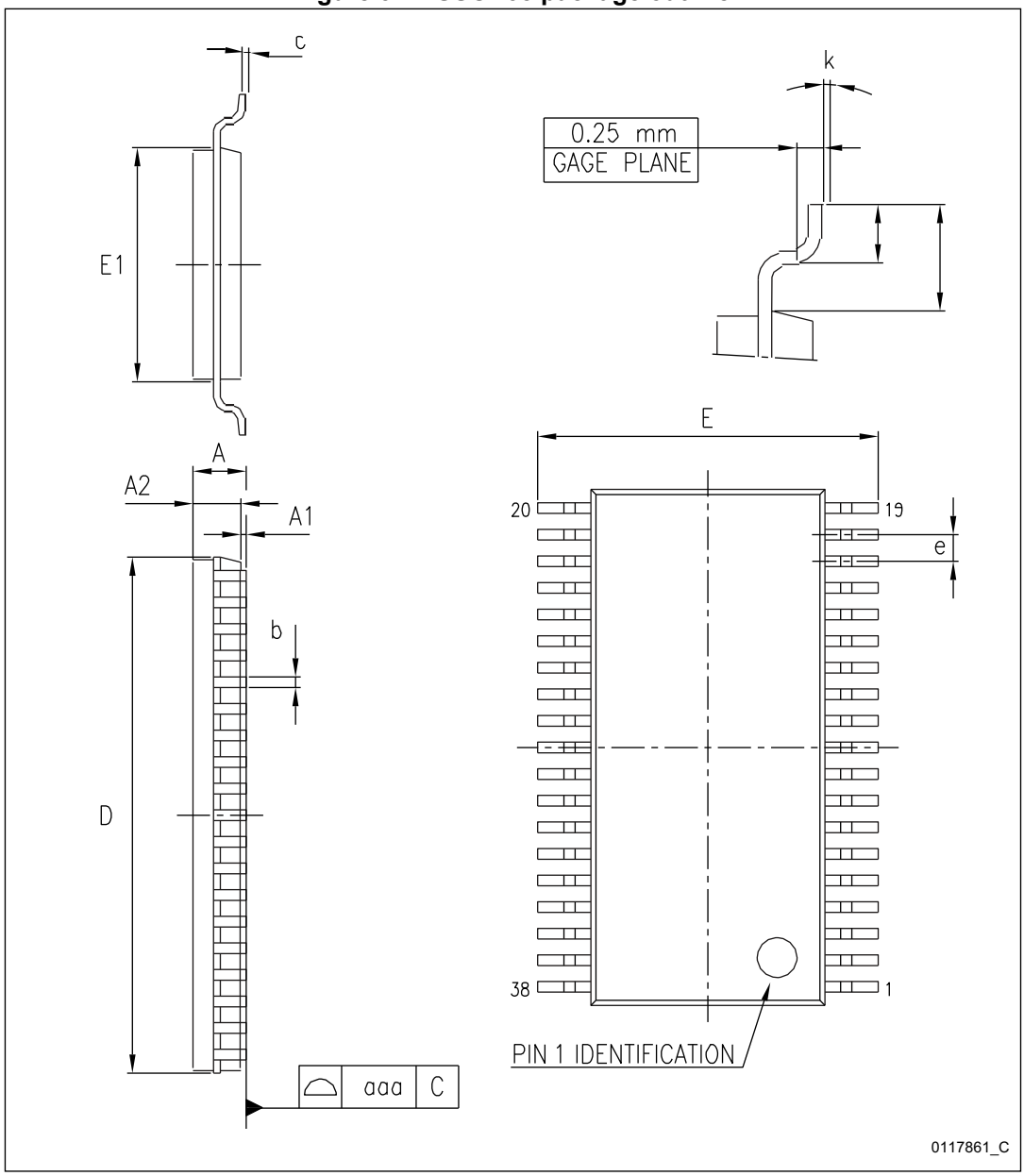


Table 19. TSSOP38 package mechanical data(1)

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	1.00	1.05
b	0.17	-	0.27
c	0.09	-	0.20
D(2)	9.60	9.70	9.80
E	6.20	6.40	6.60
E1(2)	4.30	4.40	4.50
e	-	0.50	-
L	0.45	0.60	0.75
L1	-	1.00	-
k	0	-	8
aaa	-	-	0.10

1. “TSSOP” stands for “Thin Shrink Small Outline Package”.
2. “Dimensions “D” and “E1”do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.

8 STNRGPF12 development tools

The development tools for the STNRGPF12 are provided by:

- **eDesign Suite**
  This tool uses a graphical user interface to guide customers step-by-step to implementation of a solution in accordance with their specifications.
  The tool gives users the ability to navigate through an interactive and hierarchical schematic, providing additional information like Bode diagrams for both the current and the voltage loop, power loss calculation, bill of material, and easy shortcuts for datasheets and product folder web pages.
  The final output of this process is a complete design, with a binary file that contains the optimized firmware for that specific application, which can be uploaded to the STNRGPF12 device using the UART serial communication port.
- **STNRG LOADER**
  This tool permits the user to download the binary code from the eDesign Suite.

9 Ordering information

Table 20. Ordering information

Order codes	Package	Packaging
STNRGPF12	TSSOP38	Tube
STNRGPF12TR		Tape and reel

10 Revision history

Table 21. Document history

Date	Revision	Changes
04-May-2019	1	Initial release.