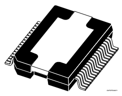
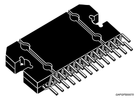
TDA7577BLV

2 x 75 W dual-bridge power amplifier with I^2C complete diagnostics and "start-stop" profile (6 V operation)

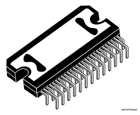
Datasheet - production data



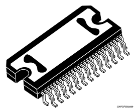
PowerSO36 (slug-up)



Flexiwatt27 (vertical)



Flexiwatt27 (horizontal)



Flexiwatt27 (SMD)

Features

- MOSFET (DMOS) output power stage
- High-efficiency (class SB)
- Single-channel 1 Ω driving capability
  - 84 W undistorted power
- High output power capability 2 x 28 W / 4 Ω @ 14.4 V, 1 kHz, 10 % THD
- Max. output power 2 x 75 W / 2 Ω, 1 x 150 W / 1 Ω
- Full I^2C bus driving with 4 addresses
- Low voltage (6 V) operation (i.e. 'start-stop')
- Gain 16/26 dB
- Full digital diagnostic (AC and DC loads)
- Legacy mode (operation without I^2C)
- Differential inputs
- Fault detection through integrated diagnostics
- DC offset detection
- Two independent short circuit protections
- Diagnostic on clipping detector with selectable threshold (2 % / 10 %)
- Clipping detector pin
- ST-BY and MUTE pins
- ESD protection
- Very robust against misconnections

Description

The TDA7577BLV is a new MOSFET dual bridge amplifier specially intended for car radio applications. Thanks to the DMOS output stage the TDA7577BLV has a very low distortion allowing a clear powerful sound, together with high output power capability.

It is a very flexible device capable to support the most demanding specifications in terms of power dissipation and battery transitions: its superior efficiency performance, coming from the internal exclusive structure, can reduce the dissipated output power up to the 50 % (when compared to conventional class AB solutions). Moreover it is compliant to the recent OEM specifications thanks to the capability to work down to 6 V ('start-stop' compatibility).

This device is also equipped with a full diagnostic array that communicates the status of each speaker through the I^2C bus. TDA7577BLV can also drive 1 Ω loads (with parallel connection of the outputs).

It is possible also to exclude the I^2C bus interface, controlling the device by means of the usual ST-BY and MUTE pins.

Table 1. Device summary

Order code	Package	Packing
TDA7577BLV	Flexiwatt 27 (vertical)	Tube
TDA7577BLVPD	PowerSO36	Tube
TDA7577BLVPDTR	PowerSO36	Tape and reel
TDA7577BLVH	Flexiwatt 27 (horizontal)	Tube
TDA7577BLVSM	Flexiwatt 27 (SMD)	Tube

Contents

List of tables

List of figures

1 Block and pins diagrams

Figure 1. Block diagram

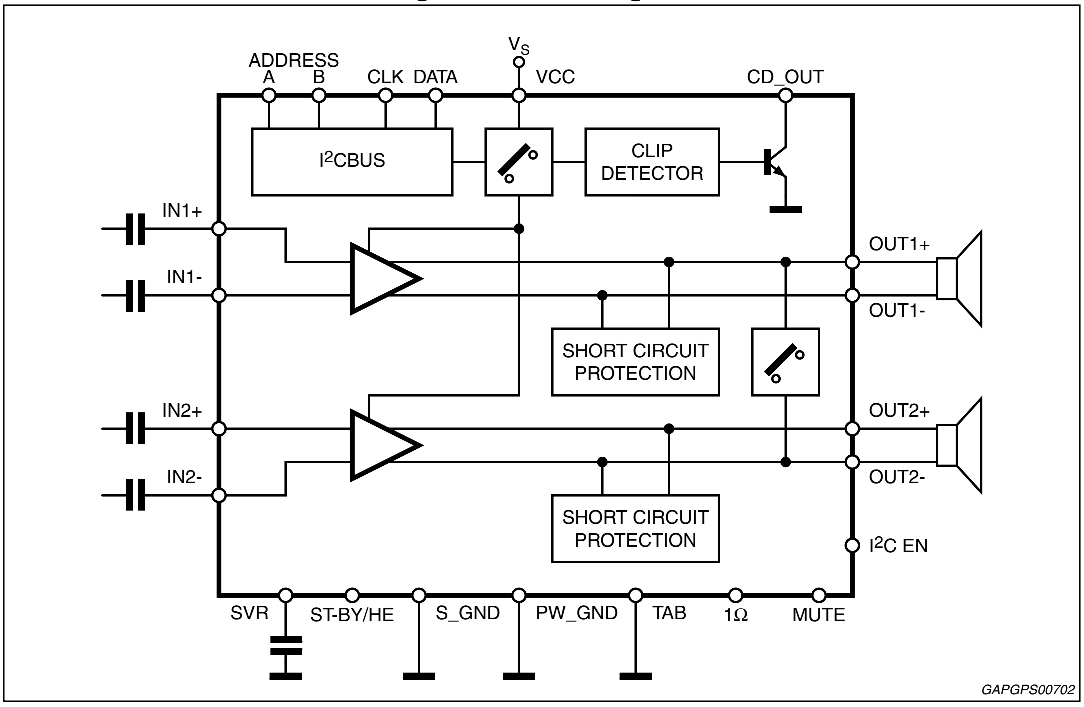
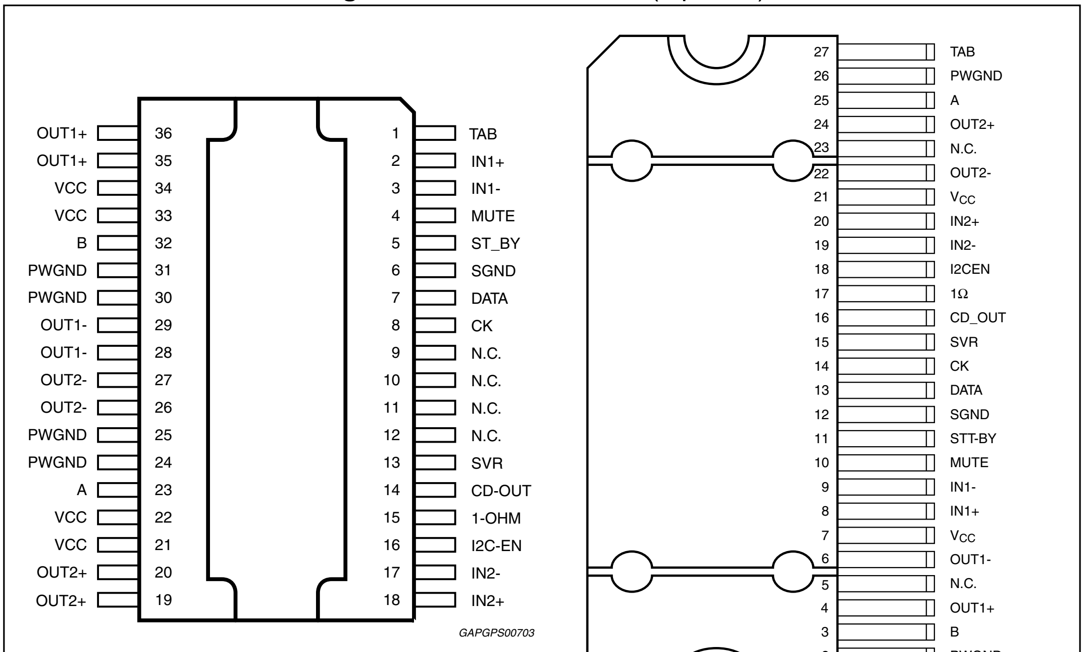


Figure 2. Pin connections (top view)

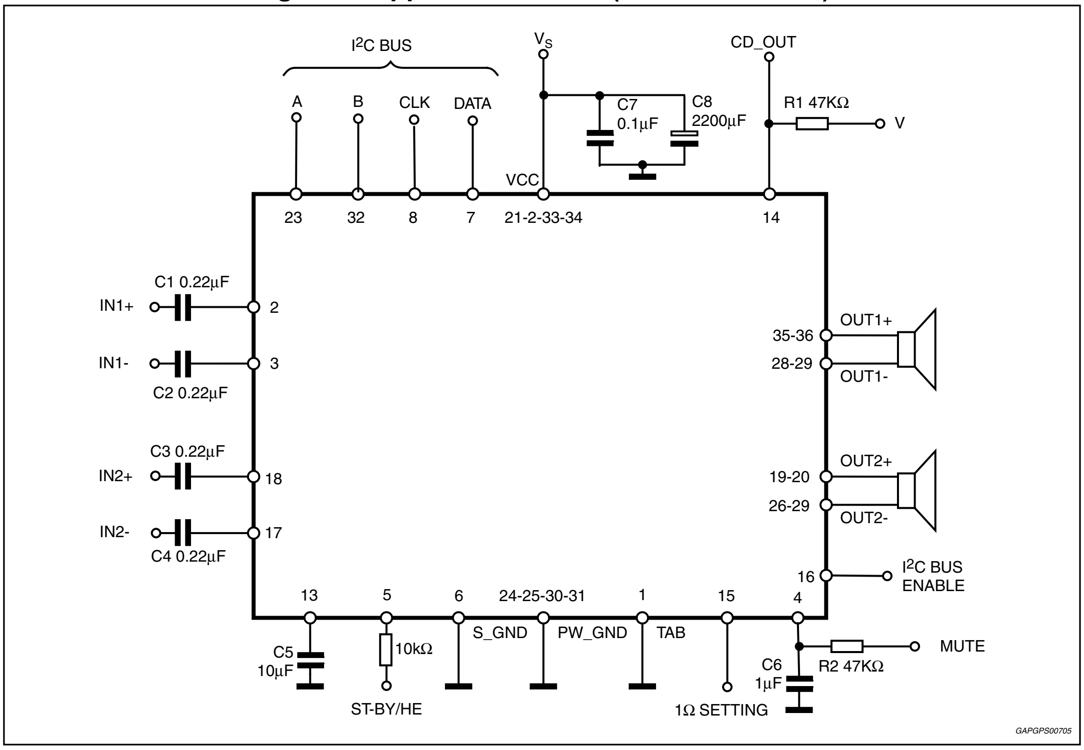


PowerSO36 (slug-up)

Flexiwatt 27 (vertical)

2 Application circuit

Figure 3. Application circuit (TDA7577BLVPD)



3 Electrical specifications

3.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{op}	Operating supply voltage	18	V
V_S	DC supply voltage	28	V
V_{peak}	Peak supply voltage (for t = 50 ms)	50	V
V_{CK}, V_{DATA}	I2C CK and DATA pin voltage	-0.3 to 6	V
GND_{max}	Ground pin voltage	-0.3 to 0.3	V
$V_{st\text{-}by}$	Standby pin voltage	-0.3 to V_{op}	V
V_{CP}	Clip detector voltage	-0.3 to V_{op}	V
$V_{in\ max}$	Input max voltage	-0.3 to V_{op}	V
I_O	Output peak current (not repetitive t = 100 ms)	8	A
I_O	Output peak current (repetitive f > 10 Hz)	6	A
P_{tot}	Power dissipation T_{case} = 70 °C (1)	86	W
T_{stg}, T_j	Storage and junction temperature (2)	-55 to 150	°C
T_{amb}	Operative temperature range	-40 to 105	°C

1. This is maximum theoretical value; for power dissipation in real application conditions, please refer to curves reported in *Section 3.4: Electrical characteristics typical curves*.
2. A suitable dissipation system should be used to keep T_j inside the specified limits.

3.2 Thermal data

Table 3. Thermal data

Symbol	Parameter		PowerSO36	Flexiwatt 27	Unit
$R_{th\ j\text{-}case}$	Thermal resistance junction-to-case	Max	1	1	°C/W

3.3 Electrical characteristics

Refer to the test circuit, V_S = 14.4 V; R_L = 4 Ω; f = 1 kHz; G_V = 26 dB; T_{amb} = 25 °C; unless otherwise specified.
Tested at T_{amb} = 25 °C and T_{hot} = 105 °C; functionality guaranteed for T_j = -40 °C to 150 °C.

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
General characteristics						
V_S	Supply voltage range	-	6	-	18	V
		R_L = 2 Ω	6	-	16	V

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_d	Total quiescent drain current	-	-	140	200	mA
R_{IN}	Input impedance	-	100	115	140	kΩ
V_{AM}	Min supply mute threshold	Start-stop IB1(D7) = 0 (default)	5	-	6	V
		No start-stop IB1(D7) = 1	7	-	8	
V_{OS}	Offset voltage	Mute & play, standard bridge	-65	-	65	mV
I_{SB}	Standby current consumption	$V_{st\text{-}by}$ = 0 V	-	1	5	µA
PSRR	Power supply rejection ratio	f = 100 Hz to 10 kHz; V_r = 1 Vpk; R_g = 600 Ω	60	75	-	dB
T_{ON}	Turn on delay	D2 (IB1) 0 to 1	-	30	50	ms
T_{OFF}	Turn off delay	D2 (IB1) 1 to 0	-	30	50	ms
V_{MC}	Max. common mode input level	f = 1 kHz	-	-	1	Vrms
SR	Slew rate	-	2	4.5	-	V/µs
Audio performances						
Po	Output power	Max. power(1) THD = 10 % THD = 1 %	40 25 -	45 28 22	-	W
		R_L = 2 Ω; THD 10 % R_L = 2 Ω; THD 1 % R_L = 2 Ω; Max. power(1)	45 - 70	50 40 78	-	W
		Single channel configuration (1 Ω pin >2.5 V); R_L = 1 Ω; THD 3 % Max. power(1)	80 140	85 155	-	W
		Max. power(1), V_s = 6 V	-	6	-	W
		Max. power(1), V_s = 6 V, R_L = 1 Ω;	-	25	-	W
THD	Total harmonic distortion	P_O = 1-12W; STD MODE HE MODE; P_O = 1-2 W HE MODE; P_O = 4-8 W	-	0.04 0.03 0.1	0.1 0.1 -	%
		P_O = 1-12 W, f = 10 kHz, STD MODE	-	0.3	0.5	%
		R_L = 2 Ω; HE MODE; Po = 3 W	-	0.05	0.5	%
		Single channel configuration (1Ω pin > 2.5 V); R_L = 1 Ω; P_O = 4-30 W	-	0.085	0.15	%
C_T	Cross talk	R_g = 600 Ω; P_O = 1 W	75	90	-	dB
G_{V1}	Voltage gain 1 (default)	-	25	26	27	dB
ΔG_{V1}	Voltage gain match 1	-	-1	-	1	dB
G_{V2}	Voltage gain 2	-	15	16	17	dB
ΔG_{V2}	Voltage gain match 2	-	-1	-	1	dB

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
E_{IN1}	Output noise voltage gain 1	R_g = 600 Ω; Gv = 26 dB filter 20 to 22 kHz	-	45	60	µV
E_{IN2}	Output noise voltage gain 2	R_g = 600 Ω; Gv = 16 dB filter 20 to 22 kHz	-	20	30	µV
BW	Power bandwidth	(-3 dB)	100	-	-	kHz
CMRR	Input CMRR	V_{CM} = 1 Vpk-pk; R_g = 0 Ω	55	70	-	dB
$\|V_{OS}\|$	Mute on/off output offset voltage	ITU R-ARM weighted (see *Figure 22*); High gain	-	3	12	mV
	Standby on/off output offset voltage		-	1	7.5	mV
$\|V_{OS}\|$	Mute on/off output offset voltage	ITU R-ARM weighted (see *Figure 22*); Low gain	-	2	7.5	mV
	Standby on/off output offset voltage		-	0.5	7.5	mV
Clip detector						
I_{CDH}	Clip pin high leakage current	CD off, 0 V < V_{CD} < 5.5 V	-5	-	5	µA
I_{CDL}	Clip pin low sink current	CD on; V_{CD} < 300 mV	1	-	-	mA
CD	Clip detect THD level	D0 (IB1) = 0	1	2	3	%
		D0 (IB1) = 1	5	10	15	%
Control pin characteristics						
V_{OFF}	ST-BY pin for standby [(2)]	-	0	-	1.2	V
V_{SB}	ST-BY pin for standard bridge	-	2.6	-	5	V
V_{HE}	ST-BY pin for Hi-eff	-	7	-	18	V
$I_{O\ (ST\text{-}BY)}$	ST-BY pin current	1.2 V < $V_{st\text{-}by/HE}$ < 18 V	-	150	200	µA
	ST-BY pin current	V_{stby} < 1.2 V	-	1	5	µA
V_m	Mute pin voltage for mute mode	-	0	-	1	V
	Mute pin voltage for play mode	-	2.6	-	18	V
I_m	Mute pin current (st_by)	V_{mute} = 0 V, $V_{st\text{-}by}$ < 1.2 V	-5	-	5	µA
	Mute pin current (operative)	0 V < V_{mute} < 18 V, $V_{st\text{-}by}$ > 2.6 V	-	60	100	µA
V_{I2C}	I^2C pin voltage for I^2C disabled	-	0	-	1.5	V
	I^2C pin voltage for I^2C enabled	-	2.5	-	18	V
I_{I2C}	I^2C pin current (standby)	0 V < I^2C EN < 18 V, V_{stby} < 1.2 V	-5	-	5	µA
	I^2C pin current (operative)	I^2C EN <18 V, $V_{st\text{-}by}$>2.6 V	7	13	18	µA
$V_{1\Omega}$	1Ω pin voltage for 2ch mode	-	0	-	1.5	V
	1Ω pin voltage for 1 Ω mode	-	2.5	-	18	V
$I_{1\Omega}$	1Ω pin current (standby)	0 V < 1 Ω <18 V, $V_{s\text{-}tby}$ < 1.2 V	-5	-	5	µA
	1Ω pin current (operative)	1 Ω < 18 V, $V_{s\text{-}tby}$ > 2.6 V	7	13	18	µA
La	A pin voltage	Low logic level	0	-	1.5	V
Ha		High logic level	2.5	-	18	V

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Ia	A pin current (ST-BY)	0 V < A < 18 V, $V_{st\text{-}by}$ < 1.2 V	-5	-	5	µA
	A pin current (operative)	A < 18 V, $V_{st\text{-}by}$ > 2.6 V	7	13	18	µA
Lb	B pin voltage	Low logic level	0	-	1.5	V
Hb		High logic level	2.5	-	18	V
Ib	B pin current (ST-BY)	0V < B < 18 V, V_{stby} < 1.2 V	-5	-	5	µA
	B pin current (operative)	B < 18 V, $V_{st\text{-}by}$ > 2.6 V	7	13	18	µA
A_{SB}	Standby attenuation	-	90	100	-	dB
A_M	Mute attenuation	-	80	100	-	dB
Turn on diagnostics (Power amplifier mode)						
Pgnd	Short to GND det. (below this limit, the Output is considered in Short Circuit to GND)	Power amplifier in standby condition	-	-	1.2	V
Pvs	Short to Vs det. (above this limit, the Output is considered in Short Circuit to VS)	-	V_s - 0.9	-	-	V
Pnop	Normal operation thresholds.(Within these limits, the Output is considered without faults).	-	1.8	-	V_s - 1.5	V
Lsc	Shorted load det.	-	-	-	0.5	Ω
Lop	Open load det.	-	85	-		Ω
Lnop	Normal load det.	-	1.5	-	45	Ω
Turn on diagnostics (Line driver mode)						
Pgnd	Short to GND det. (below this limit, the Output is considered in Short Circuit to GND)	Power amplifier in standby	-	-	1.2	V
Pvs	Short to Vs det. (above this limit, the Output is considered in Short Circuit to VS)		V_s - 0.9	-	-	V
Pnop	Normal operation thresholds.(Within these limits, the Output is considered without faults).		1.8	-	V_s - 1.5	V
Lsc	Shorted load det.		-	-	1.5	Ω
Lop	Open load det.		330	-	-	Ω
Lnop	Normal load det.		4.5	-	180	Ω
Permanent diagnostics (Power amplifier mode or line driver mode)						
Pgnd	Short to GND det. (below this limit, the Output is considered in Short Circuit to GND)	Power amplifier in Mute or Play condition, one or more short circuits protection activated	-	-	1.2	V

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Pvs	Short to Vs det. (above this limit, the Output is considered in Short Circuit to VS)	-	V_S - 0.9	-	-	V
Pnop	Normal operation thresholds.(Within these limits, the Output is considered without faults).	-	1.8	-	V_S - 1.5	V
Lsc	Shorted load det.	Pow. amp. mode	-	-	0.5	Ω
		Line driver mode	-	-	1.5	Ω
V_O	Offset detection	Power amplifier in play condition AC input signals = 0	±1.5	±2	±2.5	V
I_{NLH}	Normal load current detection	V_O < (V_S - 5)pk IB2 (D0) = 0	500	-	-	mA
I_{NLL}	Normal load current detection	V_O < (V_S - 5)pk IB2 (D0) = 1	250	-	-	mA
I_{OLH}	Open load current detection	V_O < (V_S - 5)pk IB2 (D0) = 0	-	-	250	mA
I_{OLL}	Open load current detection	V_O < (V_S - 5)pk IB2 (D0) =1	-	-	125	mA
I^2C bus interface						
f_{SCL}	Clock frequency	-	-	-	400	kHz
V_{IL}	Input low voltage	-	-	-	1.5	V
V_{IH}	Input high voltage	-	2.3	-	-	V

1. Saturated square wave output.
2. ST-BY pin high enables the I^2C bus; ST-BY pin low enables ST-BY condition: detailed pin levels description is contained in paragraph 'I^2C habilitation settings' .

3.4 Electrical characteristics typical curves

Figure 4. Quiescent drain current vs. supply voltage

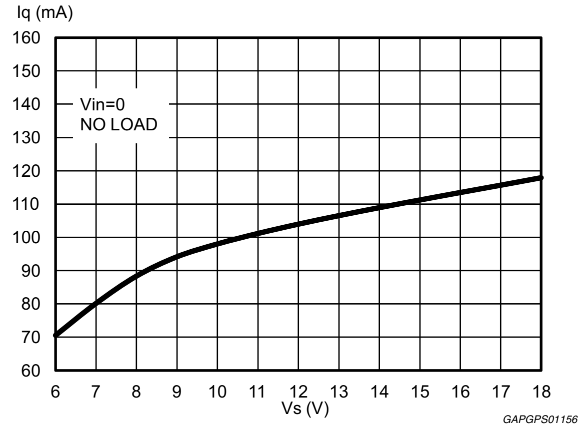


Figure 5. Output power vs. supply voltage (4 Ω)

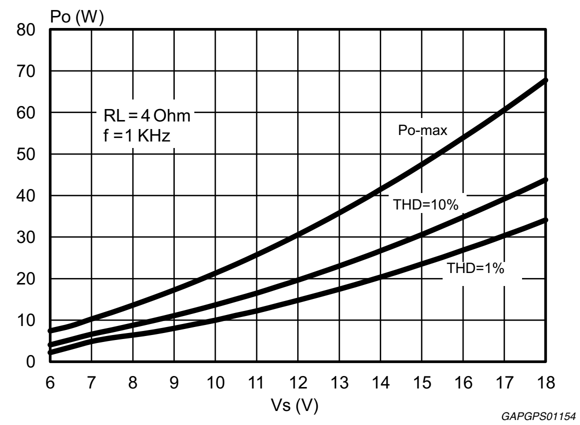


Figure 6. Output power vs. supply voltage (2 Ω)

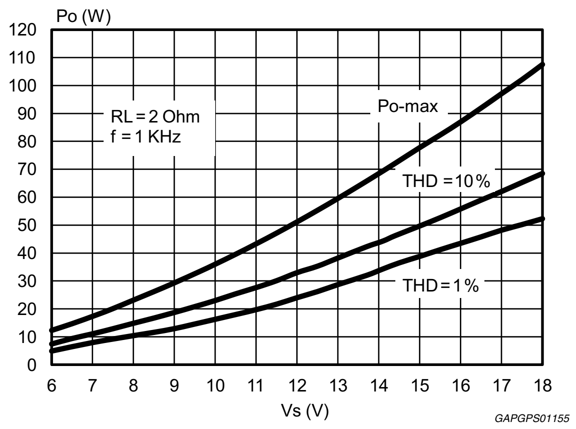


Figure 7. Output power vs. supply voltage (1 Ω)

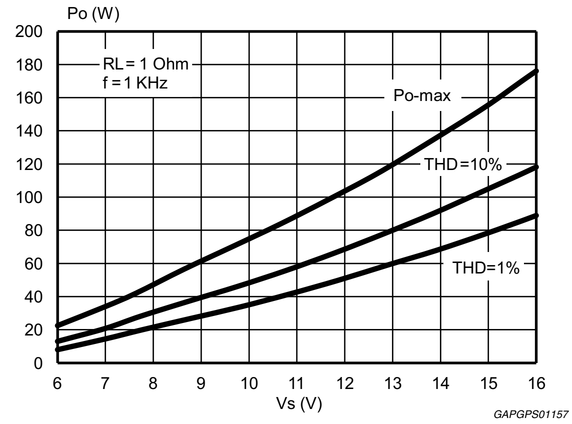


Figure 8. Distortion vs. output power (4 Ω, STD mode)

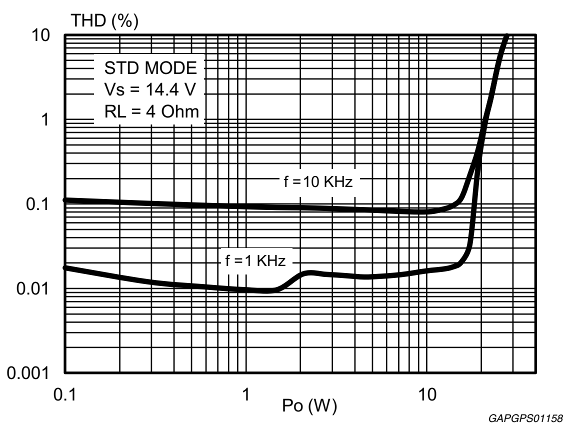


Figure 9. Distortion vs. output power (2 Ω, STD mode)

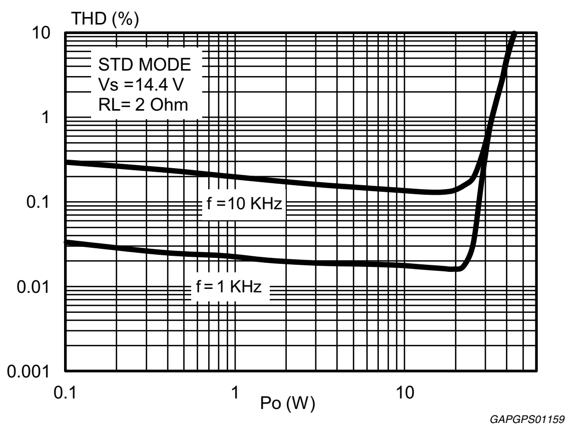


Figure 10. Distortion vs. output power (2 Ω, HI-EFF mode)

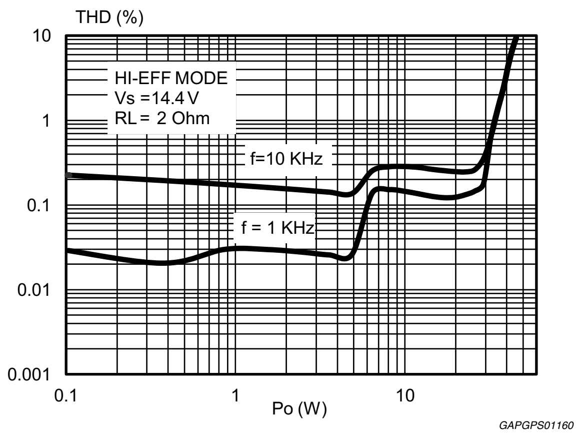


Figure 11. Distortion vs. output power (1 Ω, STD mode)

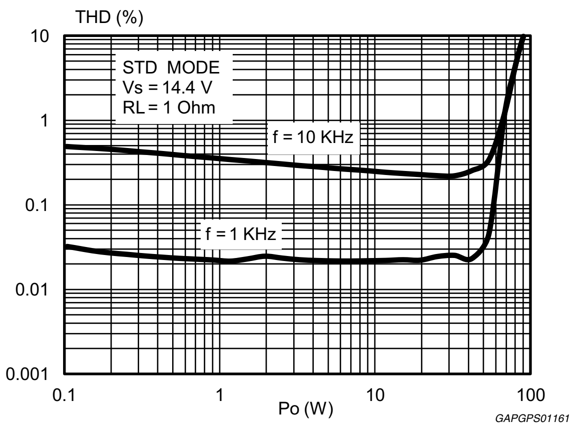


Figure 12. Distortion vs. frequency (4 Ω load)

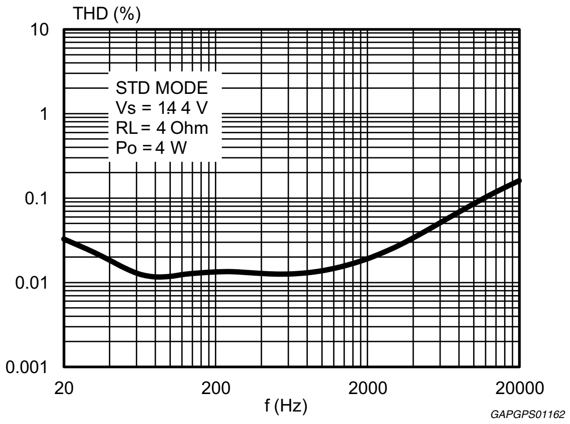


Figure 13. Distortion vs. frequency (2 Ω load)

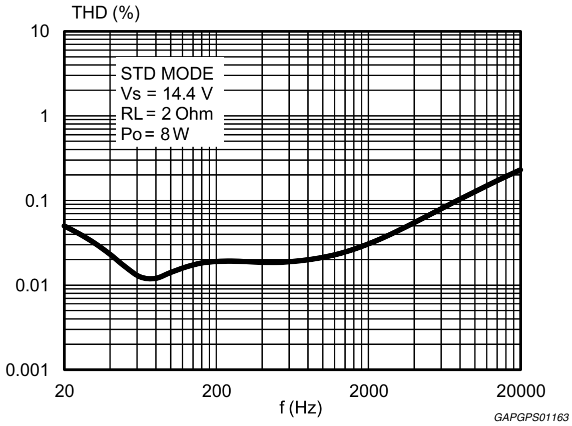


Figure 14. Distortion vs. frequency (1 Ω load)

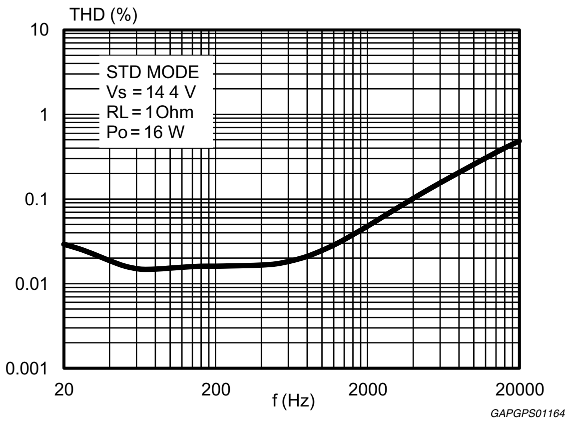


Figure 15. Output attenuation vs. supply voltage

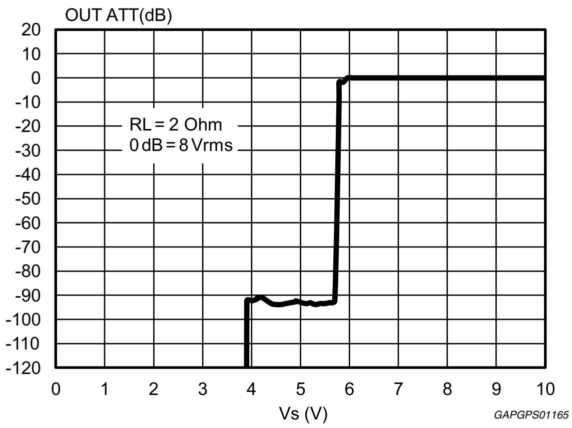


Figure 16. CMRR vs. frequency

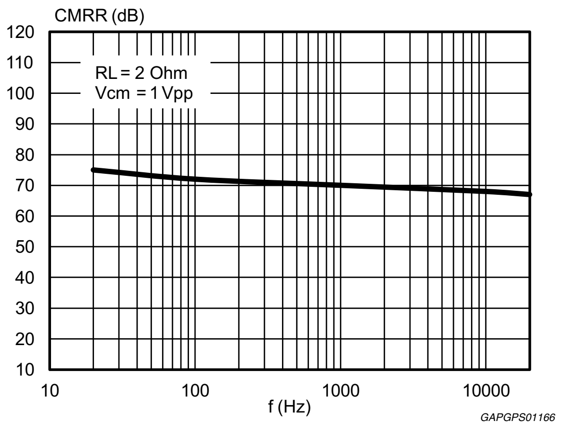


Figure 17. Cross talk vs frequency

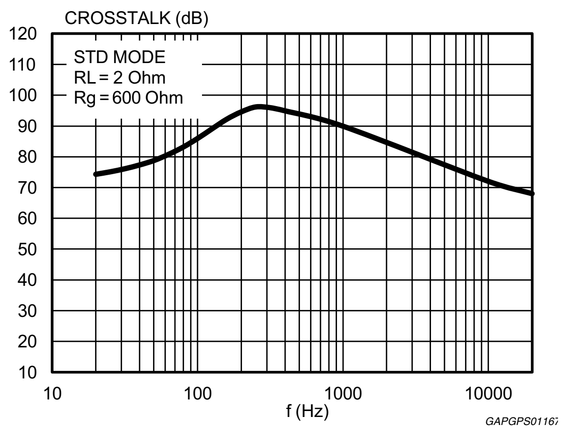


Figure 18. Power dissipation vs. average Po (2 Ω, STD mode, sine wave)

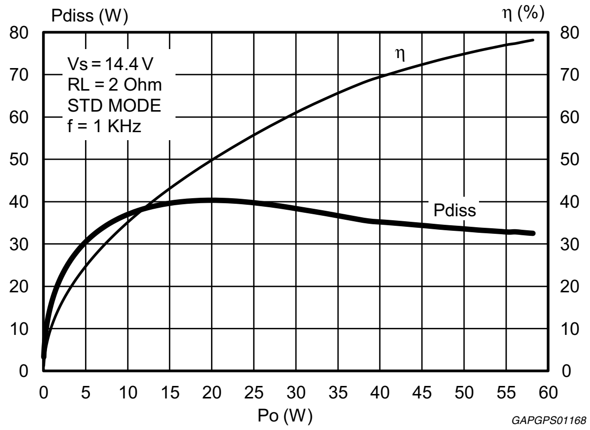


Figure 19. Power dissipation vs. Po (2 Ω, STD mode, audio program simulation)

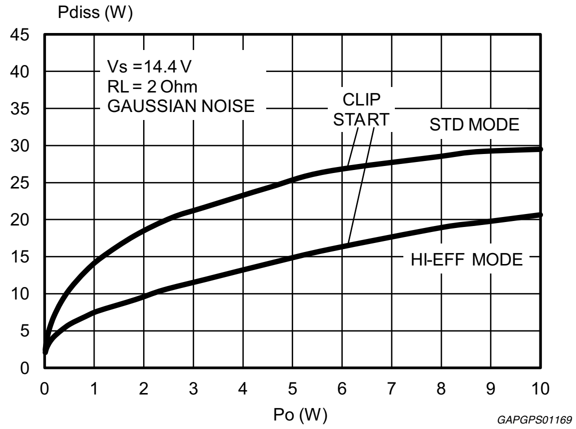


Figure 20. Power dissipation vs. average Po (2Ω, HI-EFF mode)

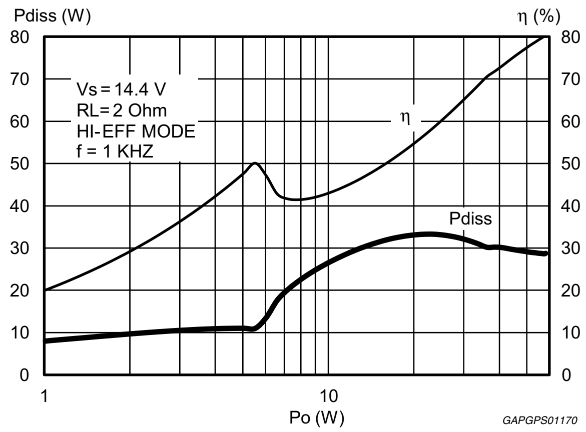


Figure 21. Power dissipation vs. Po (1 Ω, STD mode, audio program simulation)

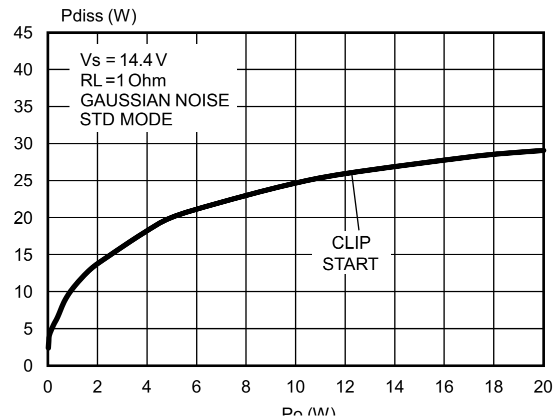
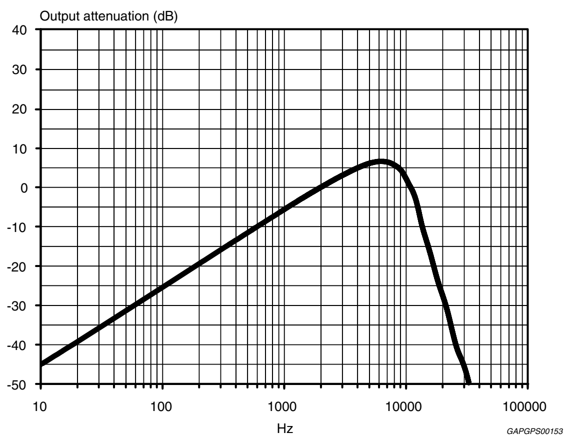


Figure 22. ITU R-ARM frequency response, weighting filter for transient pop



4 Diagnostics functional description

4.1 Turn-on diagnostic

It is strongly recommended to activate this function at the turn-on (standby out) through I^2C bus request. Detectable output faults are:

- SHORT TO GND
- SHORT TO Vs
- SHORT ACROSS THE SPEAKER
- OPEN SPEAKER

To verify if any of the above misconnections is in place, a subsonic (inaudible) current pulse (*Figure 23*) is internally generated, sent through the speaker(s) and sunk back. The Turn-on diagnostic status is internally stored until a successive diagnostic pulse is requested (after a I^2C reading).

If the "standby out" and "diag. enable" commands are both given through a single programming step, the pulse takes place first (during the pulse power stages stay off, showing high impedance at the outputs).

Afterwards, when the Amplifier is biased, the permanent diagnostic takes place. The previous turn-on state is kept until a short appears at the outputs.

Figure 23. Turn-on diagnostic: working principle

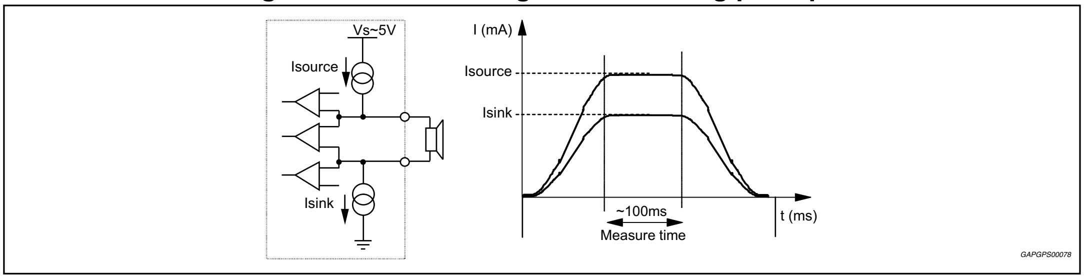


Fig. *Figure 24* and *Figure 25* show SVR and OUTPUT waveforms at the turn-on (standby out) with and without turn-on diagnostic.

Figure 24. SVR and output behavior - case 1: without turn-on diagnostic

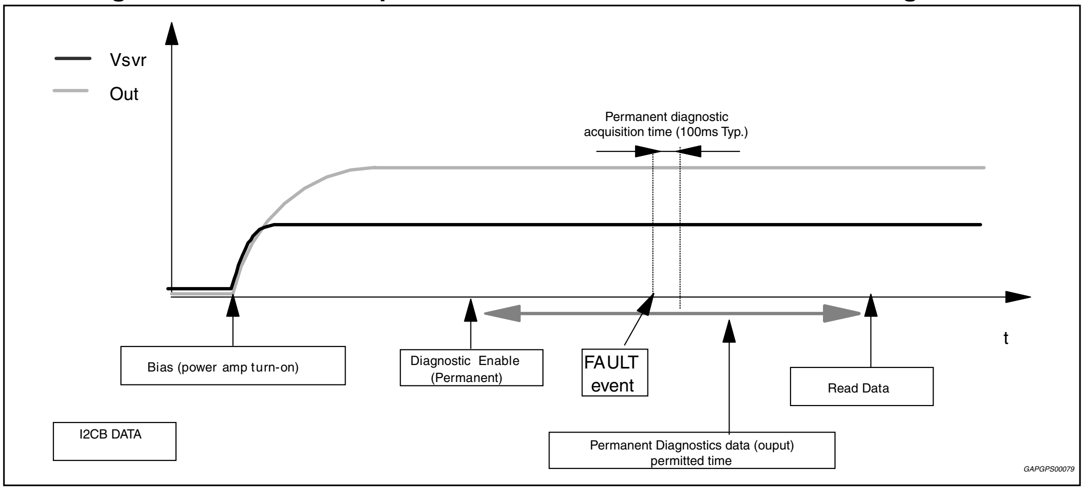
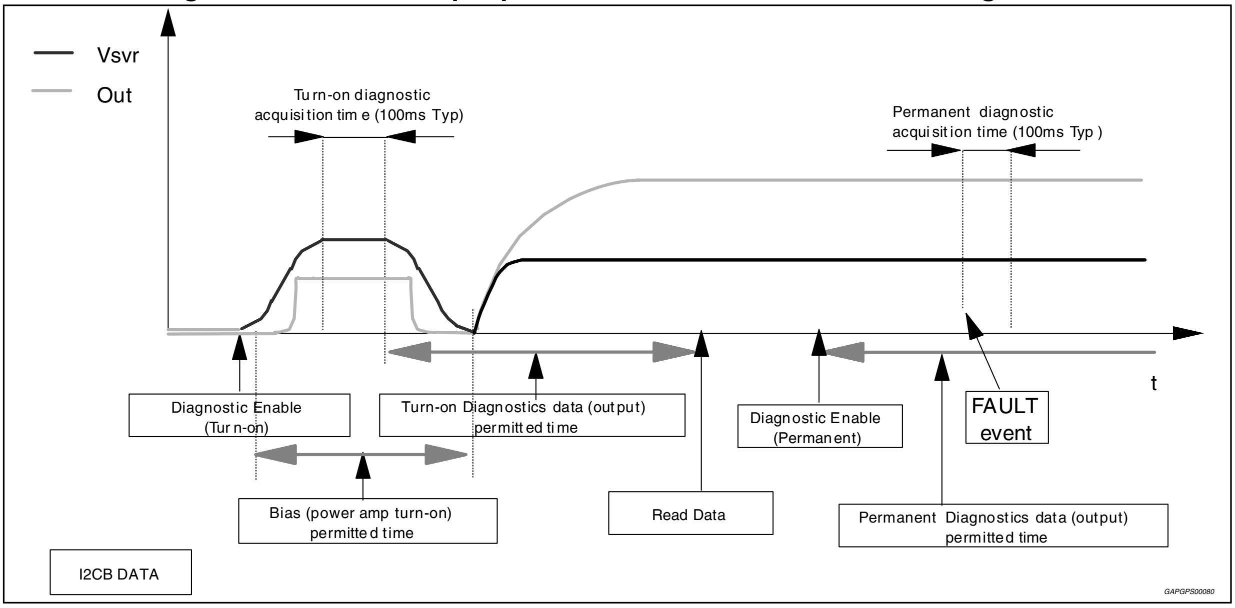
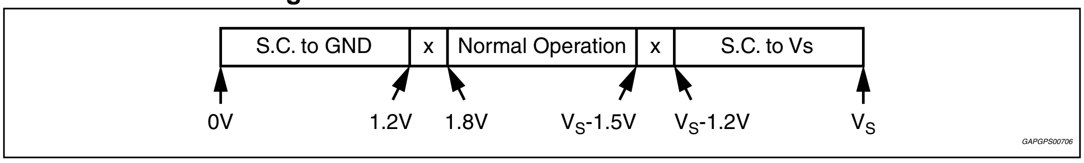


Figure 25. SVR and output pin behavior - case 2: with turn-on diagnostic



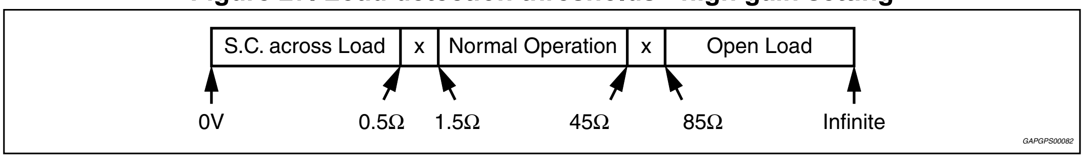
The information related to the outputs status is read and memorized at the end of the current pulse plateau. The acquisition time is 100 ms (typ.). No audible noise is generated in the process. As for SHORT TO GND / Vs the fault-detection thresholds remain unchanged from 26 dB to 16 dB gain setting. They are as follows:

Figure 26. Short circuit detection thresholds



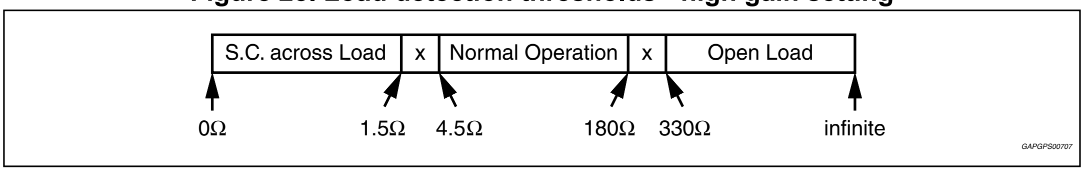
Concerning SHORT ACROSS THE SPEAKER / OPEN SPEAKER, the threshold varies from 26 dB to 16 dB gain setting, since different loads are expected (either normal speaker's impedance or high impedance). The values in case of 26 dB gain are as follows:

Figure 27. Load detection thresholds - high gain setting



If the Line-Driver mode (Gv = 16 dB and Line Driver Mode diagnostic = 1) is selected, the same thresholds will change as follows:

Figure 28. Load detection thresholds - high gain setting



4.2 Permanent diagnostics

Detectable conventional faults are:

- SHORT TO GND
- SHORT TO Vs
- SHORT ACROSS THE SPEAKER

The following additional feature is provided:

- OUTPUT OFFSET DETECTION

The TDA7577BLV has 2 operating status:

1. RESTART mode. The diagnostic is not enabled. Each audio channel operates independently of each other. If any of the a.m. faults occurs, only the channel(s) interested is shut down. A check of the output status is made every 1 ms (*Figure 29*). Restart takes place when the overload is removed.
2. DIAGNOSTIC mode. It is enabled via I^2C bus and it self activates if an output overload (such as to cause the intervention of the short-circuit protection) occurs to the speakers outputs. Once activated, the diagnostics procedure develops as follows (*Figure 30*):
   – To avoid momentary re-circulation spikes from giving erroneous diagnostics, a check of the output status is made after 1ms: if normal situation (no overloads) is detected, the diagnostic is not performed and the channel returns active.
   – Instead, if an overload is detected during the check after 1 ms, then a diagnostic cycle having a duration of about 100 ms is started.
   – After a diagnostic cycle, the audio channel interested by the fault is switched to RESTART mode. The relevant data are stored inside the device and can be read by the microprocessor. When one cycle has terminated, the next one is activated by an I^2C reading. This is to ensure continuous diagnostics throughout the car-radio operating time.
   – To check the status of the device a sampling system is needed. The timing is chosen at microprocessor level (more than half a second is recommended).

Figure 29. Restart timing without diagnostic enable (permanent) each 1ms time, a sampling of the fault is done

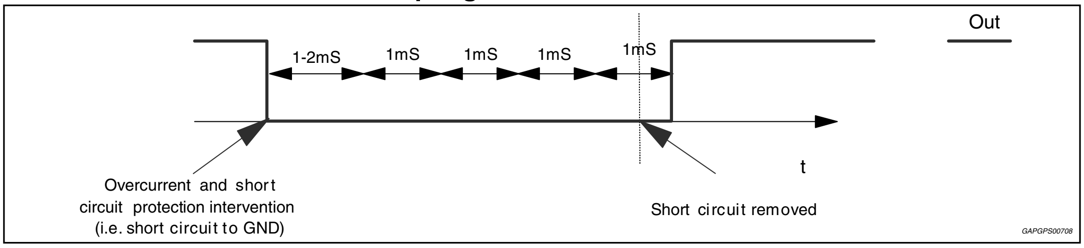
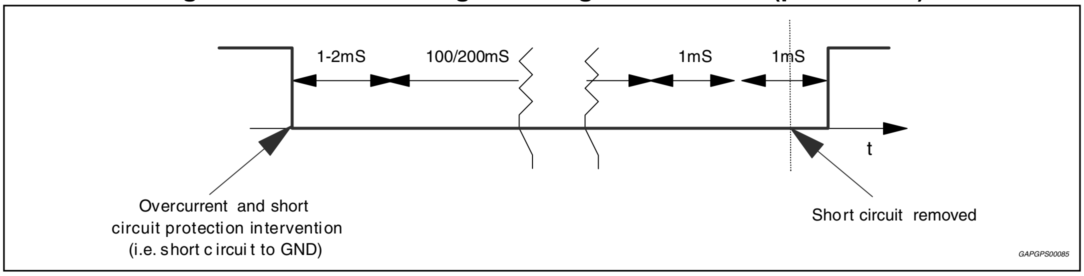


Figure 30. Restart timing with diagnostic enable (permanent)



4.3 Output DC offset detection

Any DC output offset exceeding ± 2 V is signalled out. This inconvenient might occur as a consequence of initially defective or aged and worn-out input capacitors feeding a DC component to the inputs, so putting the speakers at risk of overheating.

This diagnostic has to be performed with low-level output AC signal (or Vin = 0).

The test is run with selectable time duration by microprocessor (from a "start" to a "stop" command):

- START = Last reading operation or setting IB1 - D5 - (OFFSET enable) to 1
- STOP = Actual reading operation

Excess offset is signalled out if it is persistent for all the assigned testing time. This feature is disabled if any overloads leading to activation of the short-circuit protection occurs in the process.

4.4 AC diagnostic

It is targeted at detecting accidental disconnection of tweeters in 2-way speaker and, more in general, presence of capacitively (AC) coupled loads.

This diagnostic is based on the notion that the overall speaker's impedance (woofer + parallel tweeter) will tend to increase towards high frequencies if the tweeter gets disconnected, because the remaining speaker (woofer) would be out of its operating range (high impedance). The diagnostic decision is made according to peak output current thresholds, and it is enabled by setting (IB2-D2) = 1. Two different detection levels are available:

- HIGH CURRENT THRESHOLD IB2 (D7) = 0
  Iout > 500mApk = NORMAL STATUS
  Iout < 250mApk = OPEN TWEETER
- LOW CURRENT THRESHOLD IB2 (D7) = 1
  Iout > 250mApk = NORMAL STATUS
  Iout < 125mApk = OPEN TWEETER

To correctly implement this feature, it is necessary to briefly provide a signal tone (with the amplifier in "play") whose frequency and magnitude are such as to determine an output current higher than 500 mApk with IB2(D7) = 0 (higher than 250 mApk with IB2(D7) = 1) in normal conditions and lower than 250 mApk with IB2(D7) = 0 (lower than 125 mApk with IB2(D7) = 1) should the parallel tweeter be missing.

The test has to last for a minimum number of 3 sine cycles starting from the activation of the AC diagnostic function IB2<D2>) up to the I^2C reading of the results (measuring period). To confirm presence of tweeter, it is necessary to find at least 3 current pulses exceeding the above threshold over all the measuring period, else an "open tweeter" message will be issued.

The frequency / magnitude setting of the test tone depends on the impedance characteristics of each specific speaker being used, with or without the tweeter connected (to be calculated case by case). High-frequency tones (> 10 kHz) or even ultrasonic signals are recommended for their negligible acoustic impact and also to maximize the impedance module's ratio between with tweeter-on and tweeter-off.

Figure 31 and *32* shows the load impedance as a function of the peak output voltage and the relevant diagnostic fields.

It is recommended to keep output voltage always below 8 V (high threshold) or 4 V (low threshold) to avoid circuit to saturate (causing wrong detection cases).

This feature is disabled if any overloads leading to activation of the short-circuit protection occurs in the process.

Figure 31. Current detection high: load impedance |Z| vs. output peak voltage

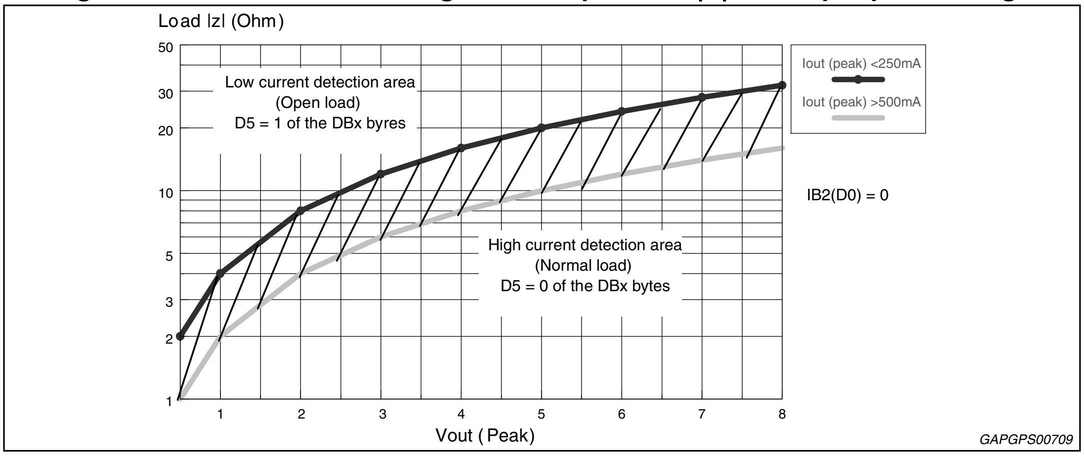
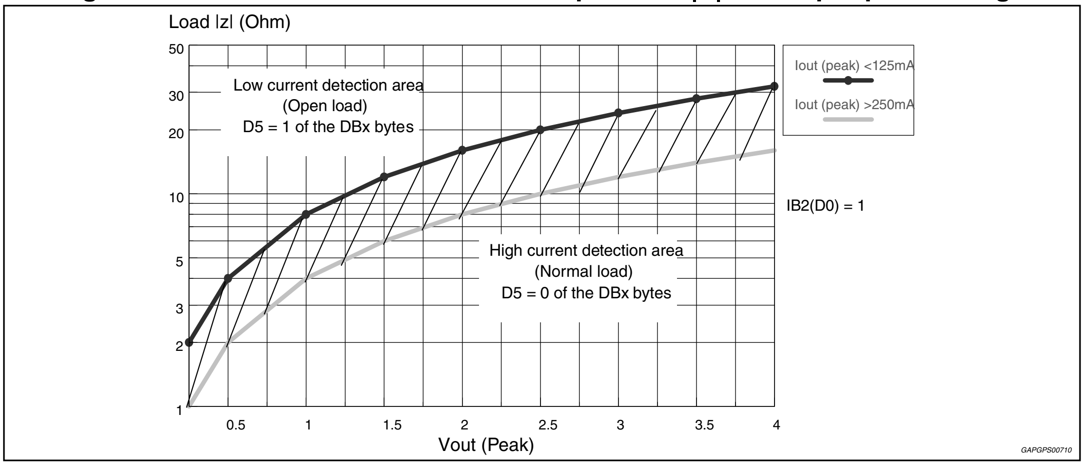


Figure 32. Current detection low: load impedance |Z| vs. output peak voltage



4.5 Multiple faults

When more misconnections are simultaneously in place at the audio outputs, it is guaranteed that at least one of them is initially read out. The others are notified after successive cycles of I^2C reading and faults removal, provided that the diagnostic is enabled. This is true for both kinds of diagnostic (Turn on and Permanent).

The table below shows all the couples of double-fault possible. It should be taken into account that a short circuit with the 4 Ω speaker unconnected is considered as double fault.

Table 5. Double fault table for turn on diagnostic

	S. GND	S. Vs	S. Across L.	Open L.
S. GND	S. GND	S. Vs + S. GND	S. GND	S. GND
S. Vs	/	S. Vs	S. Vs	S. Vs
S. Across L.	/	/	S. Across L.	N.A.
Open L.	/	/	/	Open L. (*)

In Permanent Diagnostic the table is the same, with only a difference concerning Open Load(*), which is not among the recognizable faults. Should an Open Load be present during the device's normal working, it would be detected at a subsequent Turn on Diagnostic cycle (i.e. at the successive car radio turn-on).

4.6 Fault presence information availability on I^2C

All the results coming from I^2C bus, by read operations, are the consequence of measurements inside a defined period of time. If the fault is stable throughout the whole period, it will be sent out. This is true for DC diagnostic (Turn-on and Permanent), for offset detector.

To guarantee always resident functions, every kind of diagnostic cycles (turn-on, Permanent, Offset) will be reactivated after any I^2C reading operation. Each I^2C read-out done by the microcontroller will enable a new diagnostic cycle, but the read data will come from the previous diagnostic cycle (i.e. The device is in turn-on state, with a short to GND, then the short is removed and micro reads I^2C. The short to GND is still present in bytes, because it is the result of the previous cycle. If another I^2C reading operation occurs, the bytes do not show the short). In general to observe a change in diagnostic bytes, two I^2C reading operations are necessary.

5 1 Ω load capability setting

It is possible to drive 1 Ω load paralleling the outputs into a single channel.

In order to implement this feature, outputs should be connected as follows:

OUT1+ shorted to OUT2+

OUT1- shorted to OUT2-.

It is recommended to minimize the impedance on the board between OUT2 and the load in order to minimize THD distortion. It is also recommended to control the maximum mismatch impedance between V_{CC} pins (PIN21/PIN22 respect to PIN33/PIN34) and between PWGND pins (PIN24/PIN25 respect to PIN30/PIN31), mismatch that must not exceed a value of 20 mΩ.

With 1Ω feature settled the active input is IN2 (PIN17 and PIN18), therefore IN1 pins should be let floating.

It is possible to set the load capability acting on 1 Ω pin as follows:

1 Ω PIN < 1.2V: two channels mode (for a minimum load of 2 Ω)

1 Ω PIN > 2.6V: one channel mode (for 1 Ω load).

It is to remember that 1 Ω function is a hardware selection.

Therefore it is recommended to leave 1 Ω pin floating or shorted to GND to set the two channels mode configuration, or to short 1 Ω pin to V_{CC} to set the one channel (1 Ω) configuration.

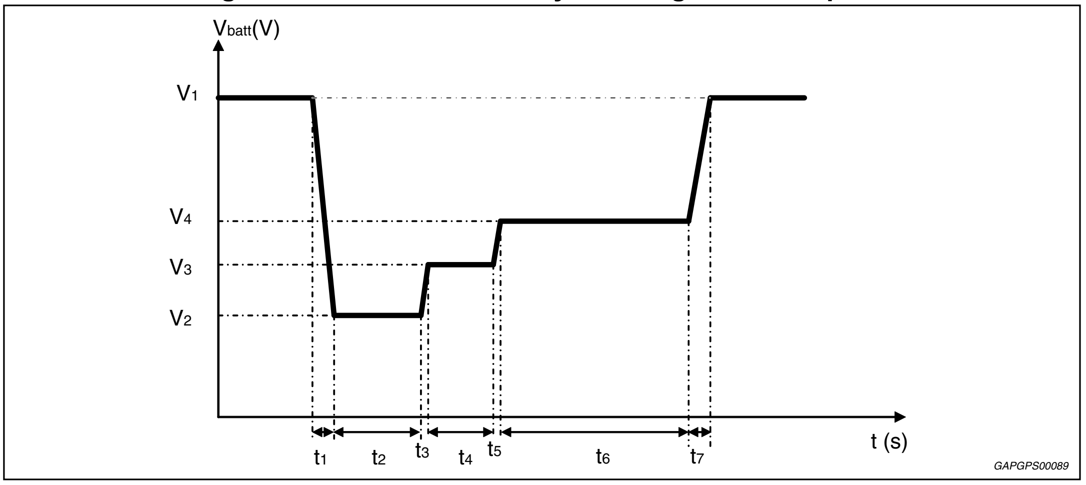
6 Battery transitions management

6.1 Low voltage operation (“start stop”)

The most recent OEM specifications require automatic stop of car engine at traffic light, in order to reduce emissions of polluting substances. The TDA7577BLV, thanks to its innovating design, is able to play when battery falls down to 6/7 V during such conditions, without producing audible pop noise. The maximum system power will be reduced accordingly.

Worst case battery cranking curves are shown below, indicating the shape and duration of allowed battery transitions.

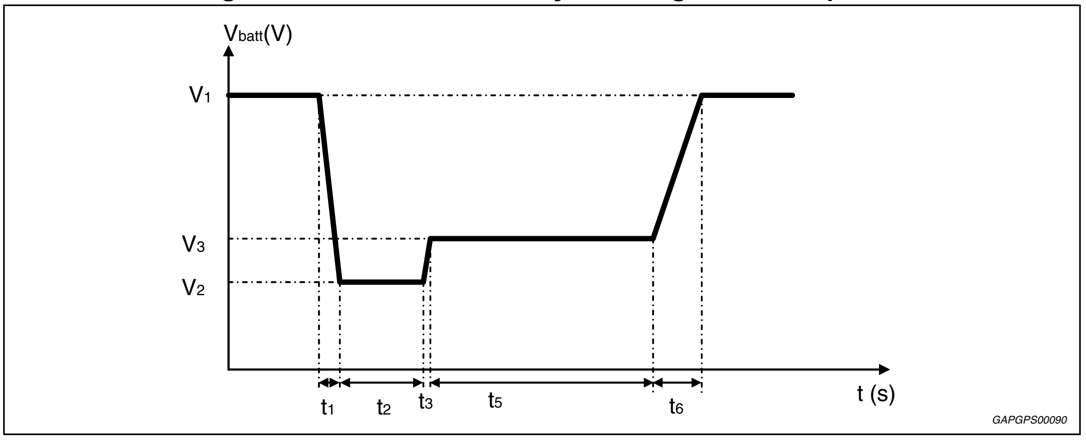
Figure 33. Worst case battery cranking curve sample 1



V1 = 12 V; V2 = 6 V; V3 = 7 V; V4 = 8 V

t1 = 2 ms; t2 = 50 ms; t3 = 5 ms; t4 = 300 ms; t5 =10 ms; t6 = 1 s; t7 = 2 ms

Figure 34. Worst case battery cranking curve sample 2



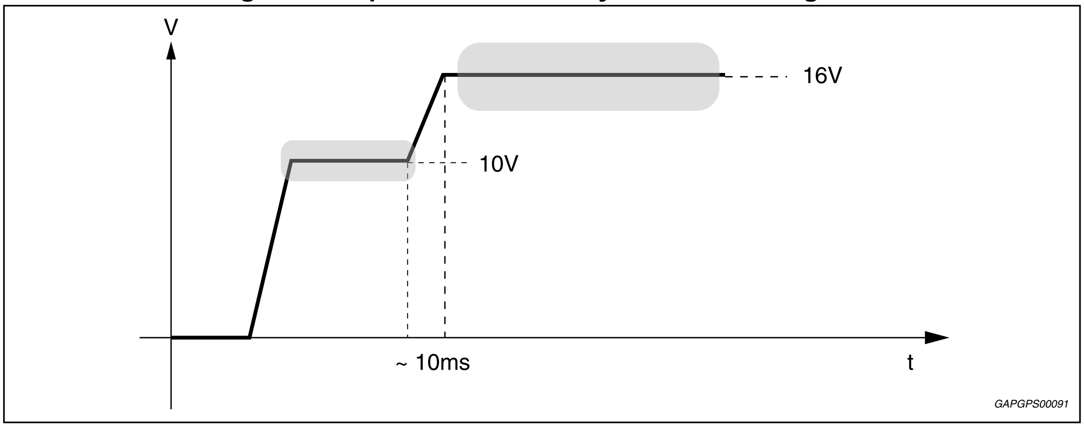
V1 = 12 V; V2 = 6 V; V3 = 7 V

t1 = 2 ms; t2 = 5 ms; t3 = 15 ms; t5 = 1 s; t6 = 50 ms

6.2 Advanced battery management

In addition to compatibility with low V_{batt}, the TDA7577BLV is able to substain upwards fast battery transitions (like the one showed in *Figure 35*) without causing unwanted audible effect, thanks to the innovative circuit topology.

Figure 35. Upwards fast battery transitions diagram



7 I^2C mode and legacy mode selection

It is possible to disable the I^2C interface by acting on I2C EN pin and control the TDA7577BLV by means of the usual ST-BY and MUTE pins. In order to activate or deactivate this feature, I2C-EN must be set as follows:

- I2C-EN (PIN16) < 1.5 V:
  - I^2C bus interface deactivated
- I2C-EN (PIN16) > 2.5 V:
  - I^2C bus interface activated

(It is also possible to let I2C-EN PIN floating to deactivate the I^2C bus interface, or to short to V_{CC} to activate I^2C).

In particular:

When I^2C is ENABLED: (I2C-EN pin > 2.5 V) then there are the following modes:

- STD MODE: V_{stby} (PIN5) > 2.6 V, IB2(D1)=0
- HE MODE: V_{stby} (PIN5) > 2.6 V, IB2(D1)=1
- PLAY MODE: V_{mute} (pin 4) > 2.6 V, IB1 (D2) = 1

The amplifier can always be switched off by putting V_{stby} to 0V, but with I^2C enabled it can be turn on only through I^2C (with V_{stby} > 2.6 V).

When I^2C is DISABLED: (I2C pin < 1.5 V) then there are the following modes:

- STD MODE: 2.6 V < ST-BY (PIN5) < 5 V
- HE MODE: V_{stby} (PIN5) > 7 V
- PLAY MODE: V_{mute} (pin 4) > 2.6 V

For both STD and HE MODE the play/mute mode can be set acting on V_{mute} pin.

In legacy mode (I^2C disabled), faults (diagnostics information) are available on HW pin CD-Out. CD-Out pin is active on a low value [CD-Out low = fault detected]. The faults detected are: short to ground or V_{CC}, short across the load.

8 Application suggestions

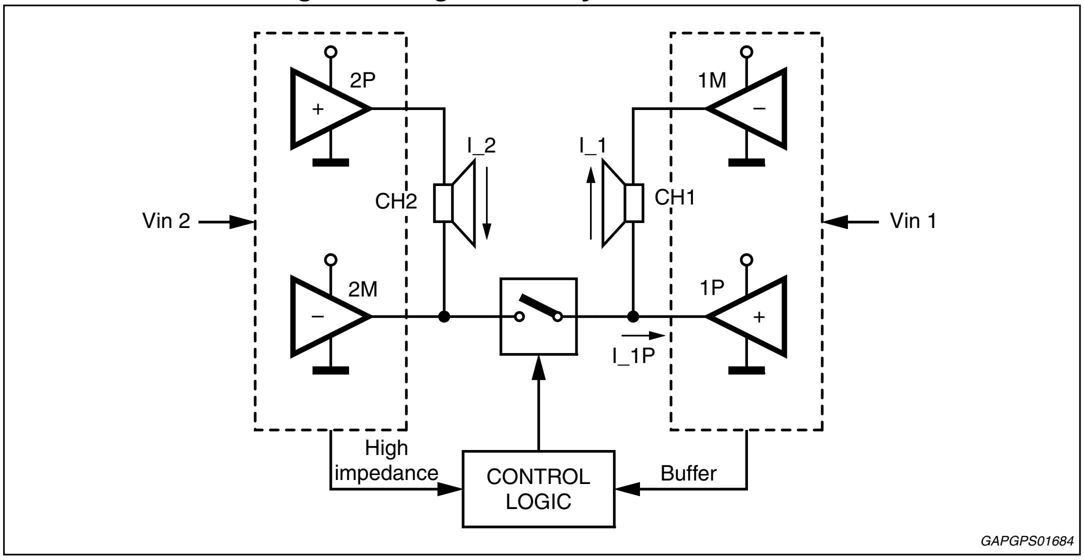
8.1 High efficiency introduction

Thanks to its operating principle, the TDA7577BLV obtains a substantial reduction of power dissipation from traditional class-AB amplifiers without being affected by the massive radiation effects and complex circuitry normally associated with class-D solutions.

The high efficiency operating principle is based on the use of bridge structures which are connected by means of a power switch (*Figure 1*). The switch, controlled by a logic circuit which senses the input signals, is closed at low volumes (output power steadily lower than 2.5 W) and the system acts like a "single bridge" with double load. In this case, the total power dissipation is a quarter of a double bridge.

Due to its structure, the highest efficiency level can be reached when symmetrical loads are applied on channels sharing the same switch.

Figure 36. High efficiency - basic structure



When the power demand increases to more than 2.5 W, the system behavior is switched back to a standard double bridge in order to guarantee the maximum output power, while in the 6 V start-stop devices the High Efficiency mode is automatically disabled at low V_{CC} (7.3 V ±0.3 V). No need to re-program it when Vcc goes back to normal levels.

In the range 2-4 W (@ V_{CC} = 14.4 V), with the High Efficiency mode, the dissipated power gets up to 50 % less than the value obtained with the standard mode.

9 I^2C bus interface

Data transmission from microprocessor to the TDA7577BLV and vice versa takes place through the 2 wires I^2C bus interface, consisting of the two lines SDA and SCL (pull-up resistors to positive supply voltage must be connected).

9.1 Data validity

As shown by *Figure 37*, the data on the SDA line must be stable during the high period of the clock.
The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

9.2 Start and stop conditions

As shown by *Figure 38* a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH.
The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH.

9.3 Byte format

Every byte transferred to the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

9.4 Acknowledge

The transmitter(*) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see *Figure 39*). The receiver(**) has to pull-down (LOW) the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during this clock pulse.

(*) Transmitter
- = master (µP) when it writes an address to the TDA7577BLV
- = slave (TDA7577BLV) when the µP reads a data byte from TDA7577BLV

(**) Receiver
- = slave (TDA7577BLV) when the µP writes an address to the TDA7577BLV
- = master (µP) when it reads a data byte from TDA7577BLV

Figure 37. Data validity on the I^2C bus

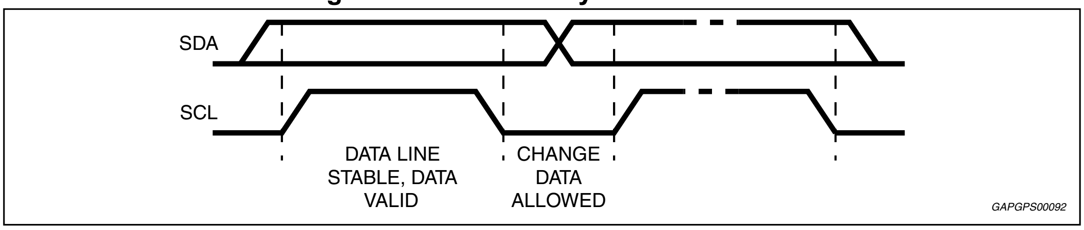


Figure 38. Timing diagram on the I²C bus

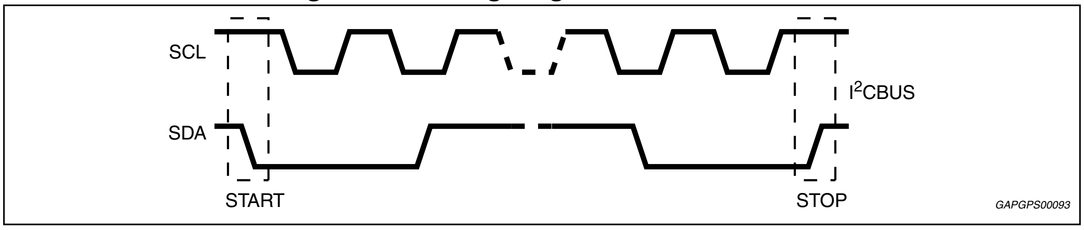
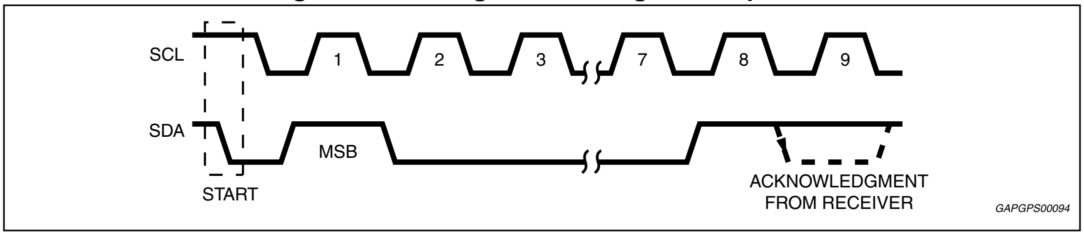


Figure 39. Timing acknowledge clock pulse



9.5 I²C programming/reading sequences

A correct turn on/off sequence with respect to the diagnostic timings and producing no audible noises could be as follows (after battery connection):

- TURN-ON: (STANDBY OUT + DIAG ENABLE) --- 1 s (min) --- MUTING OUT
- TURN-OFF: MUTING IN --- 20 ms --- (DIAG DISABLE + STAND-BY IN)

Car Radio Installation: DIAG ENABLE (write) --- 200ms --- I²C read (repeat until All faults disappear).

- OFFSET TEST: Device in Play (no signal) --
- OFFSET ENABLE - 30ms - I²C reading

(repeat I²C reading until high-offset message disappears).

10 Software specifications

All the functions of the TDA7577BLV are activated by I^2C interface.

The bit 0 of the "ADDRESS BYTE" defines if the next bytes are write instruction (from µP to TDA7577BLV) or read instruction (from TDA7577BLV to µP).

Table 6. Address selection

Bit	Selection
A6	1
A5	1
A4	0
A3	1
A2	0
A1	B
A0	A
R/W	X

If R/W = 0, the µP sends 2 "Instruction Bytes": IB1 and IB2.

Table 7. IB1

Bit	Instruction decoding bit
D7	Supply voltage mute high threshold (D7 = 1) Supply voltage mute low threshold (D7 = 0)
D6	Diagnostic enable (D6 = 1) Diagnostic defeat (D6 = 0)
D5	Offset Detection enable (D5 = 1) Offset Detection defeat (D5 = 0)
D4	Gain = 26 dB (D4 = 0) Gain = 16 dB (D4 = 1)
D3	0
D2	Mute (D2 = 0) Unmute (D2 = 1)
D1	0
D0	CD 2% (D0 = 0) CD 10% (D0 = 1)

Table 8. IB2

Bit	Instruction decoding bit
D7	Current Detection Threshold HIGH (D7 =0) Current Detection Threshold LOW (D7 =1)
D6	0
D5	Fast muting disable - (D5 = 0) Fast muting enable - (D5 = 1)
D4	Stand-by on - Amplifier not working - (D4 = 0) Stand-by off - Amplifier working - (D4 = 1)
D3	Power Amplifier Mode Diagnostic (D3 = 0); Line Driver Mode Diagnostic (D3 = 1)
D2	Current Detection Diagnostic Enabled (D2 = 1) Current Detection Diagnostic Defeat (D2 = 0)
D1	Power amplifier working in standard mode (D1 = 0) Power amplifier working in high efficiency mode (D1 = 1)
D0	0

If R/W = 1, the TDA7577BLV sends 2 "Diagnostics Bytes" to µP: DB1 and DB2.

Table 9. DB1

<table>
<tr><th>Bit</th><th colspan="2">Instruction decoding bit</th></tr>
<tr><td>D7</td><td colspan="2">Thermal warning (if Tchip ≥ 150°C, D7 = 1)</td></tr>
<tr><td>D6</td><td colspan="2">Diag. cycle not activated or not terminated (D6 = 0)
Diag. cycle terminated (D6 = 1)</td></tr>
<tr><td>D5</td><td>Channel 1
Current detection IB2 (D0) = 0
Output peak current < 250 mA - Open load (D5 = 1)
Output peak current > 500 mA - Normal load (D5 = 0)</td><td>Channel1
Current detection IB2 (D0) = 1
Output peak current < 125 mA - Open load (D5 = 1)
Output peak current > 250 mA - Normal load (D5 = 0)</td></tr>
<tr><td>D4</td><td colspan="2">Channel 1
Turn-on diagnostic (D4 = 0)
Permanent diagnostic (D4 = 1)</td></tr>
<tr><td>D3</td><td colspan="2">Channel 1
Normal load (D3 = 0)
Short load (D3 = 1)</td></tr>
<tr><td>D2</td><td colspan="2">Channel 1
Turn-on diag.: No open load (D2 = 0)
Open load detection (D2 = 1)
Offset diag.: No output offset (D2 = 0)
Output offset detection (D2 = 1)</td></tr>
<tr><td>D1</td><td colspan="2">Channel 1
No short to V_{cc} (D1 = 0)
Short to V_{cc} (D1 = 1)</td></tr>
<tr><td>D0</td><td colspan="2">Channel 1
No short to GND (D0 = 0)
Short to GND (D0 = 1)</td></tr>
</table>

Table 10. DB2

<table>
<tr><th>Bit</th><th colspan="2">Instruction decoding bit</th></tr>
<tr><td>D7</td><td colspan="2">Offset detection not activated (D7 = 0)
Offset detection activated (D7 = 1)</td></tr>
<tr><td>D6</td><td colspan="2">Current sensor not activated (D6 = 0)
Current sensor activated (D6 = 1)</td></tr>
<tr><td>D5</td><td>Channel 2
Current detection IB2 (D0) = 0
Output peak current < 250 mA - Open load (D5 = 1)
Output peak current > 500 mA - Normal load (D5 = 0)</td><td>Channel 2
Current detection IB2 (D0) = 1
Output peak current < 125 mA - Open load (D5 = 1)
Output peak current > 250 mA - Normal load (D5 = 0)</td></tr>
<tr><td>D4</td><td colspan="2">Channel 2
Turn-on diagnostic (D4 = 0)
Permanent diagnostic (D4 = 1)</td></tr>
<tr><td>D3</td><td colspan="2">Channel 2
Normal load (D3 = 0)
Short load (D3 = 1)</td></tr>
<tr><td>D2</td><td colspan="2">Channel 2
Turn-on diag.: No open load (D2 = 0)
Open load detection (D2 = 1)
Permanent diag.: No output offset (D2 = 0)
Output offset detection (D2 = 1)</td></tr>
<tr><td>D1</td><td colspan="2">Channel 2
No short to V_{cc} (D1 = 0)
Short to V_{cc} (D1 = 1)</td></tr>
<tr><td>D0</td><td colspan="2">Channel 2
No short to GND (D0 = 0)
Short to GND (D0 = 1)</td></tr>
</table>

10.1 Examples of bytes sequence

1 - Turn-on diagnostic - Write operation

Start	Address byte with D0 = 0	ACK	IB1 with D6 = 1	ACK	IB2	ACK	STOP

2 - Turn-on diagnostic - Read operation

Start	Address byte with D0 = 1	ACK	DB1	ACK	DB2	ACK	STOP

The delay from 1 to 2 can be selected by software, starting from 1 ms

3a - Turn-on of the power amplifier with mute on, diagnostic defeat.

Start	Address byte with D0 = 0	ACK	IB1	ACK	IB2	ACK	STOP
			X000XXXX		XXX1XX1X		

3b - Turn-off of the power amplifier

Start	Address byte with D0 = 0	ACK	IB1	ACK	IB2	ACK	STOP
			X0XXXXXX		XXX0XXXX		

4 - Offset detection procedure enable

Start	Address byte with D0 = 0	ACK	IB1	ACK	IB2	ACK	STOP
			XX1XX1XX		XXX1XXXX		

5 - Offset detection procedure stop and reading operation (the results are valid only for the offset detection bits (D2 of the bytes DB1, DB2).

Start	Address byte with D0 = 1	ACK	DB1	ACK	DB2	ACK	STOP

- The purpose of this test is to check if a D.C. offset (2 V typ.) is present on the outputs, produced by input capacitor with anomalous leakage current or humidity between pins.
- The delay from 4 to 5 can be selected by software, starting from 1 ms.

11 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.

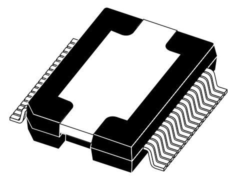
ECOPACK® is an ST trademark.

Figure 40. PowerSO36 (slug up) mechanical data and package dimensions

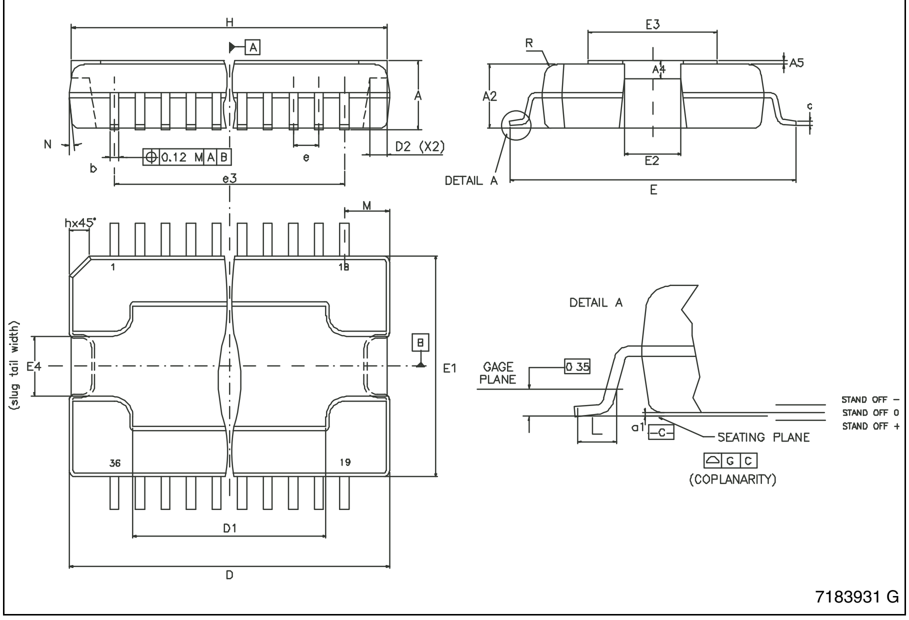
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	3.270	-	3.410	0.1287	-	0.1343
A2	3.100	-	3.180	0.1220	-	0.1252
A4	0.800	-	1.000	0.0315	-	0.0394
A5	-	0.200	-	-	0.0079	-
a1	0.030	-	-0.040	0.0012	-	-0.0016
b	0.220	-	0.380	0.0087	-	0.0150
c	0.230	-	0.320	0.0091	-	0.0126
D	15.800	-	16.000	0.6220	-	0.6299
D1	9.400	-	9.800	0.3701	-	0.3858
D2	-	1.000	-	-	0.0394	-
E	13.900	-	14.500	0.5472	-	0.5709
E1	10.900	-	11.100	0.4291	-	0.4370
E2	-	-	2.900	-	-	0.1142
E3	5.800	-	6.200	0.2283	-	0.2441
E4	2.900	-	3.200	0.1142	-	0.1260
e	-	0.650	-	-	0.0256	-
e3	-	11.050	-	-	0.4350	-
G	0	-	0.075	0	-	0.0031
H	15.500	-	15.900	0.6102	-	0.6260
h	-	-	1.100	-	-	0.0433
L	0.800	-	1.100	0.0315	-	0.0433
N	-	-	10°	-	-	10°
s	-	-	8°	-	-	8°

(1) "D and E1" do not include mold flash or protusions.
Mold flash or protusions shall not exceed 0.15mm (0.006").
(2) No intrusion allowed inwards the leads.

OUTLINE AND MECHANICAL DATA



PowerSO36 (SLUG UP)



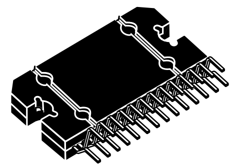
GAPGPS00098

Figure 41. Flexiwatt27 (vertical) mechanical data and package dimensions

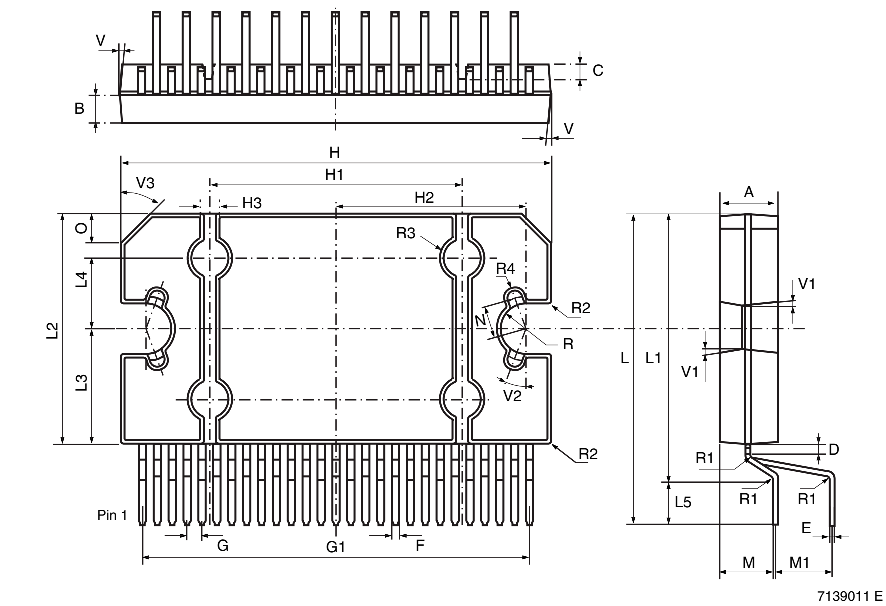
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.45	4.50	4.65	0.175	0.177	0.183
B	1.80	1.90	2.00	0.070	0.074	0.079
C		1.40			0.055	
D	0.75	0.90	1.05	0.029	0.035	0.041
E	0.37	0.39	0.42	0.014	0.015	0.016
F (1)			0.57			0.022
G	0.80	1.00	1.20	0.031	0.040	0.047
G1	25.75	26.00	26.25	1.014	1.023	1.033
H (2)	28.90	29.23	29.30	1.139	1.150	1.153
H1		17.00			0.669	
H2		12.80			0.503	
H3		0.80			0.031	
L (2)	22.07	22.47	22.87	0.869	0.884	0.904
L1	18.57	18.97	19.37	0.731	0.747	0.762
L2 (2)	15.50	15.70	15.90	0.610	0.618	0.626
L3	7.70	7.85	7.95	0.303	0.309	0.313
L4		5			0.197	
L5		3.5			0.138	
M	3.70	4.00	4.30	0.145	0.157	0.169
M1	3.60	4.00	4.40	0.142	0.157	0.173
N		2.20			0.086	
O		2			0.079	
R		1.70			0.067	
R1		0.5			0.02	
R2		0.3			0.12	
R3		1.25			0.049	
R4		0.50			0.019	
V	5° (Typ.)					
V1	3° (Typ.)					
V2	20° (Typ.)					
V3	45° (Typ.)					

(1): dam-bar protusion not included; (2): molding protusion included.

OUTLINE AND MECHANICAL DATA



Flexiwatt27 (vertical)



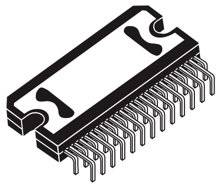
GAPGPS00096

Figure 42. Flexiwatt27 (horizontal) mechanical data and package dimensions

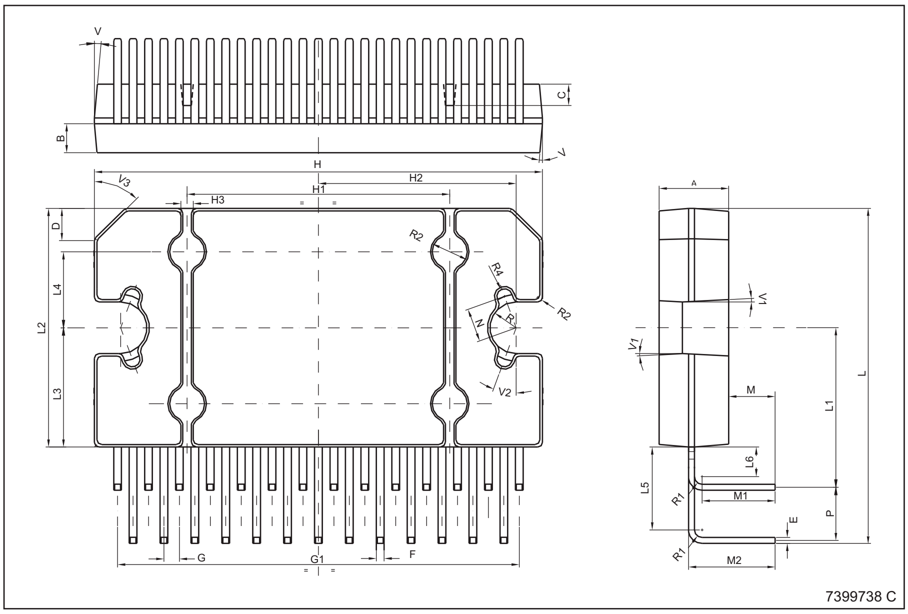
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.45	4.50	4.65	0.175	0.177	0.183
B	1.80	1.90	2.00	0.070	0.074	0.079
C		1.40			0.055	
D		2.00			0.079	
E	0.37	0.39	0.42	0.014	0.015	0.016
F (1)			0.57			0.022
G	0.75	1.00	1.25	0.0295	0.040	0.0492
G1	25.70	26.00	26.30	1.0118	1.023	1.0354
H (2)	28.90	29.23	29.30	1.139	1.150	1.153
H1		17.00			0.669	
H2		12.80			0.503	
H3		0.80			0.031	
L (2)	21.64	22.04	22.44	0.852	0.868	0.883
L1	10.15	10.5	10.85	0.40	0.413	0.427
L2 (2)	15.50	15.70	15.90	0.610	0.618	0.626
L3	7.70	7.85	7.95	0.303	0.309	0.313
L4		5			0.197	
L5	5.15	5.45	5.85	0.203	0.214	0.23
L6	1.80	1.95	2.10	0.070	0.077	0.083
M	2.75	3.00	3.50	0.108	0.118	0.138
M1		4.73			0.186	
M2		5.61			0.220	
N		2.20			0.086	
P	3.20	3.50	3.80	0.126	0.138	0.15
R		1.70			0.067	
R1		0.50			0.02	
R2		0.30			0.12	
R3		1.25			0.049	
R4		0.50			0.02	
V	5° (Typ.)					
V1	3° (Typ.)					
V2	20° (Typ.)					
V3	45° (Typ.)					

(1): dam-bar protusion not included; (2): molding protusionincluded

OUTLINE AND MECHANICAL DATA



Flexiwatt27 (Horizontal)



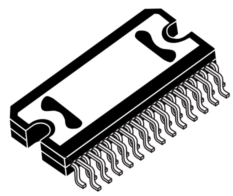
GAPGPS00095

Figure 43. Flexiwatt27 (SMD) mechanical data and package dimensions

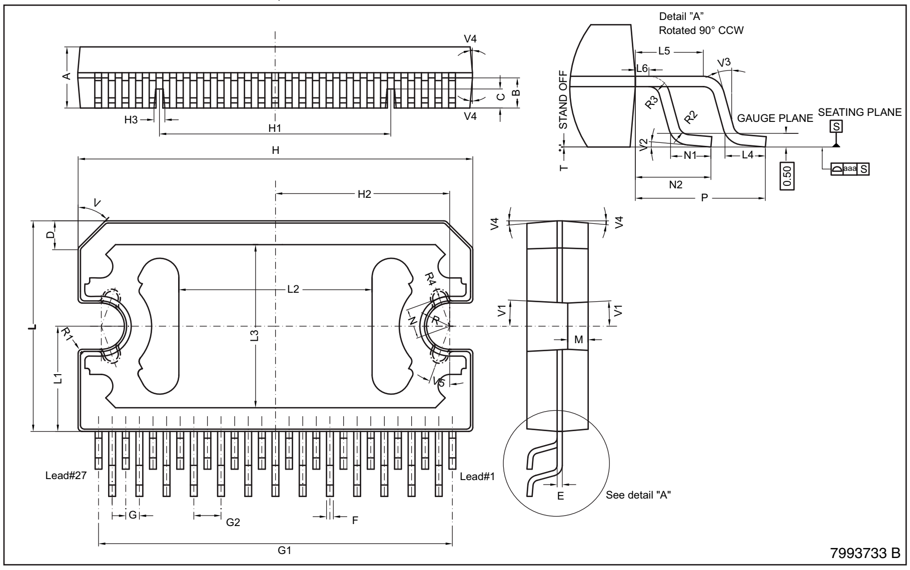
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.45	4.50	4.65	0.1752	0.1772	0.1831
B	2.12	2.22	2.32	0.0835	0.0874	0.0913
C		1.40			0.0551	
D		2.00			0.0787	
E	0.36	0.40	0.44	0.0142	0.0157	0.0173
F(**)	0.47	0.51	0.57	0.0185	0.0201	0.0224
G(*)	0.75	1.00	1.25	0.0295	0.0394	0.0492
G1	25.70	26.00	26.30	1.0118	1.0236	1.0354
G2(*)	1.75	2.00	2.25	0.0689	0.0787	0.0886
H(**)	28.85	29.23	29.40	1.1358	1.1508	1.1575
H1		17.00			0.6693	
H2		12.80			0.5039	
H3		0.80			0.0315	
L(**)	15.50	15.70	15.90	0.6102	0.6181	0.6260
L1	7.70	7.85	7.95	0.3031	0.3091	0.3130
L2	14.00	14.20	14.40	0.5512	0.5591	0.5669
L3	11.80	12.00	12.20	0.4646	0.4724	0.4803
L4	1.30	1.48	1.66	0.0512	0.0583	0.0654
L5	2.42	2.50	2.58	0.0953	0.0984	0.1016
L6	0.42	0.50	0.58	0.0165	0.0197	0.0228
M		1.50			0.0591	
N		2.20			0.0866	
N1	1.30	1.48	1.66	0.0512	0.0583	0.0654
N2(*)	2.73	2.83	2.93	0.1075	0.1114	0.1154
P(*)	4.73	4.83	4.93	0.1862	0.1902	0.1941
R		1.70			0.0669	
R1		0.30			0.0118	
R2	0.35	0.40	0.45	0.0138	0.0157	0.0177
R3	0.35	0.40	0.45	0.0138	0.0157	0.0177
R4		0.50			0.0197	
T(*)	-0.08		0.10	-0.0031		0.0039
aaa(*)		0.1			0.0039	
V		45°			45°	
V1		3°			3°	
V2	3°	5°	7°	3°	5°	7°
V3	12°	15°	18°	12°	15°	18°
V4		5°			5°	
V5		20°			20°	

(*) Golden parameters
(**) – Dimension "F" doesn't include dam-bar protrusion.
– Dimensions "H" and "L" include mold flash or protrusions.

OUTLINE AND MECHANICAL DATA



Flexiwatt27 (SMD)



GAPGPS00097

12 Revision history

Table 11. Document revision history

Date	Revision	Changes
14-Oct-2013	1	Initial release.