TS4990

1.2 W audio power amplifier with active-low standby mode

Features

- Operating from V_{CC} = 2.2 V to 5.5 V
- 1.2 W output power @ V_{CC} = 5 V, THD = 1%, F = 1 kHz, with 8Ω load
- Ultra-low consumption in standby mode (10 nA)
- 62 dB PSRR @ 217 Hz in grounded mode
- Near-zero pop & click
- Ultra-low distortion (0.1%)
- Unity gain stable
- Available in a 9-bump Flip-Chip, MiniSO-8 and DFN8 packages

Description

The TS4990 has been designed for demanding audio applications such as mobile phones and permits the reduction of the number of external components.

This audio power amplifier is capable of delivering 1.2 W of continuous RMS output power into an 8Ω load @ 5 V.

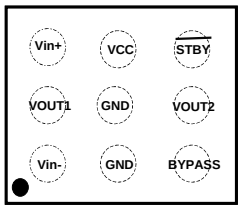
An externally-controlled standby mode reduces the supply current to less than 10 nA. It also includes internal thermal shutdown protection.

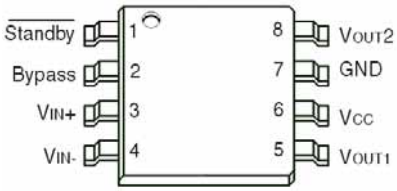
The unity-gain stable amplifier can be configured by external gain setting resistors.

Applications

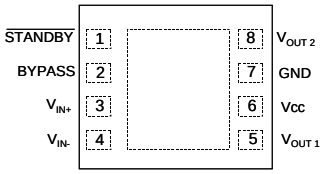
- Mobile phones (cellular / cordless)
- Laptop / notebook computers
- PDAs
- Portable audio devices

TS4990IJT/TS4990EIJT - Flip-Chip 9 bumps

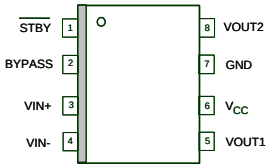




TS4990IQT - DFN8



TS4990ID/TS4990IDT - SO-8



Contents

1 Order codes

Part number	Temperature range	Package	Packing	Marking
TS4990IJT TS4990EIJT(1)	-40°C, +85°C	Flip-chip, 9 bumps	Tape & reel	90
TS4990IST		MiniSO-8	Tape & reel	K990
TS4990IQT		DFN8	Tape & reel	K990
TS4990EKIJT		FC + back coating	Tape & reel	90
TS4990ID/IDT		SO-8	Tube or tape & reel	TS4990I

1. Lead-free flip-chip part number.

2 Absolute maximum ratings & operating conditions

Table 1. Absolute maximum ratings (AMR)

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (1)	6	V
V_i	Input voltage (2)	GND to V_{CC}	V
T_{oper}	Operating free air temperature range	-40 to + 85	°C
T_{stg}	Storage temperature	-65 to +150	°C
T_j	Maximum junction temperature	150	°C
R_{thja}	Thermal resistance junction to ambient Flip-Chip (3) MiniSO-8 DFN8	 250 215 120	°C/W
P_{diss}	Power dissipation	Internally limited	
ESD	Human body model	2	kV
ESD	Machine model	200	V
	Latch-up immunity	200 mA	
	Lead temperature (soldering, 10sec) Lead temperature (soldering, 10sec) for Lead-Free version	250 260	°C

1. All voltage values are measured with respect to the ground pin.
2. The magnitude of the input signal must never exceed V_{CC} + 0.3V / G_{ND} - 0.3V.
3. The device is protected in case of over temperature by a thermal shutdown active @ 150°C.

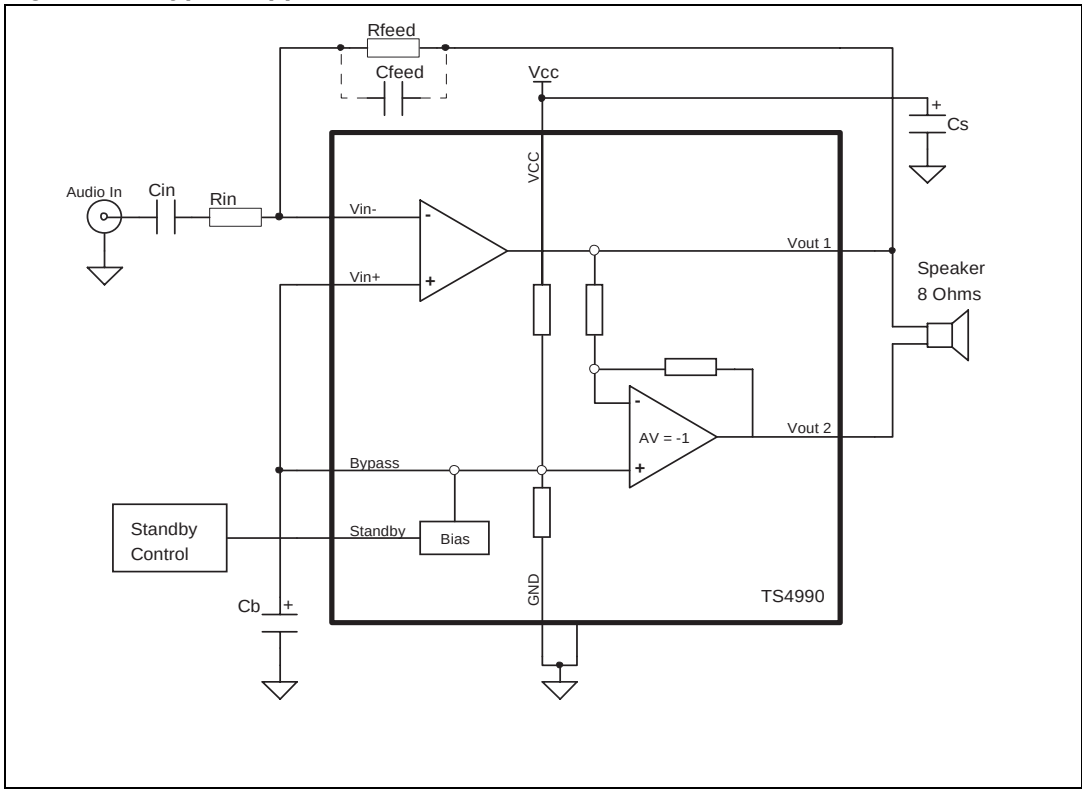
Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2.2 to 5.5	V
V_{ICM}	Common mode input voltage range	1.2V to V_{CC}	V
V_{STBY}	Standby voltage input: Device ON Device OFF	 $1.35 \leq V_{STB} \leq V_{CC}$ $GND \leq V_{STB} \leq 0.4$	V
R_L	Load resistor	≥ 4	Ω
R_{OUTGND}	Resistor output to GND (V_{STBY} = GND)	≥ 1	MΩ
T_{SD}	Thermal shutdown temperature	150	°C
R_{thja}	Thermal resistance junction to ambient Flip-chip (1) MiniSO-8 DFN8(2)	 100 190 40	°C/W

1. This thermal resistance is reached with a 100mm^2 copper heatsink surface.
2. When mounted on a 4-layer PCB.

3 Typical application schematic

Figure 1. Typical application schematic



4 Electrical characteristics

Table 3. Electrical characteristics when V_{CC} = +5 V, GND = 0 V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current No input signal, no load		3.7	6	mA
I_{STBY}	Standby current (1) No input signal, V_{STBY} = G_{ND}, R_L = 8Ω		10	1000	nA
V_{oo}	Output offset voltage No input signal, R_L = 8Ω		1	10	mV
P_{out}	Output power THD = 1% Max, F = 1kHz, R_L = 8Ω	0.9	1.2		W
THD + N	Total harmonic distortion + noise P_{out} = 1Wrms, A_V = 2, 20Hz ≤ F ≤ 20kHz, R_L = 8Ω		0.2		%
PSRR	Power supply rejection ratio(2) R_L = 8Ω, A_V = 2, V_{ripple} = 200mVpp, input grounded F = 217Hz F = 1kHz	 55 55	 62 64		dB
t_{WU}	Wake-up time (C_b = 1µF)		90	130	ms
t_{STBY}	Standby time (C_b = 1µF)		10		µs
V_{STBYH}	Standby voltage level high			1.3	V
V_{STBYL}	Standby voltage level low			0.4	V
Φ_M	Phase margin at unity gain R_L = 8Ω, C_L = 500pF		65		Degrees
GM	Gain margin R_L = 8Ω, C_L = 500pF		15		dB
GBP	Gain bandwidth product R_L = 8Ω		1.5		MHz

1. Standby mode is activated when V_{STBY} is tied to GND.
2. All PSRR data limits are guaranteed by production sampling tests.
Dynamic measurements - 20*log(rms(Vout)/rms(V_{ripple})). V_{ripple} is the sinusoidal signal superimposed upon Vcc.

Table 4. Electrical characteristics when V_{CC} = +3.3 V, GND = 0 V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current No input signal, no load		3.3	6	mA
I_{STBY}	Standby current (1) No input signal, V_{STBY} = G_{ND}, R_L = 8Ω		10	1000	nA
V_{oo}	Output offset voltage No input signal, R_L = 8Ω		1	10	mV
P_{out}	Output power THD = 1% Max, F = 1kHz, R_L = 8Ω	375	500		mW
THD + N	Total harmonic distortion + noise P_{out} = 400mWrms, A_V = 2, 20Hz ≤ F ≤ 20kHz, R_L = 8Ω		0.1		%
PSRR	Power supply rejection ratio(2) R_L = 8Ω, A_V = 2, V_{ripple} = 200mVpp, input grounded F = 217Hz F = 1kHz	 55 55	 1 63		dB
t_{WU}	Wake-up time (C_b = 1µF)		110	140	ms
t_{STBY}	Standby time (C_b = 1µF)		10		µs
V_{STBYH}	Standby voltage level high			1.2	V
V_{STBYL}	Standby voltage level low			0.4	V
Φ_M	Phase margin at unity gain R_L = 8Ω, C_L = 500pF		65		Degrees
GM	Gain margin R_L = 8Ω, C_L = 500pF		15		dB
GBP	Gain bandwidth product R_L = 8Ω		1.5		MHz

1. Standby mode is activated when V_{STBY} is tied to GND.
2. All PSRR data limits are guaranteed by production sampling tests.
Dynamic measurements - 20*log(rms(Vout)/rms(V_{ripple})). V_{ripple} is the sinusoidal signal superimposed upon Vcc.

Table 5. Electrical characteristics when V_{CC} = 2.6V, GND = 0V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current No input signal, no load		3.1	6	mA
I_{STBY}	Standby current (1) No input signal, V_{STBY} = G_{ND}, R_L = 8Ω		10	1000	nA
V_{oo}	Output offset voltage No input signal, R_L = 8Ω		1	10	mV
P_{out}	Output power THD = 1% Max, F = 1kHz, R_L = 8Ω	220	300		mW
THD + N	Total harmonic distortion + noise P_{out} = 200mWrms, A_V = 2, 20Hz ≤ F ≤ 20kHz, R_L = 8Ω		0.1		%
PSRR	Power supply rejection ratio(2) R_L = 8Ω, A_V = 2, V_{ripple} = 200mVpp, input grounded F = 217Hz F = 1kHz	 55 55	 60 62		dB
t_{WU}	Wake-up time (C_b = 1µF)		125	150	ms
t_{STBY}	Standby time (C_b = 1µF)		10		µs
V_{STBYH}	Standby voltage level high			1.2	V
V_{STBYL}	Standby voltage level low			0.4	V
Φ_M	Phase margin at unity gain R_L = 8Ω, C_L = 500pF		65		Degrees
GM	Gain margin R_L = 8Ω, C_L = 500pF		15		dB
GBP	Gain bandwidth product R_L = 8Ω		1.5		MHz

1. Standby mode is activated when V_{STBY} is tied to GND.
2. All PSRR data limits are guaranteed by production sampling tests.
Dynamic measurements - 20*log(rms(V_{out})/rms(V_{ripple})). V_{ripple} is the sinusoidal signal superimposed upon Vcc.

Table 6. Component descriptions

Component	Functional description
R_{in}	Inverting input resistor which sets the closed loop gain in conjunction with R_{feed}. This resistor also forms a high pass filter with C_{in} (F_c = 1 / (2 x Pi x R_{in} x C_{in})).
C_{in}	Input coupling capacitor which blocks the DC voltage at the amplifier input terminal.
R_{feed}	Feed back resistor which sets the closed loop gain in conjunction with R_{in}.
C_s	Supply bypass capacitor which provides power supply filtering.
C_b	Bypass pin capacitor which provides half supply filtering.
C_{feed}	Low pass filter capacitor allowing to cut the high frequency (low pass filter cut-off frequency 1 / (2 x Pi x R_{feed} x C_{feed})).
A_V	Closed loop gain in BTL configuration = 2 x (R_{feed} / R_{in}).
Exposed Pad	DFN8 exposed pad is electrically connected to pin 7. See *DFN8 package on page 31* for more information.

Figure 2. Open loop frequency response

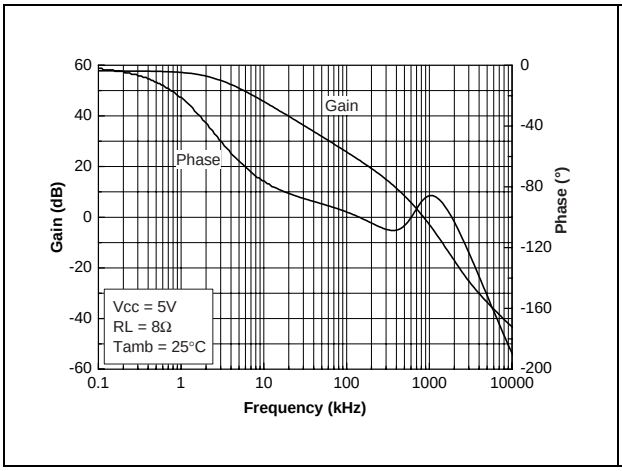


Figure 3. Open loop frequency response

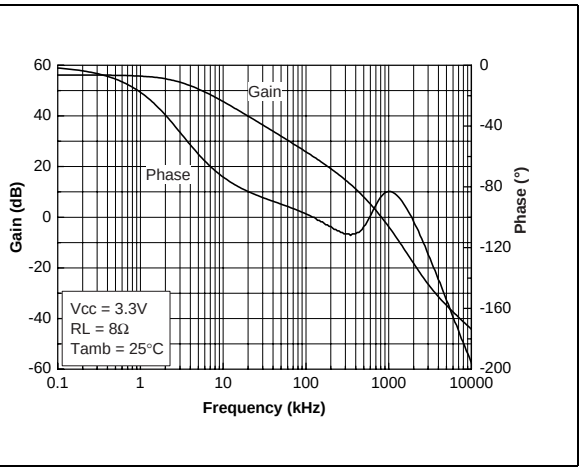


Figure 4. Open loop frequency response

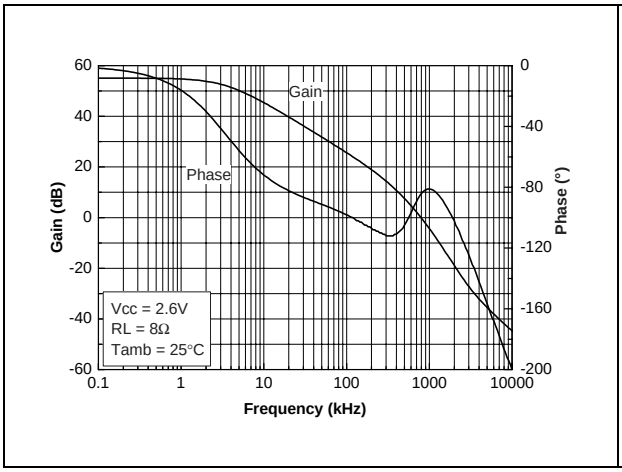


Figure 5. Open loop frequency response

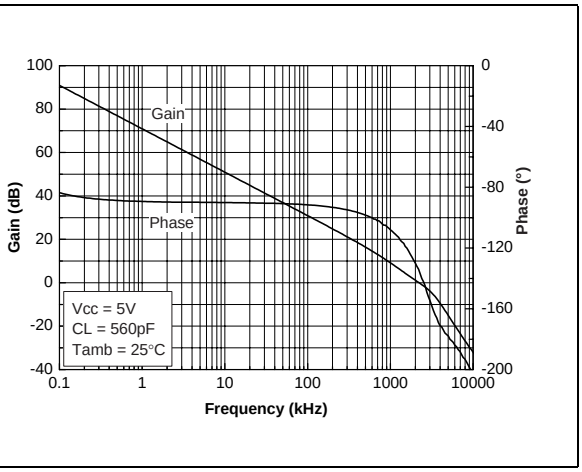


Figure 6. Open loop frequency response

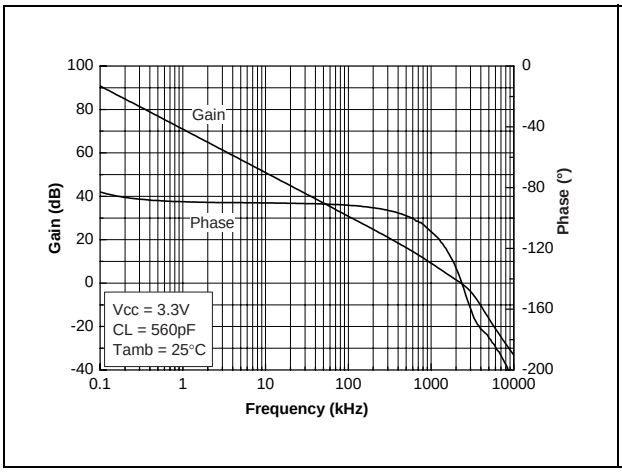


Figure 7. Open loop frequency response

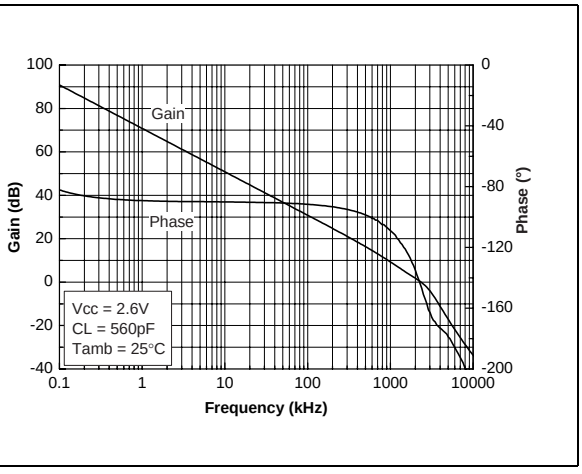


Figure 8. PSRR vs. power supply

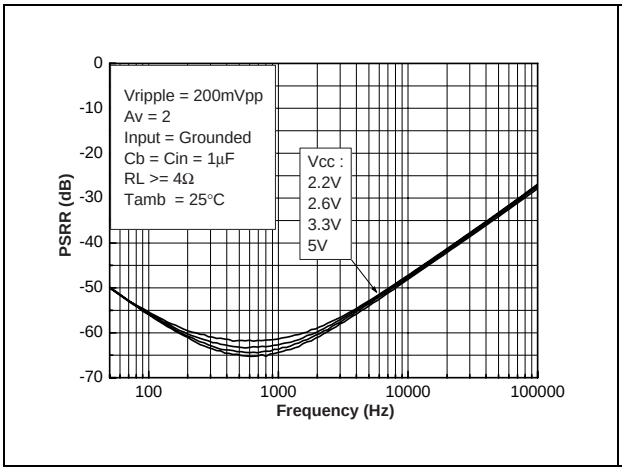


Figure 9. PSRR vs. power supply

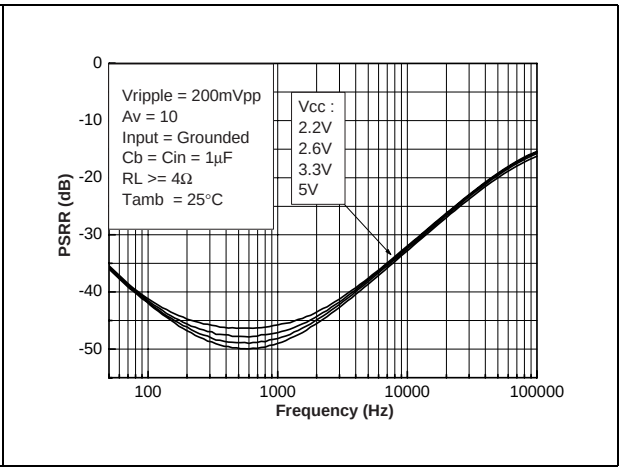


Figure 10. PSRR vs. power supply

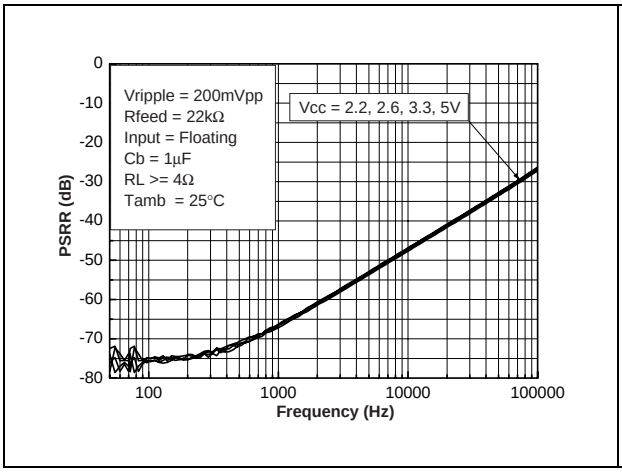


Figure 11. PSRR vs. power supply

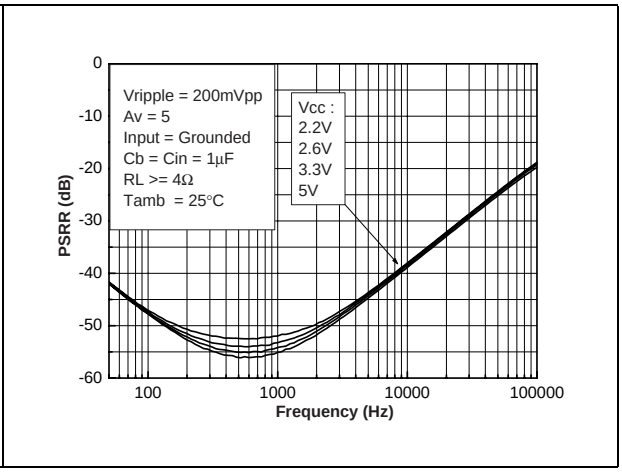


Figure 12. PSRR vs. power supply

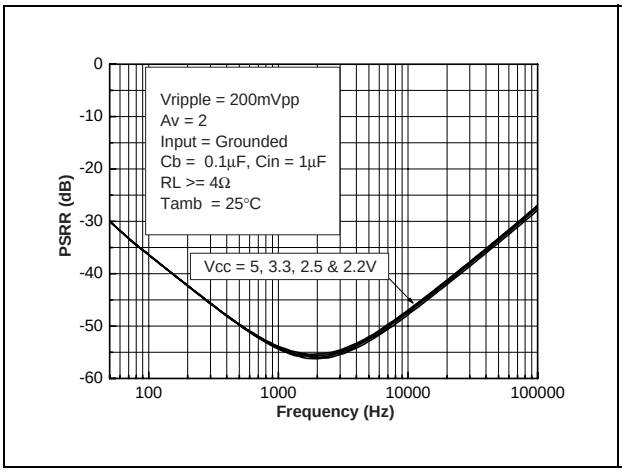


Figure 13. PSRR vs. power supply

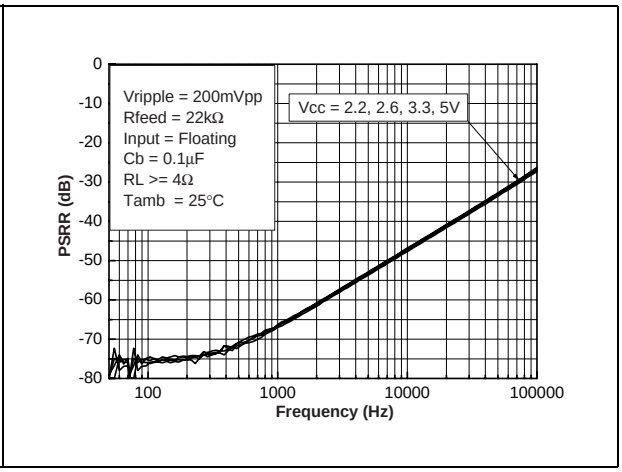


Figure 14. PSRR vs. DC output voltage

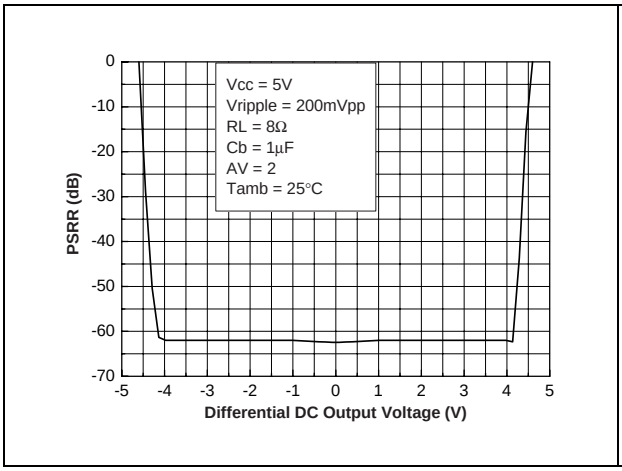


Figure 15. PSRR vs. DC output voltage

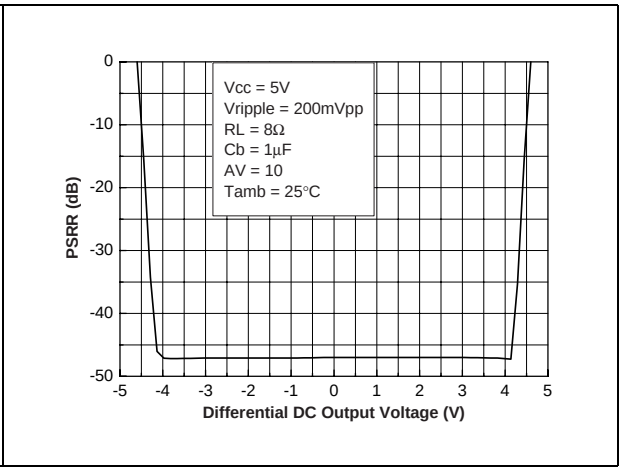


Figure 16. PSRR vs. DC output voltage

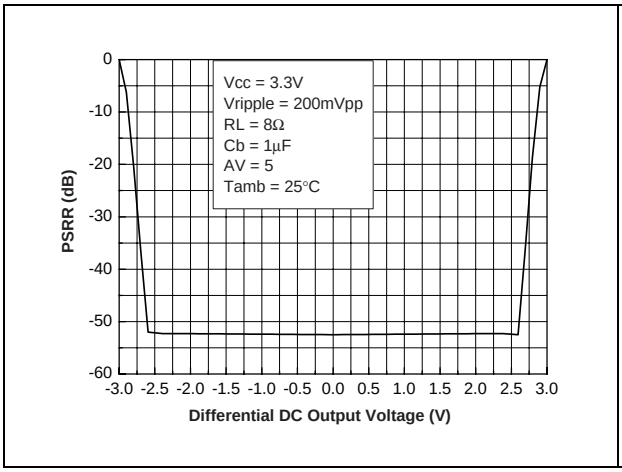


Figure 17. PSRR vs. DC output voltage

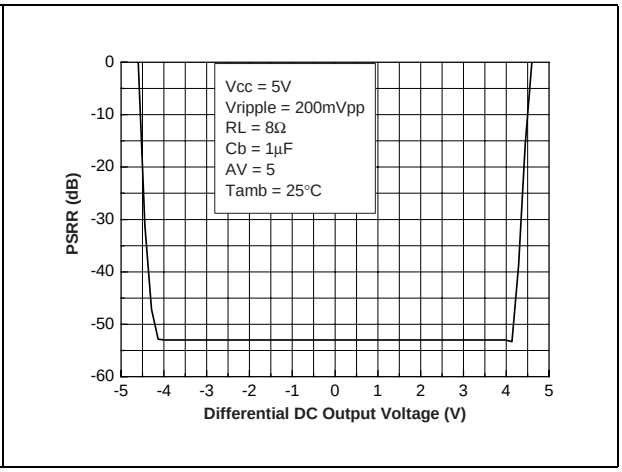


Figure 18. PSRR vs. DC output voltage

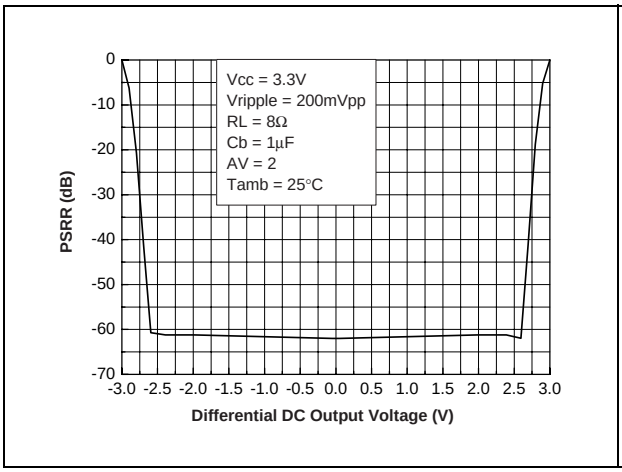


Figure 19. PSRR vs. DC output voltage

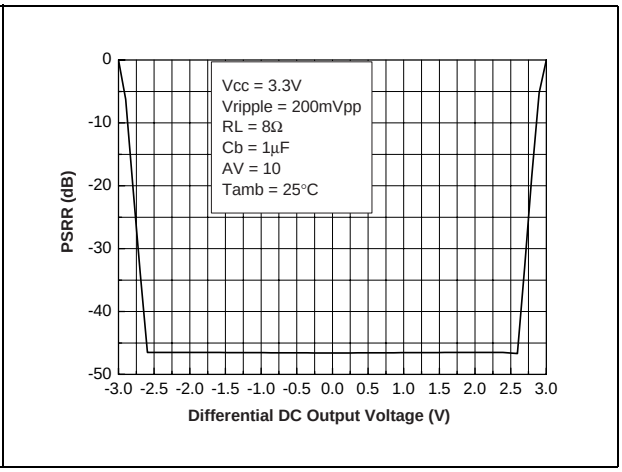


Figure 20. PSRR vs. DC output voltage

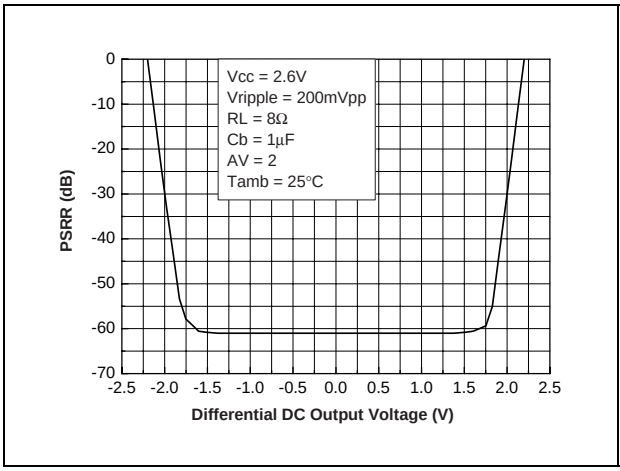


Figure 21. PSRR vs. DC output voltage

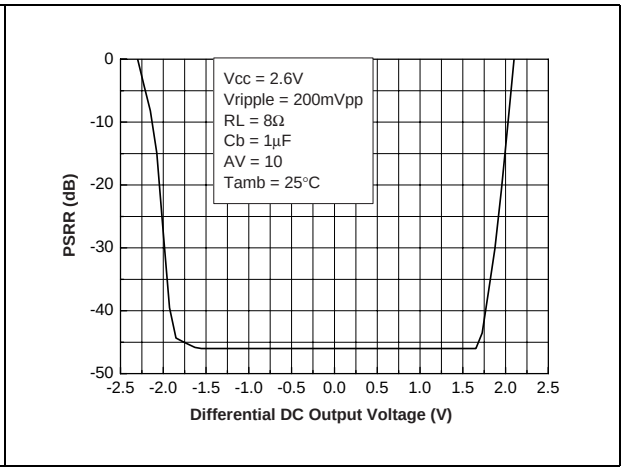


Figure 22. Output power vs. power supply voltage

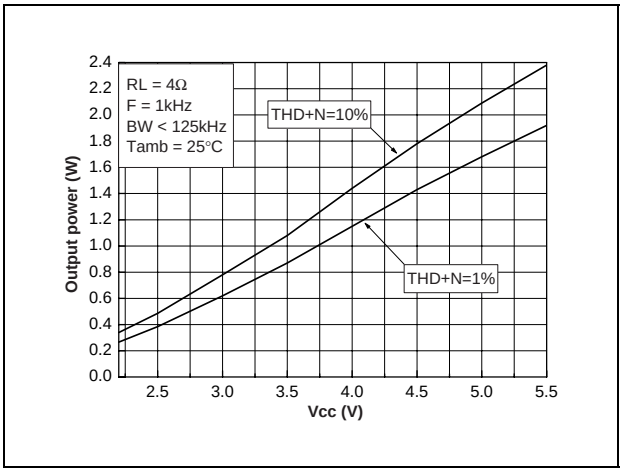


Figure 23. PSRR vs. DC output voltage

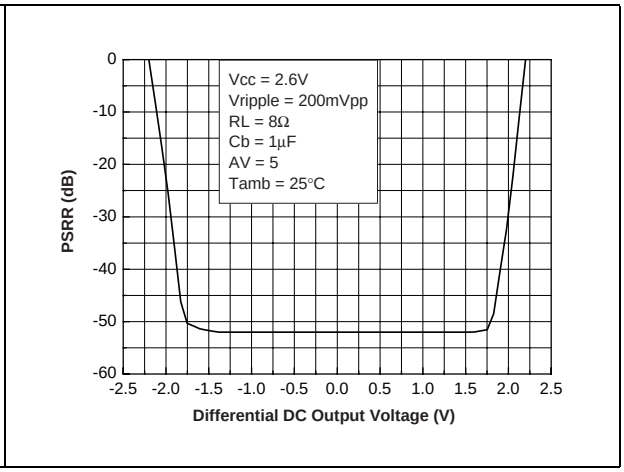


Figure 24. PSRR at F = 217 Hz vs. bypass capacitor

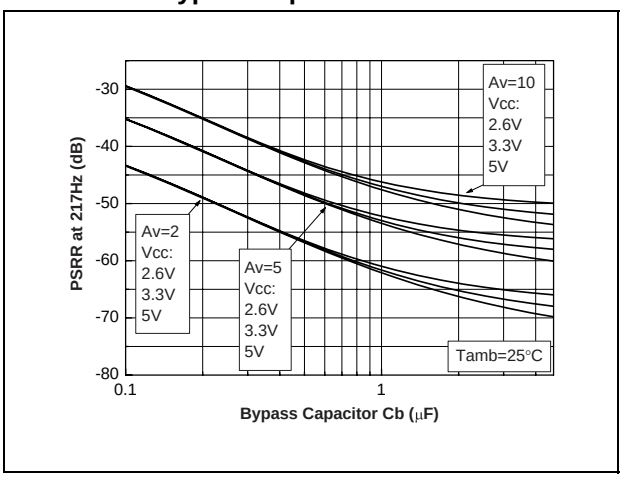


Figure 25. Output power vs. power supply voltage

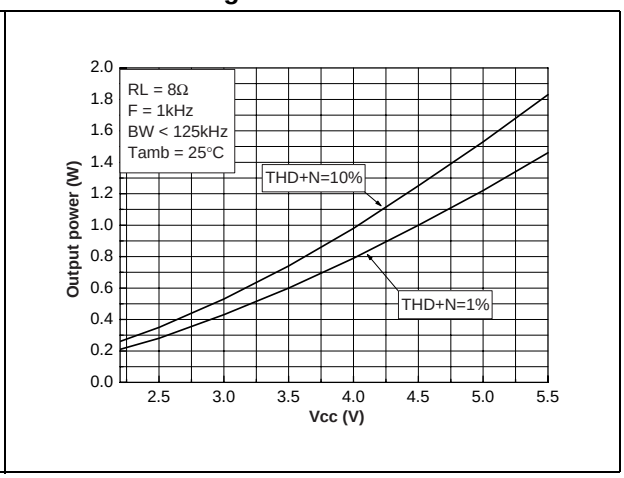


Figure 26. Output power vs. power supply voltage

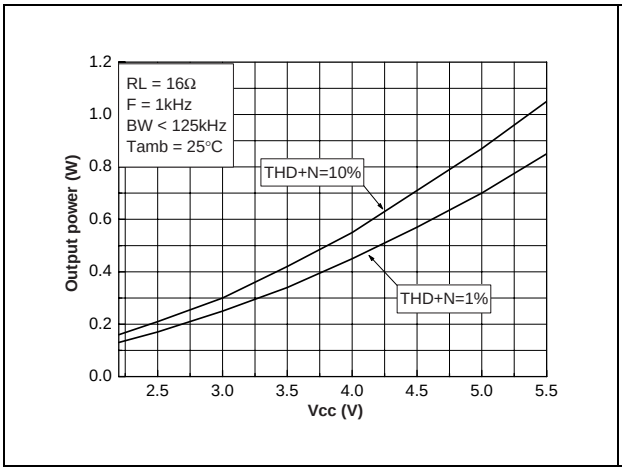


Figure 27. Output power vs. load resistor

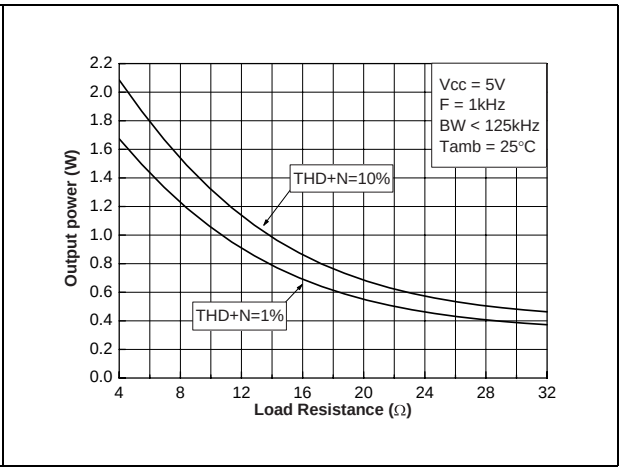


Figure 28. Output power vs. load resistor

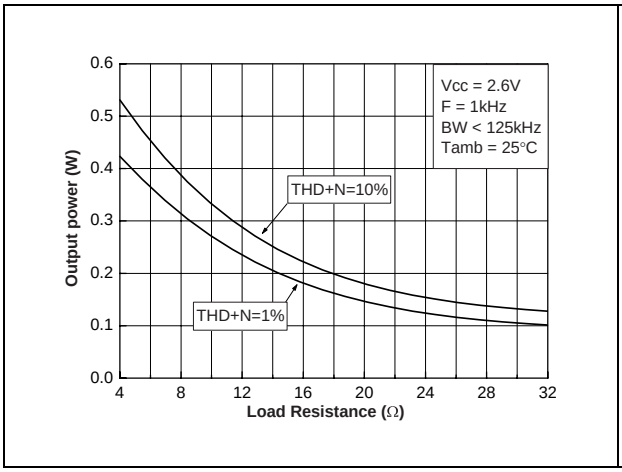


Figure 29. Output power vs. power supply voltage

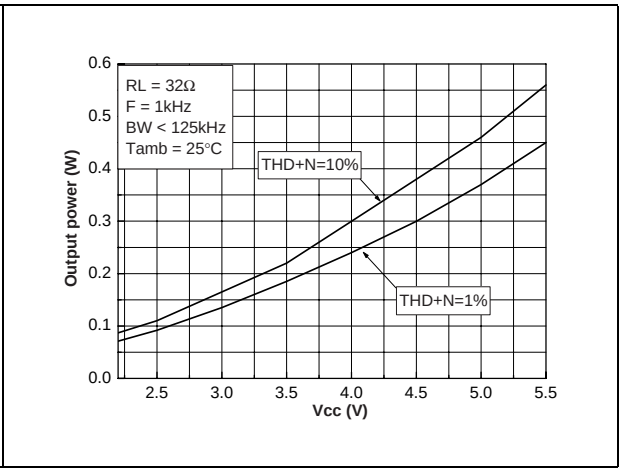


Figure 30. Output power vs. load resistor

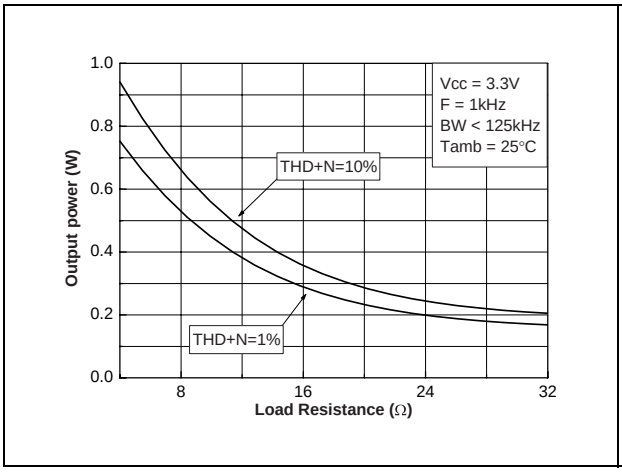


Figure 31. Power dissipation vs. P_{out}

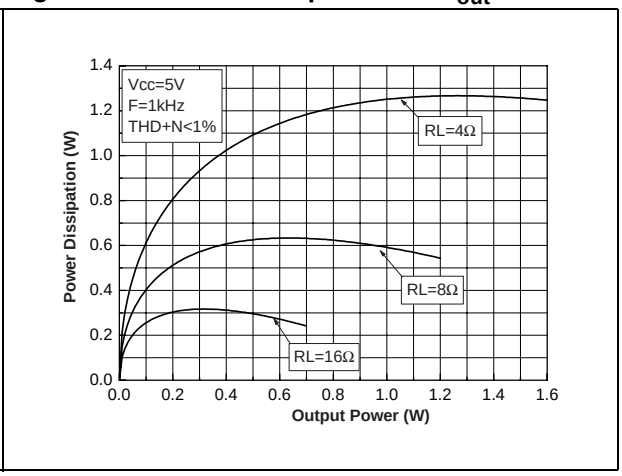


Figure 32. Power dissipation vs. P_{out}

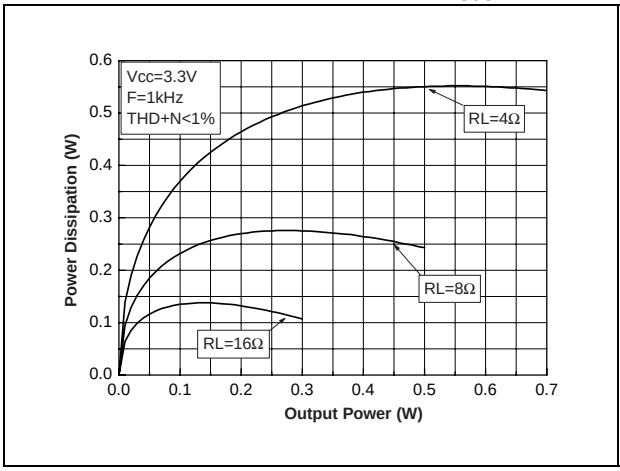


Figure 33. Power derating curves

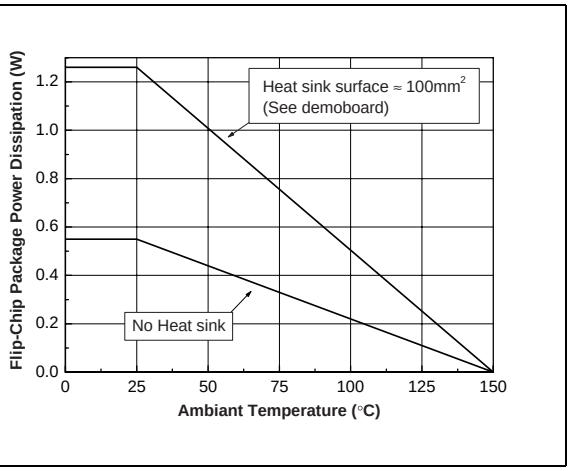


Figure 34. Clipping voltage vs. power supply voltage and load resistor

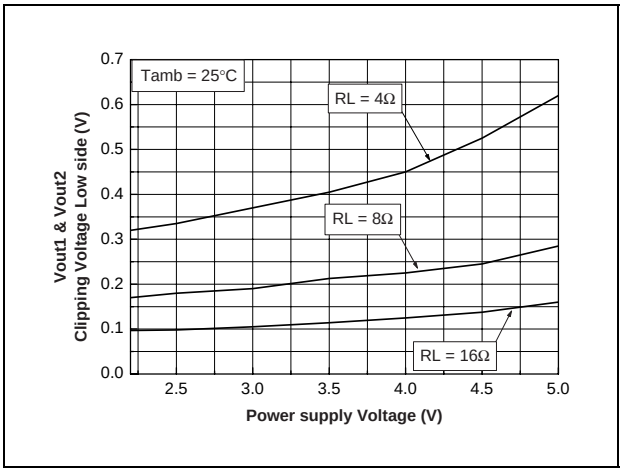


Figure 35. Power dissipation vs. P_{out}

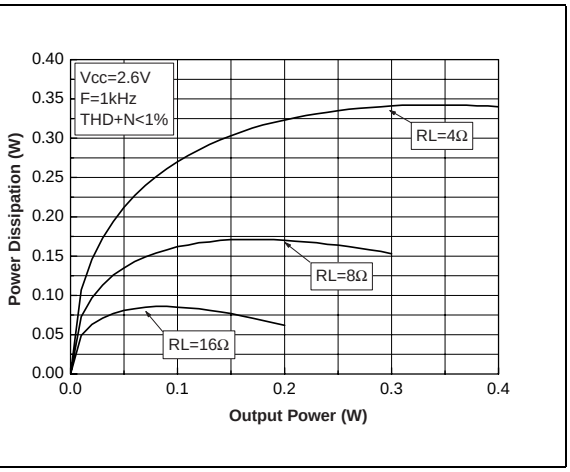


Figure 36. Clipping voltage vs. power supply voltage and load resistor

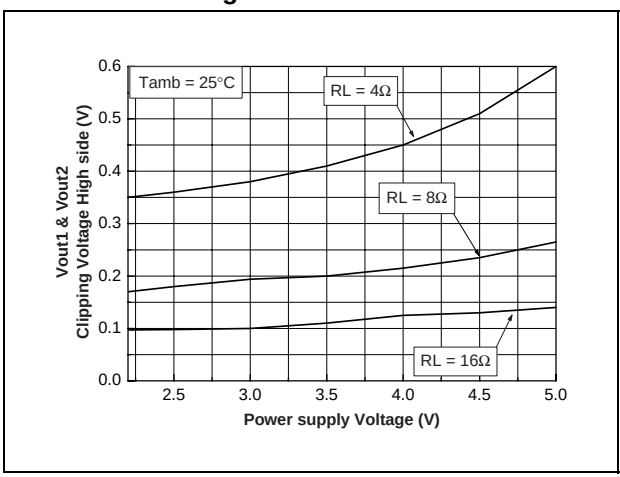


Figure 37. Current consumption vs. power supply voltage

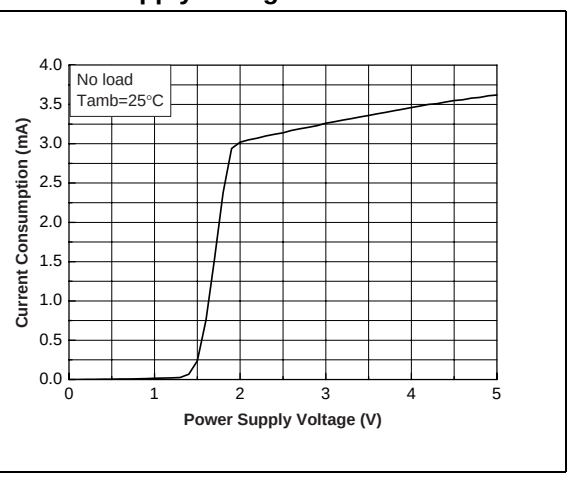


Figure 38. Current consumption vs. standby voltage @ V_{CC} = 5V

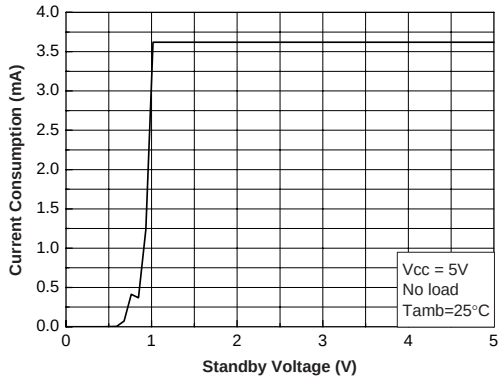


Figure 39. Current consumption vs. standby voltage @ V_{CC} = 2.6V

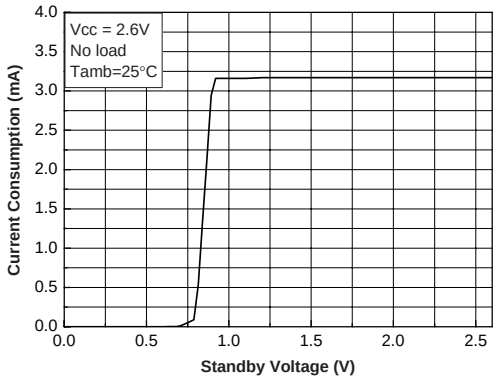


Figure 40. THD + N vs. output power

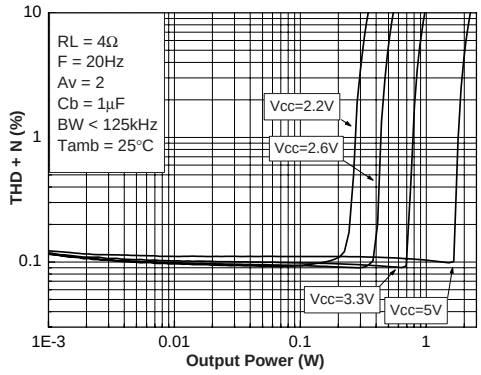


Figure 41. Current consumption vs. standby voltage @ V_{CC} = 3.3V

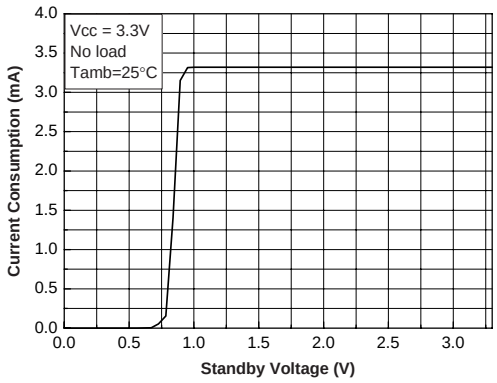


Figure 42. Current consumption vs. standby voltage @ V_{CC} = 2.2V

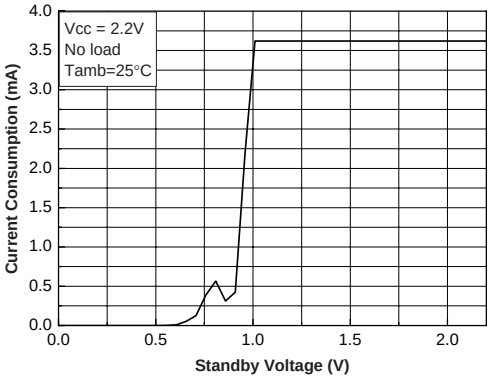


Figure 43. THD + N vs. output power

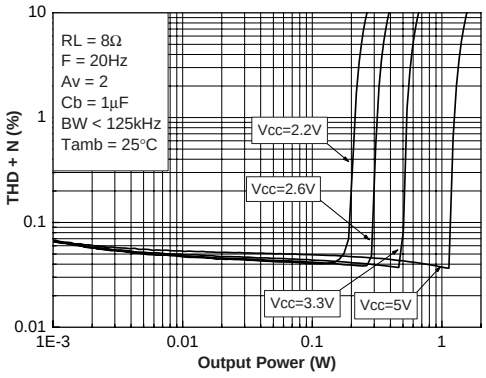


Figure 44. THD + N vs. output power

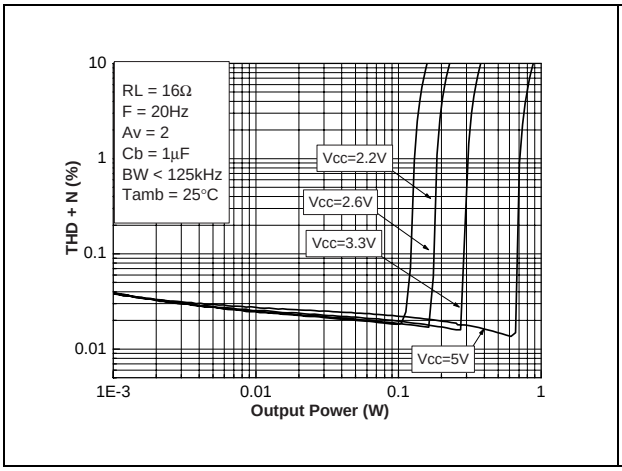


Figure 45. THD + N vs. output power

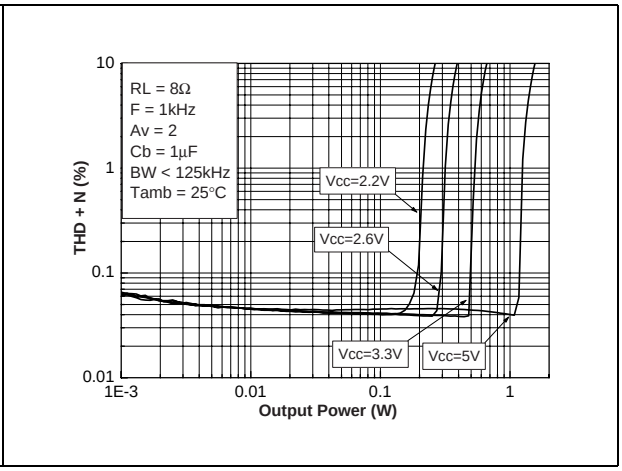


Figure 46. THD + N vs. output power

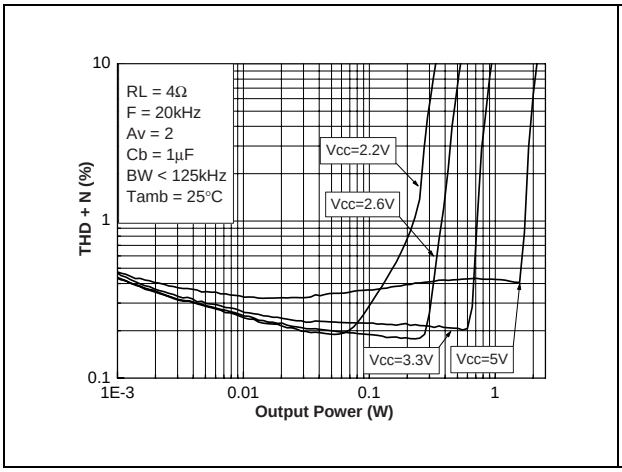


Figure 47. THD + N vs. output power

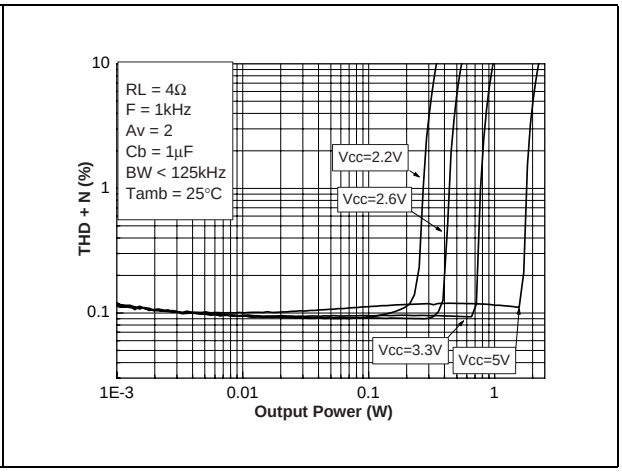


Figure 48. THD + N vs. output power

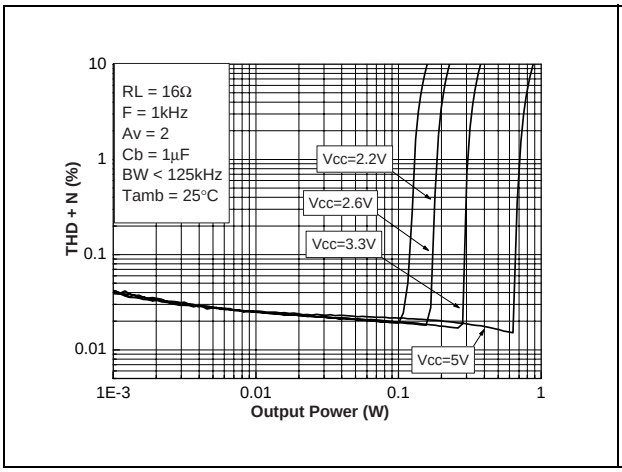


Figure 49. THD + N vs. output power

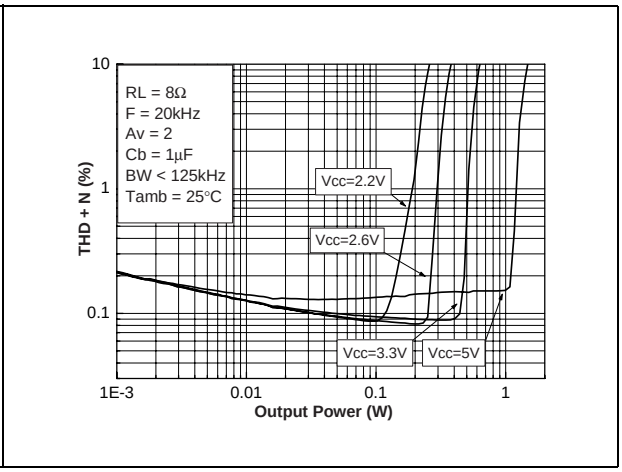


Figure 50. THD + N vs. output power

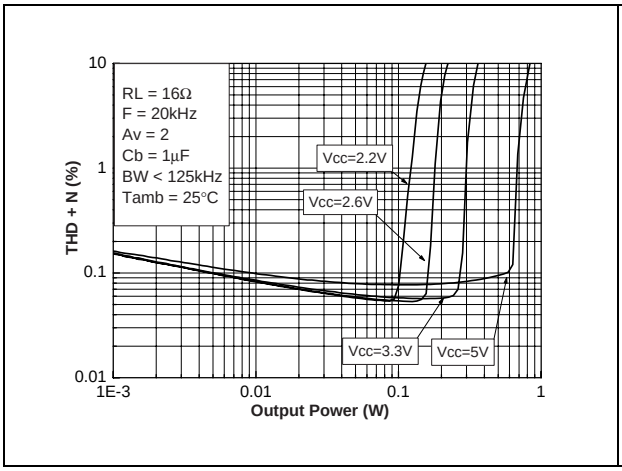


Figure 51. THD + N vs. frequency

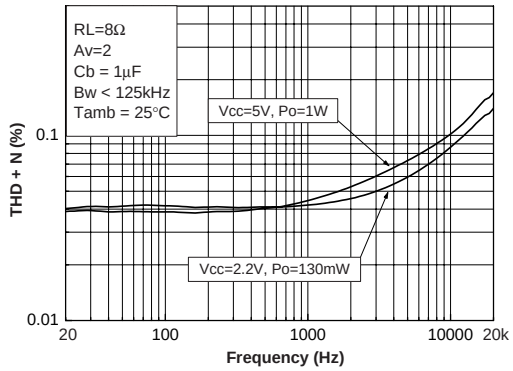


Figure 52. SNR vs. power supply with unweighted filter (20Hz to 20kHz)

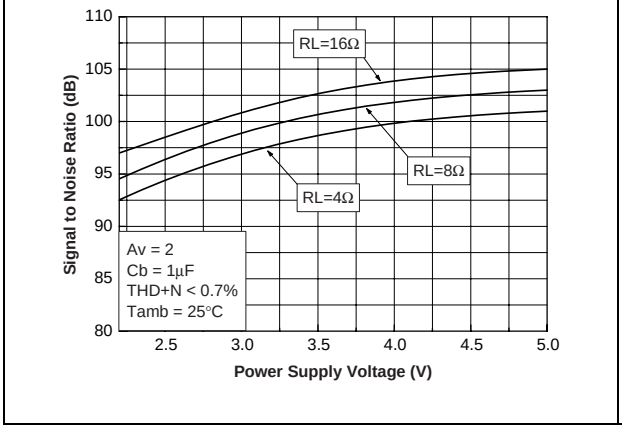


Figure 53. THD + N vs. frequency

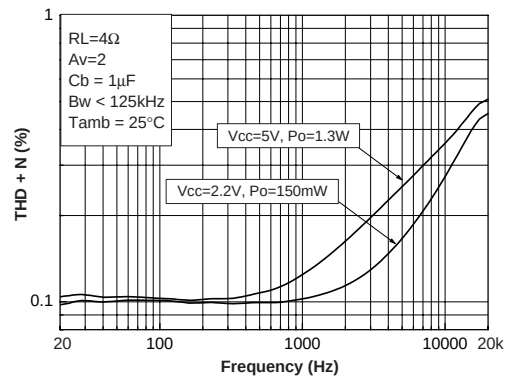


Figure 54. THD + N vs. frequency

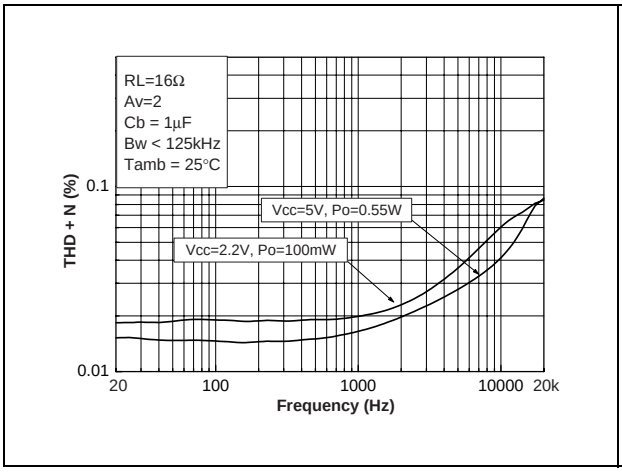


Figure 55. SNR vs. power supply with unweighted filter (20Hz to 20kHz)

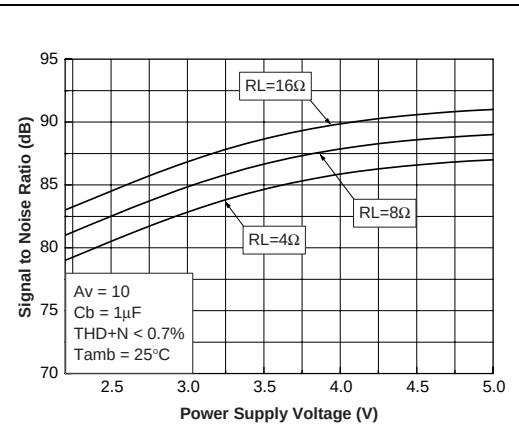


Figure 56. Signal to noise ratio vs. power supply with a weighted filter

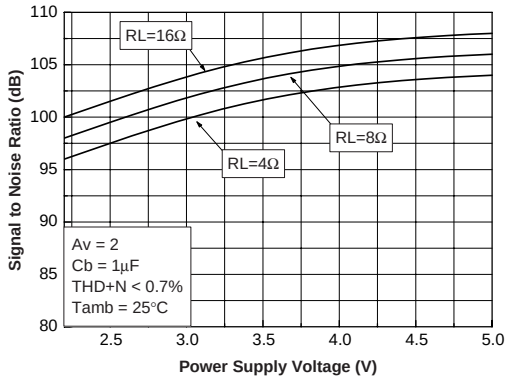


Figure 57. Output noise voltage device ON

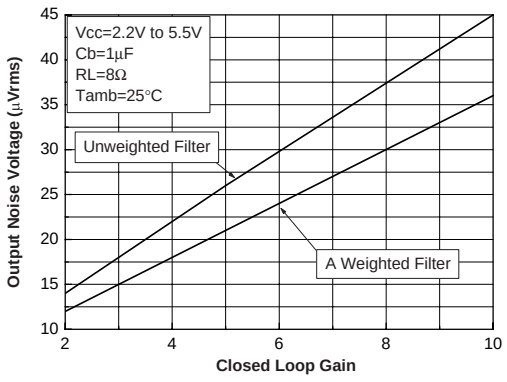


Figure 58. Signal to noise ratio vs. power supply with a weighted filter

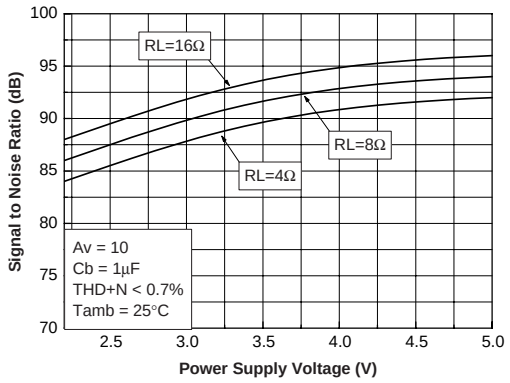
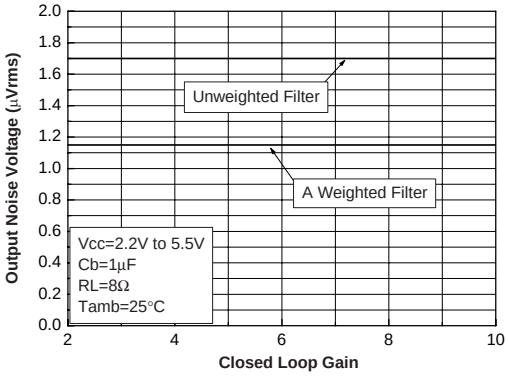


Figure 59. Output noise voltage device in Standby



5 Application information

5.1 BTL configuration principle

The TS4990 is a monolithic power amplifier with a BTL output type. BTL (bridge tied load) means that each end of the load is connected to two single-ended output amplifiers. Thus, we have:

Single-ended output 1 = $V_{out1} = V_{out}$ (V)
Single ended output 2 = $V_{out2} = -V_{out}$ (V)
and $V_{out1} - V_{out2} = 2V_{out}$ (V)

The output power is:

$$P_{out} = \frac{(2V_{out_{RMS}})^2}{R_L}$$

For the same power supply voltage, the output power in BTL configuration is four times higher than the output power in single ended configuration.

5.2 Gain in a typical application schematic

The typical application schematic is shown in *Figure 1 on page 5*.

In the flat region (no C_{in} effect), the output voltage of the first stage is (in Volts):

$$V_{out1} = (-V_{in})\frac{R_{feed}}{R_{in}}$$

For the second stage: $V_{out2} = -V_{out1}$ (V)

The differential output voltage is (in Volts):

$$V_{out2} - V_{out1} = 2V_{in}\frac{R_{feed}}{R_{in}}$$

The differential gain named gain (G_v) for more convenient usage is:

$$G_v = \frac{V_{out2} - V_{out1}}{V_{in}} = 2\frac{R_{feed}}{R_{in}}$$

V_{out2} is in phase with V_{in} and V_{out1} is phased 180° with V_{in}. This means that the positive terminal of the loudspeaker should be connected to V_{out2} and the negative to V_{out1}.

5.3 Low and high frequency response

In the low frequency region, C_{in} starts to have an effect. C_{in} forms with R_{in} a high-pass filter with a -3dB cut-off frequency. F_{CL} is in Hz.

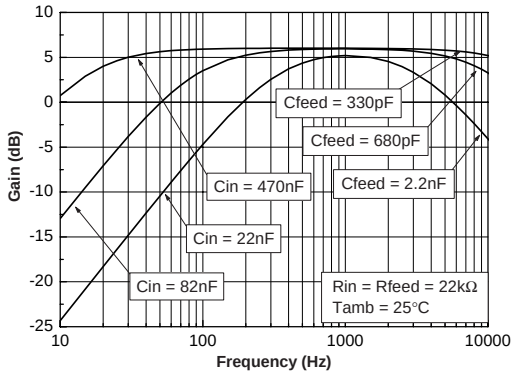
$$F_{CL} = \frac{1}{2\pi R_{in} C_{in}}$$

In the high frequency region, you can limit the bandwidth by adding a capacitor (C_{feed}) in parallel with R_{feed}. It forms a low-pass filter with a -3dB cut-off frequency. F_{CH} is in Hz.

$$F_{CH} = \frac{1}{2\pi R_{feed} C_{feed}}$$

The following graph shows an example of C_{in} and C_{feed} influence.

Figure 60. Frequency response gain vs. C_{in} & C_{feed}



5.4 Power dissipation and efficiency

Hypotheses:

- Load voltage and current are sinusoidal (V_{out} and I_{out}).
- Supply voltage is a pure DC source (V_{cc}).

Regarding the load we have:

$$V_{out} = V_{PEAK} \sin\omega t \quad (V)$$

and

$$I_{out} = \frac{V_{out}}{R_L} \quad (A)$$

and

$$P_{out} = \frac{V_{PEAK}^{2}}{2R_L} \quad (W)$$

Therefore, the average current delivered by the supply voltage is:

$$I_{CC_{AVG}} = 2\frac{V_{PEAK}}{\pi R_L} \quad (A)$$

The power delivered by the supply voltage is:

$$P_{supply} = V_{CC} \cdot I_{CC_{AVG}} \quad (W)$$

Then, the **power dissipated by each amplifier** is:

$$P_{diss} = P_{supply} - P_{out} \ (W)$$

$$P_{diss} = \frac{2\sqrt{2}V_{CC}}{\pi\sqrt{R_L}}\sqrt{P_{out}} - P_{out}$$

and the maximum value is obtained when:

$$\frac{\delta P_{diss}}{\delta P_{out}} = 0$$

and its value is:

$$P_{diss_{max}} = \frac{2V_{CC}^2}{\pi^2 R_L} \quad (W)$$

Note: This maximum value is only dependent on power supply voltage and load values.

The **efficiency** is the ratio between the output power and the power supply:

$$\eta = \frac{P_{out}}{P_{supply}} = \frac{\pi V_{PEAK}}{4V_{CC}}$$

The maximum theoretical value is reached when $V_{PEAK} = V_{CC}$, so:

$$\frac{\pi}{4} = 78.5\%$$

5.5 Decoupling of the circuit

Two capacitors are needed to correctly bypass the TS4990: a power supply bypass capacitor C_s and a bias voltage bypass capacitor C_b.

C_s has particular influence on the THD+N in the high frequency region (above 7kHz) and an indirect influence on power supply disturbances. With a value for C_s of 1µF, you can expect THD+N levels similar to those shown in the datasheet.

In the high frequency region, if C_s is lower than 1µF, it increases THD+N and disturbances on the power supply rail are less filtered.

On the other hand, if C_s is higher than 1µF, those disturbances on the power supply rail are more filtered.

C_b has an influence on THD+N at lower frequencies, but its function is critical to the final result of PSRR (with input grounded and in the lower frequency region).

If C_b is lower than 1µF, THD+N increases at lower frequencies and PSRR worsens.

If C_b is higher than 1µF, the benefit on THD+N at lower frequencies is small, but the benefit to PSRR is substantial.

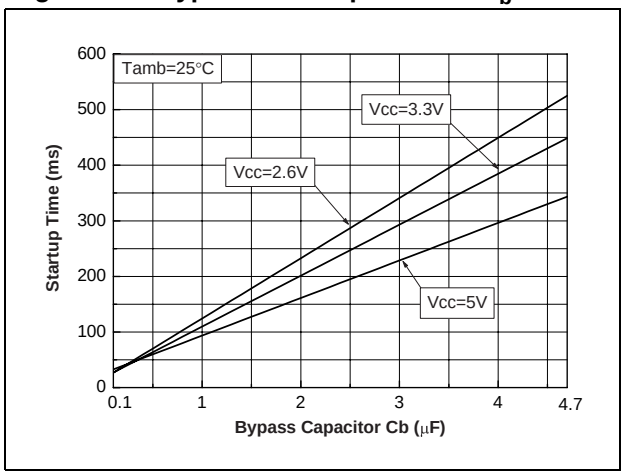
Note that C_{in} has a non-negligible effect on PSRR at lower frequencies. The lower the value of C_{in}, the higher the PSRR.

5.6 Wake-up time(t_{WU})

When the standby is released to put the device ON, the bypass capacitor C_b will not be charged immediately. As C_b is directly linked to the bias of the amplifier, the bias will not work properly until the C_b voltage is correct. The time to reach this voltage is called wake-up time or t_{WU} and specified in the electrical characteristics table with C_b = 1µF.

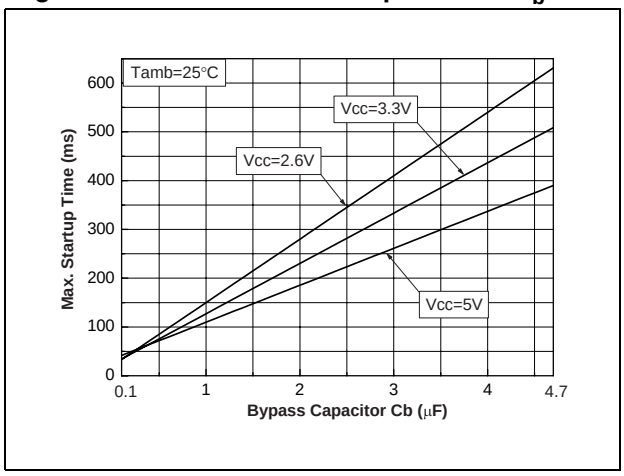
If C_b has a value other than 1µF, please refer to the graph in *Figure 60 on page 21* to establish the wake-up time value.

Figure 61. Typical wake-up time vs. C_b



Due to process tolerances, the maximum value of wake-up time can be established by the graph in *Figure 62*.

Figure 62. Maximum wake-up time vs. C_b



Note: The bypass capacitor C_b also has a typical tolerance of +/-20%. To calculate the wake-up time with this tolerance, refer to the graph above (considering for example for C_b=1µF in the range of 0.8µF≤1µF≤1.2µF).

5.7 Shutdown time

When the standby command is set, the time required to put the two output stages in high impedance and the internal circuitry in shutdown mode is a few microseconds.

In shutdown mode, Bypass pin and Vin- pin are short-circuited to ground by internal switches. This allows a quick discharge of C_b and C_{in} capacitors.

5.8 Pop performance

Pop performance is intimately linked with the size of the input capacitor C_{in} and the bias voltage bypass capacitor C_b.

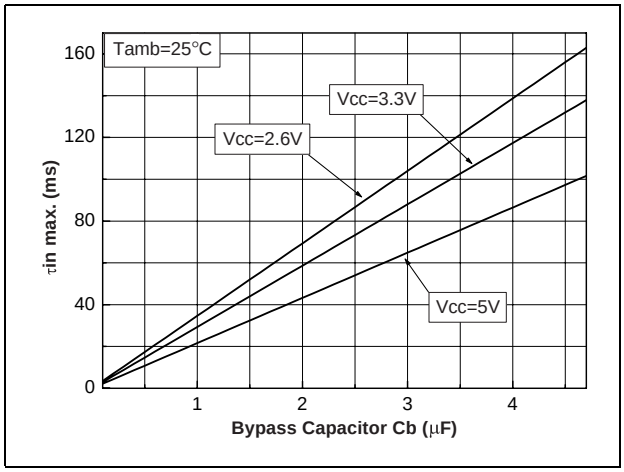
The size of C_{in} is dependent on the lower cut-off frequency and PSRR values requested. The size of C_b is dependent on THD+N and PSRR values requested at lower frequencies.

Moreover, C_b determines the speed with which the amplifier turns ON. In order to reach near zero pop and click, the equivalent input constant time,

$\tau_{in} = (R_{in} + 2k\Omega) \times C_{in}$ (s) with $R_{in} \geq 5k\Omega$

must not reach the τ_{in} maximum value as indicated in *Figure 63* below.

Figure 63. τ_{in} max. versus bypass capacitor



By following the previous rules, the TS4990 can reach near zero pop and click even with high gains such as 20 dB.

Example:

With R_{in} = 22 kΩ and a 20 Hz, -3 dB low cut-off frequency, C_{in} = 361 nF. So, C_{in} = 390 nF with standard value which gives a lower cut-off frequency equal to 18.5 Hz. In this case, (R_{in} + 2kΩ) x C_{in} = 9.36ms. When referring to the previous graph, if C_b = 1 µF and V_{CC} = 5 V, we read 20 ms max. This value is twice as high as our current value, thus we can state that pop and click will be reduced to its lowest value.

Minimizing both C_{in} and the gain benefits both the pop phenomena, and the cost and size of the application.

5.9 Application example: differential input, BTL power amplifier

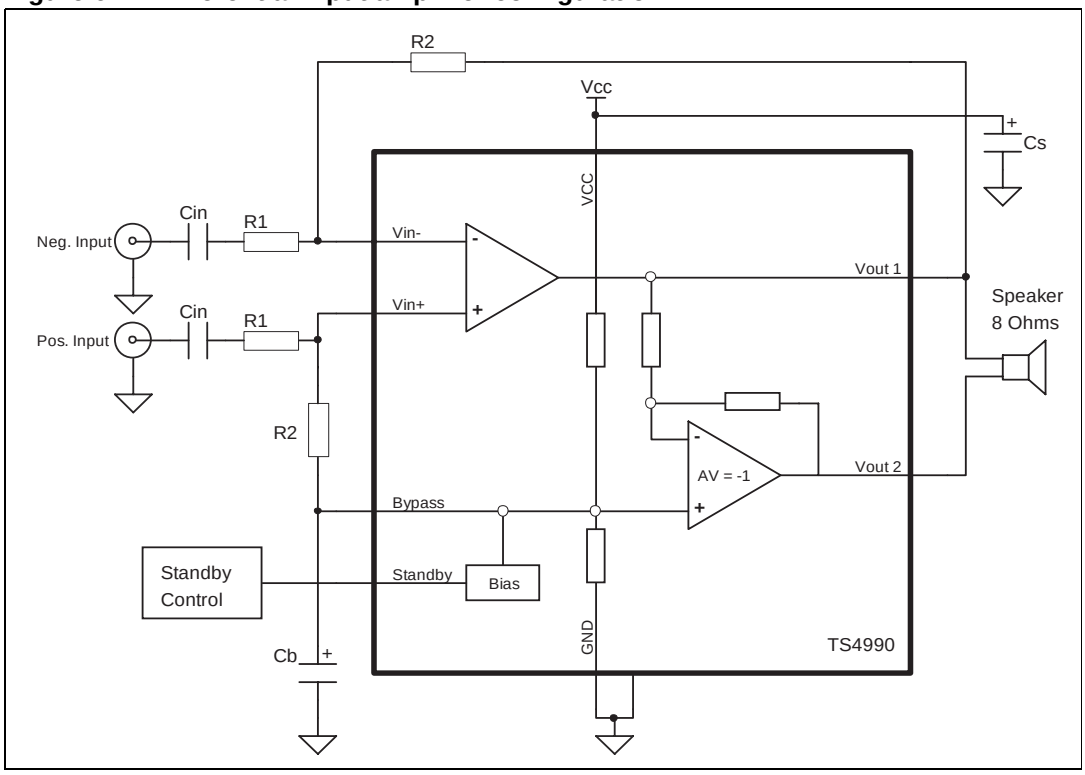
The schematic in *Figure 64* shows how to design the TS4990 to work in a differential input mode.

The gain of the amplifier is:

$$G_{VDIFF} = 2\frac{R_2}{R_1}$$

In order to reach the optimal performance of the differential function, R_1 and R_2 should be matched at 1% max.

Figure 64. Differential input amplifier configuration



The input capacitor C_{in} can be calculated by the following formula using the -3dB lower frequency required. (F_L is the lower frequency required).

$$C_{in} \approx \frac{1}{2\pi R_1 F_L} \quad (F)$$

Note: This formula is true only if:

$$F_{CB} = \frac{1}{2\pi(R_1 + R_2)C_B} \quad (Hz)$$

is 5 times lower than F_L.

Example bill of materials

The following bill of materials is for the example of a differential amplifier with a gain of 2 and a -3dB lower cut-off frequency of about 80Hz.

Designator pin	Functional description
R_1	20k / 1%
R_2	20k / 1%
C_{in}	100nF
C_b=C_s	1µF
U1	TS4990

6 Package mechanical data

In order to meet environmental requirements, STMicroelectronics offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an STMicroelectronics trademark. ECOPACK specifications are available at: www.st.com.

6.1 Flip-chip package

Figure 65. Flip-chip silhouette and pin-out (top view)

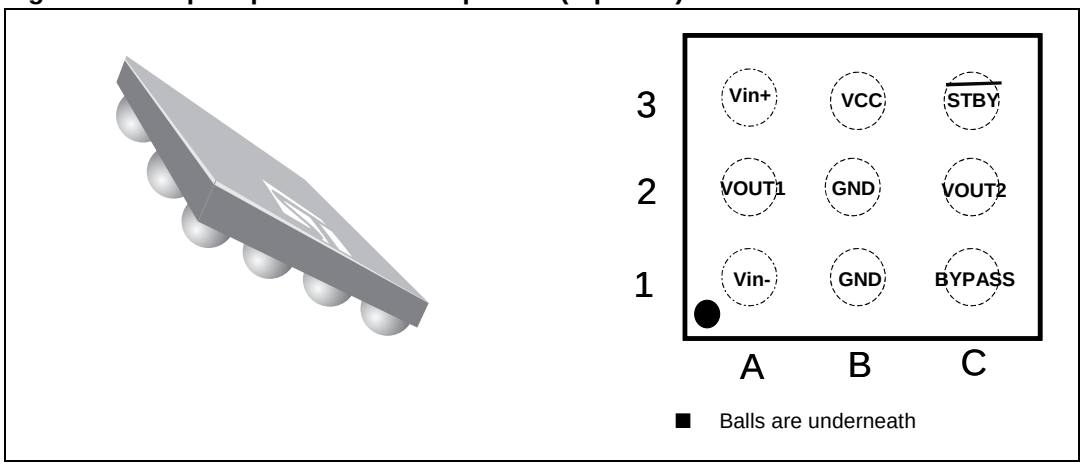


Figure 66. Marking (top view)

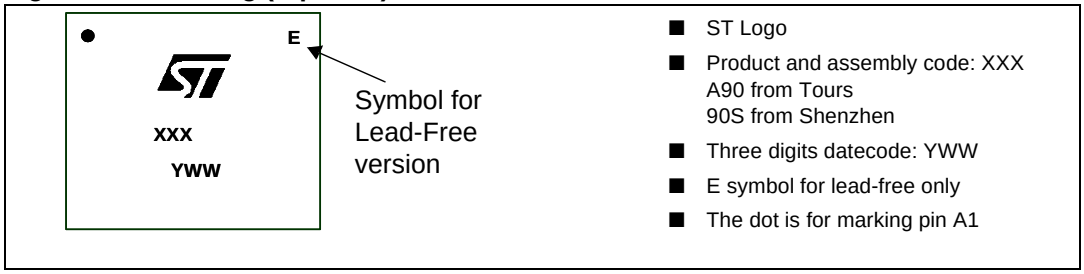
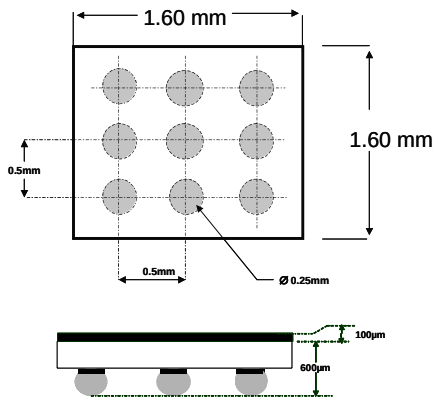


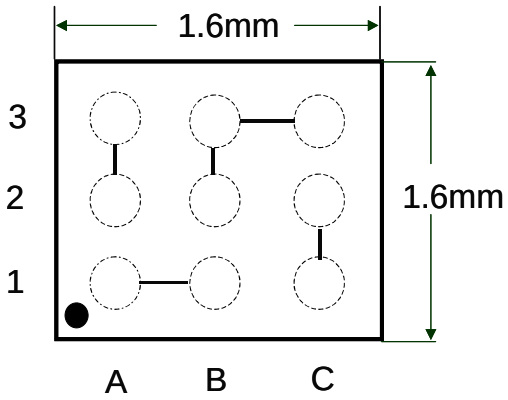
Figure 67. Package mechanical data for 9-bump flip-chip



- Die size: **1.60 x 1.60 mm ±30µm**
- Die height (including bumps): **600µm**
- Bump diameter: **315µm ±50µm**
- Bump diameter before reflow: **300µm ±10µm**
- Bump height: **250µm ±40µm**
- Die height: **350µm ±20µm**
- Pitch: **500µm ±50µm**
- Coplanarity: **50µm max**
- * Back coating height: **100µm ±10µm**

* Optional

Figure 68. Daisy chain mechanical data



Remarks:

The daisy chain sample features two by two pin connections. The schematic above illustrates the way pins connect to each other. This sample is used to test continuity on your board. Your PCB needs to be designed the opposite way, so that pins that are unconnected in the daisy chain sample, are connected on your PCB. If you do this, by simply connecting a Ohmmeter between pin A1 and pin A3, the soldering process continuity can be tested.

Table 7. Order codes

Part number	Temperature range	Package	Marking
		J	
TSDC05IJT	-40, +85°C	•	DC3
TSDC05EIJT(1)		•	DC3

1. Lead free Daisy Chain part number

Figure 69. TS4990 footprint recommendations

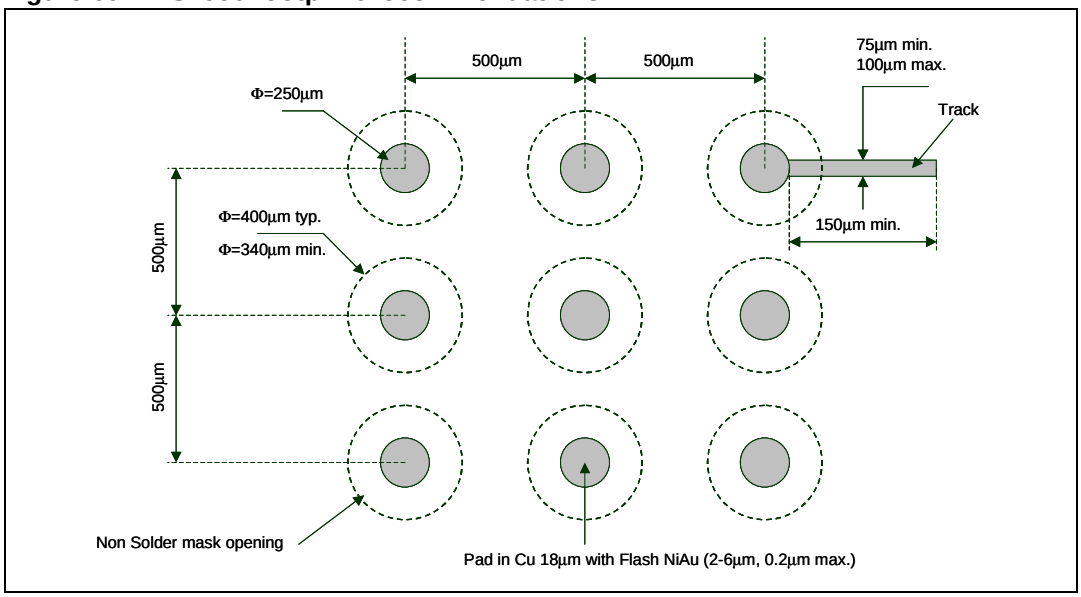
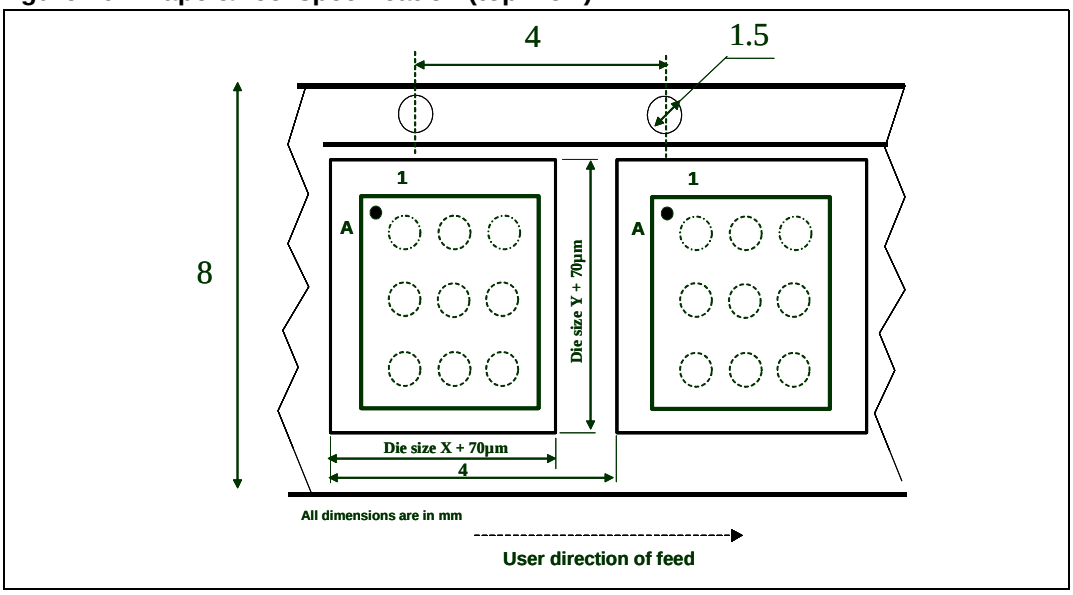


Figure 70. Tape & reel specification (top view)

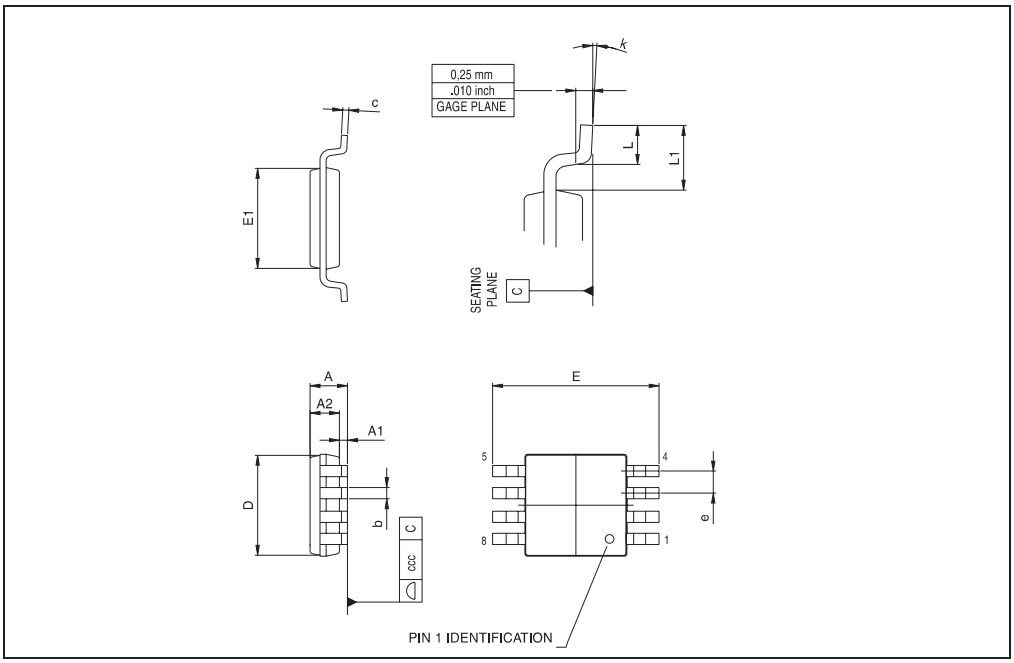


Device orientation

The devices are oriented in the carrier pocket with pin number A1 adjacent to the sprocket holes.

6.2 MiniSO-8 package

miniSO-8 MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.1			0.043
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.78	0.86	0.94	0.031	0.031	0.037
b	0.25	0.33	0.40	0.010	0.13	0.013
c	0.13	0.18	0.23	0.005	0.007	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	4.75	4.90	5.05	0.187	0.193	0.199
E1	2.90	3.00	3.10	.0114	0.118	0.122
e		0.65			0.026	
K	0°		6°	0°		6°
L	0.40	0.55	0.70	0.016	0.022	0.028
L1			0.10			0.004

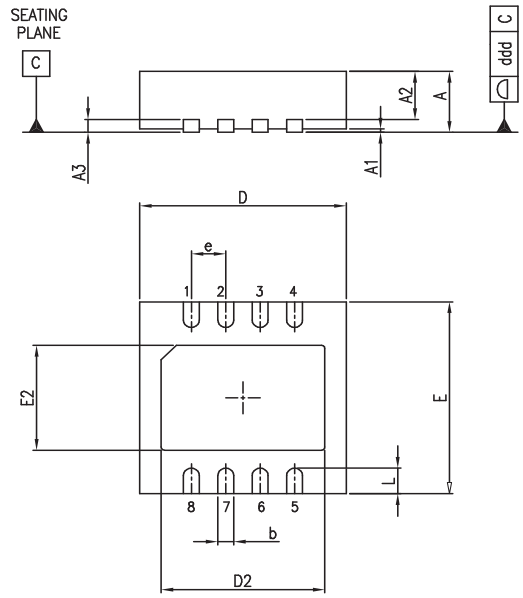


6.3 DFN8 package

Note: DFN8 exposed pad (e2 x d2) is connected to pin number 7.
For enhanced thermal performance, the exposed pad must be soldered to a copper area on the PCB, acting as heatsink. This copper area can be electrically connected to pin7 or left floating.

DFN8 (3x3) MECHANICAL DATA

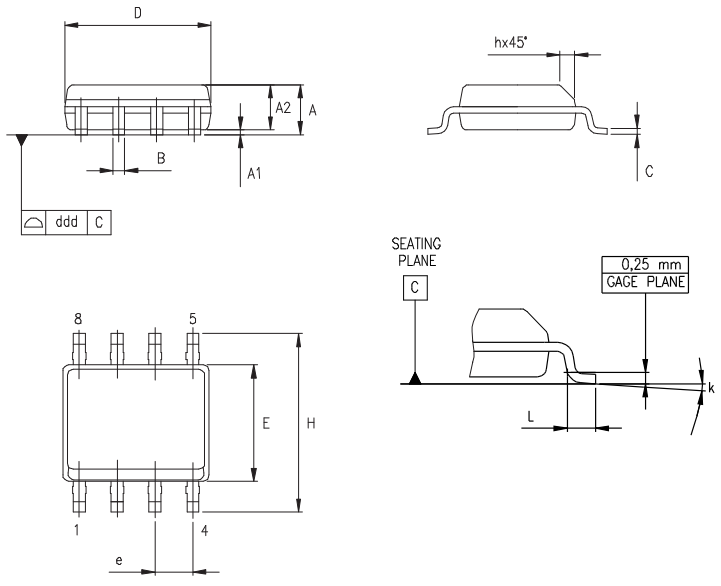
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	0.80	0.90	1.00	31.5	35.4	39.4
A1		0.02	0.05		0.8	2.0
A2		0.70			27.6	
A3		0.20			7.9	
b	0.18	0.23	0.30	7.1	9.1	11.8
D	2.875	3.00	3.125		118.1	
D2	2.23	2.38	2.48	87.8	93.7	97.7
E	2.875	3.00	3.125		118.1	
E2	1.49	1.64	1.74	58.7	64.6	68.5
e		0.50			19.7	
L	0.30	0.40	0.50	11.8	15.7	19.7



6.4 SO-8 package

SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.04		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D	4.80		5.00	0.189		0.197
E	3.80		4.00	0.150		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	8° (max.)					
ddd			0.1			0.04



0016023/C

7 Revision history

Table 8. Document revision history

Date	Revision	Changes
Jul-2002	1	First release.
Sep-2003	2	Update mechanical data.
Oct-2004	3	Order code for back coating on flip-chip.
Apr-2005	4	Typography error on page 1: Mini-SO-8 pin connection.
May-2005	5	New marking for assembly code plant.
Jul-2005	6	Error on *Table 3 on page 6*. Parameters in wrong column.
Sep-2005	7	Updated mechanical coplanarity data to 50µm (instead of 60µm) (see *Figure 67 on page 25*).
Mar-2006	8	SO-8 package inserted in the datasheet.
21-Jul-2006	9	Update of *Figure 66 on page 27*. Disclaimer update.

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