TSX561, TSX561A

Micropower, wide bandwidth (900 kHz) 16 V CMOS op amps

Datasheet - production data

Features

- Low power consumption: 235 µA typ. at 5 V
- Supply voltage: 3 V to 16 V
- Gain bandwidth product: 900 kHz typ.
- Low offset voltage:

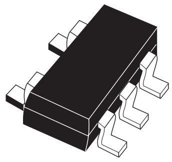
  600 µV max. for “A” version,
  1 mV max. for standard version
- Low input bias current: 1 pA typ.
- High tolerance to ESD: 4 kV
- Wide temperature range: -40 to +125 °C
- Automotive qualification
- Package: SOT23-5

Applications

- Industrial signal conditioning
- Automotive signal conditioning
- Active filtering
- Medical instrumentation
- High impedance sensors

Description

The TSX56x series of operational amplifiers offers low voltage operation and rail-to-rail input and output. The TSX561 device is the single version, the TSX562 device the dual version and the TSX564 device the quad version, with pinouts compatible with industry standards.
The TSX56x series offers an outstanding speed/power consumption ratio, 900 kHz gain bandwidth product while consuming only 250 µA at 16 V. The devices are housed in the smallest industrial packages.



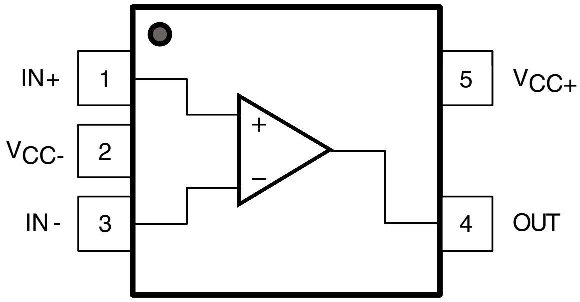
SOT23-5

These features make the TSX56x family ideal for sensor interfaces and industrial signal conditioning. The wide temperature range and high ESD tolerance ease use in harsh automotive applications.

Contents

1 Package pin connections

Figure 1. Pin connections for SOT23-5 (top view)



2 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings (AMR)

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage[1]	18	V
V_{id}	Differential input voltage[2]	$\pm V_{CC}$	V
V_{in}	Input voltage[3]	V_{CC-} - 0.2 to V_{CC+}+ 0.2	V
I_{in}	Input current[4]	10	mA
T_{stg}	Storage temperature	-65 to +150	°C
R_{thja}	Thermal resistance junction-to-ambient[5],[6] SOT23-5	250	°C/W
T_j	Maximum junction temperature	150	°C
ESD	HBM: human body model[7]	4	kV
	MM: machine model[8]	200	V
	CDM: charged device model[9]	1.5	kV
	Latch-up immunity	200	mA

1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. V_{CC} - V_{in} must not exceed 18 V, V_{in} must not exceed 18 V.
4. Input current must be limited by a resistor in series with the inputs.
5. Short-circuits can cause excessive heating and destructive dissipation.
6. R_{th} are typical values.
7. Human body model: 100 pF discharged through a 1.5 kΩ resistor between two pins of the device, done for all couples of pin combinations with other pins floating.
8. Machine model: a 200 pF cap is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω), done for all couples of pin combinations with other pins floating.
9. Charged device model: all pins plus package are charged together to the specified voltage and then discharged directly to ground.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	3 to 16	V
V_{icm}	Common mode input voltage range	V_{CC-} - 0.1 to V_{CC+} + 0.1	V
T_{oper}	Operating free air temperature range	-40 to +125	°C

3 Electrical characteristics

Table 3. Electrical characteristics at V_{CC+} = +3.3 V with V_{CC-} = 0 V, V_{icm} = $V_{CC}/2$, T_{amb} = 25 °C, and R_L=10 kΩ connected to $V_{CC}/2$ (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Offset voltage	TSX56xA, T = 25 °C			600	µV
		TSX56xA, -40 °C < T < 125 °C			1800	
		TSX56x, T = 25 °C			1	mV
		TSX56x, -40 °C < T < 125 °C			2.2	
$\Delta V_{io}/\Delta T$	Input offset voltage drift	-40 °C < T < 125 °C(1)		2	12	µV/°C
I_{io}	Input offset current (V_{out} = $V_{CC}/2$)	T = 25 °C		1	100(3)	pA
		-40 °C < T < 125 °C		1	200(3)	
I_{ib}	Input bias current (V_{out} = $V_{CC}/2$)	T = 25 °C		1	100(3)	pA
		-40 °C < T < 125 °C		1	200(3)	
CMR1	Common mode rejection ratio CMR = 20 log ($\Delta V_{ic}/\Delta V_{io}$) ($V_{ic}$ = -0.1 V to V_{CC}-1.5 V, V_{out} = $V_{CC}/2$, R_L > 1 MΩ)	T = 25 °C	63	80		dB
		-40 °C < T < 125 °C	59			
CMR2	Common mode rejection ratio CMR = 20 log ($\Delta V_{ic}/\Delta V_{io}$) ($V_{ic}$ = -0.1 V to V_{CC}+0.1 V, V_{out} = $V_{CC}/2$, R_L > 1 MΩ)	T = 25 °C	47	66		dB
		-40 °C < T < 125 °C	45			
A_{vd}	Large signal voltage gain (V_{out} = 0.5 V to (V_{CC} - 0.5 V), R_L > 1 MΩ)	T = 25 °C	85			dB
		-40 °C < T < 125 °C	83			
V_{OH}	High level output voltage (V_{OH} = V_{CC} - V_{out})	T = 25 °C			70	mV
		-40 °C < T < 125 °C			100	
V_{OL}	Low level output voltage	T = 25 °C			70	mV
		-40 °C < T < 125 °C			100	
I_{out}	I_{sink} (V_{out} = V_{CC})	T = 25 °C	4.3	5.3		mA
		-40 °C < T < 125 °C	2.5			
	I_{source} (V_{out} = 0 V)	T = 25 °C	3.3	4.3		mA
		-40 °C < T < 125 °C	2.5			
I_{CC}	Supply current (per channel, V_{out} = $V_{CC}/2$, R_L > 1 MΩ)	T = 25 °C		220	300	µA
		-40 °C < T < 125 °C			350	
AC performance						
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 100 pF	600	800		kHz
F_u	Unity gain frequency	R_L = 10 kΩ, C_L = 100 pF		690		kHz
Φ_m	Phase margin	R_L = 10 kΩ, C_L = 100 pF		55		degrees

Table 3. Electrical characteristics at V_{CC+} = +3.3 V with V_{CC-} = 0 V, V_{icm} = $V_{CC}/2$, T_{amb} = 25 °C, and R_L=10 kΩ connected to $V_{CC}/2$ (unless otherwise specified) (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
G_m	Gain margin	R_L = 10 kΩ, C_L = 100 pF		9		dB
SR	Slew rate	R_L = 10 kΩ, C_L = 100 pF, V_{out} = 0.5 V to V_{CC} - 0.5 V		1		V/µs
$\int e_n$	Low-frequency peak-to-peak input noise	Bandwidth: f = 0.1 to 10 Hz		16		μV_{pp}
e_n	Equivalent input noise voltage density	f = 1 kHz f = 10 kHz		55 29		$\frac{nV}{\sqrt{Hz}}$
THD+N	Total harmonic distortion + noise	Follower configuration, f_{in} = 1 kHz, R_L = 100 kΩ, V_{icm} = (V_{CC} -1.5 V)/2, BW = 22 kHz, V_{out} = 1 V_{pp}		0.004		%

Table 4. Electrical characteristics at V_{CC+} = +5 V with V_{CC-} = 0 V, V_{icm} = $V_{CC}/2$, T_{amb} = 25 °C, and R_L = 10 kΩ connected to $V_{CC}/2$ (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Offset voltage	TSX56xA, T = 25 °C			600	µV
		TSX56xA, -40 °C < T < 125 °C			1800	µV
		TSX56x, T = 25 °C			1	mV
		TSX56x, -40 °C < T < 125 °C			2.2	mV
$\Delta V_{io}/\Delta T$	Input offset voltage drift	-40 °C < T < 125 °C(1)		2	12	µV/°C
ΔV_{io}	Long term input offset voltage drift	T = 25 °C(2)		5		$\frac{nV}{\sqrt{month}}$
I_{io}	Input offset current (V_{out} = $V_{CC}/2$)	T = 25 °C		1	100(3)	pA
		-40 °C < T < 125 °C		1	200(3)	pA
I_{ib}	Input bias current (V_{out} = $V_{CC}/2$)	T = 25 °C		1	100(3)	pA
		-40 °C < T < 125 °C		1	200(3)	pA
CMR1	Common mode rejection ratio CMR = 20 log ($\Delta V_{ic}/\Delta V_{io}$) ($V_{ic}$ = -0.1 V to V_{CC} - 1.5 V, V_{out} = $V_{CC}/2$, R_L > 1 MΩ)	T = 25 °C	66	84		dB
		-40 °C < T < 125 °C	63			dB
CMR2	Common mode rejection ratio CMR = 20 log ($\Delta V_{ic}/\Delta V_{io}$) ($V_{ic}$ = -0.1 V to V_{CC} + 0.1 V, V_{out} = $V_{CC}/2$, R_L > 1 MΩ)	T = 25 °C	50	69		dB
		-40 °C < T < 125 °C	47			dB
A_{vd}	Large signal voltage gain (V_{out} = 0.5 V to (V_{CC} - 0.5 V), R_L > 1 MΩ)	T = 25 °C	85			dB
		-40 °C < T < 125 °C	83			dB

Table 4. Electrical characteristics at V_{CC+} = +5 V with V_{CC-} = 0 V, $V_{icm} = V_{CC}/2$, T_{amb} = 25 °C, and R_L = 10 kΩ connected to $V_{CC}/2$ (unless otherwise specified) (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{OH}	High level output voltage ($V_{OH} = V_{CC} - V_{out}$)	R_L = 10 kΩ, T = 25 °C R_L = 10 kΩ, -40 °C < T < 125 °C			70 100	mV
V_{OL}	Low level output voltage	R_L = 10 kΩ, T = 25 °C R_L = 10 kΩ, -40 °C < T < 125 °C			70 100	mV
I_{out}	I_{sink}	$V_{out} = V_{CC}$, T = 25 °C	11	14		mA
		$V_{out} = V_{CC}$, -40 °C < T < 125 °C	8			
	I_{source}	V_{out} = 0 V, T = 25 °C	9	12		mA
		V_{out} = 0 V, -40 °C < T < 125 °C	7			
I_{CC}	Supply current (per channel, $V_{out} = V_{CC}/2$, R_L > 1 MΩ)	T = 25 °C		235	350	µA
		-40 °C < T < 125 °C			400	
AC performance						
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 100 pF	700	850		kHz
F_u	Unity gain frequency	R_L = 10 kΩ, C_L = 100 pF		730		kHz
Φ_m	Phase margin	R_L = 10 kΩ, C_L = 100 pF		55		degrees
G_m	Gain margin	R_L = 10 kΩ, C_L = 100 pF		9		dB
SR	Slew rate	R_L = 10 kΩ, C_L = 100 pF, V_{out} = 0.5 V to V_{CC} - 0.5 V		1.1		V/µs
$\int e_n$	Low-frequency peak-to-peak input noise	Bandwidth: f = 0.1 to 10 Hz		15		μV_{pp}
e_n	Equivalent input noise voltage density	f = 1 kHz f = 10 kHz		55 29		$\frac{nV}{\sqrt{Hz}}$
THD+N	Total harmonic distortion + noise	Follower configuration, f_{in} = 1 kHz, R_L = 100 kΩ, $V_{icm} = (V_{CC}-1.5\ V)/2$, BW = 22 kHz, $V_{out} = 2\ V_{pp}$		0.002		%

Table 5. Electrical characteristics at V_{CC+} = +16 V with V_{CC-} = 0 V, V_{icm} = $V_{CC}/2$, T_{amb} = 25 °C, and R_L = 10 kΩ connected to $V_{CC}/2$ (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Offset voltage	TSX56xA, T = 25 °C			600	µV
		TSX56xA, -40 °C < T < 125 °C			1800	µV
		TSX56x, T = 25 °C			1	mV
		TSX56x, -40 °C < T < 125 °C			2.2	mV
$\Delta V_{io}/\Delta T$	Input offset voltage drift	-40 °C < T < 125 °C(1)		2	12	µV/°C
ΔV_{io}	Long term input offset voltage drift	T = 25 °C(2)		1.6		$\frac{\mu V}{\sqrt{month}}$
I_{io}	Input offset current (V_{out} = $V_{CC}/2$)	T = 25 °C		1	100(3)	pA
		-40 °C < T < 125 °C		1	200(3)	pA
I_{ib}	Input bias current (V_{out} = $V_{CC}/2$)	T = 25 °C		1	100(3)	pA
		-40 °C < T < 125 °C		1	200(3)	pA
CMR1	Common mode rejection ratio CMR = 20 log ($\Delta V_{ic}/\Delta V_{io}$) ($V_{ic}$ = -0.1 V to V_{CC} - 1.5 V, V_{out} = $V_{CC}/2$, R_L > 1 MΩ)	T = 25 °C	76	95		dB
		-40 °C < T < 125 °C	72			dB
CMR2	Common mode rejection ratio CMR = 20 log ($\Delta V_{ic}/\Delta V_{io}$) ($V_{ic}$ = -0.1 V to V_{CC} + 0.1 V, V_{out} = $V_{CC}/2$, R_L > 1 MΩ)	T = 25 °C	60	78		dB
		-40 °C < T < 125 °C	56			dB
SVR	Common mode rejection ratio 20 log ($\Delta V_{CC}/\Delta V_{io}$) ($V_{CC}$ = 3 V to 16 V, V_{out} = V_{icm} = $V_{CC}/2$)	T = 25 °C	76	90		dB
		-40 °C < T < 125 °C	72			dB
A_{vd}	Large signal voltage gain (V_{out} = 0.5 V to (V_{CC} - 0.5 V), R_L > 1 MΩ)	T = 25 °C	85			dB
		-40 °C < T < 125 °C	83			dB
V_{OH}	High level output voltage (V_{OH} = V_{CC} - V_{out})	R_L = 10 kΩ, T = 25 °C R_L = 10 kΩ, -40 °C < T < 125 °C			70 100	mV
V_{OL}	Low level output voltage	R_L = 10 kΩ, T = 25 °C R_L = 10 kΩ, -40 °C < T < 125 °C			70 100	mV
I_{out}	I_{sink}	V_{out} = V_{CC}, T = 25 °C	40	92		mA
		V_{out} = V_{CC}, -40 °C < T < 125 °C	35			mA
	I_{source}	V_{out} = 0 V, T = 25 °C	30	90		mA
		V_{out} = 0 V, -40 °C < T < 125 °C	25			mA
I_{CC}	Supply current (per channel, V_{out} = $V_{CC}/2$, R_L > 1 MΩ)	T = 25 °C		250	360	µA
		-40 °C < T < 125 °C			400	µA

Table 5. Electrical characteristics at V_{CC+} = +16 V with V_{CC-} = 0 V, $V_{icm} = V_{CC}/2$, T_{amb} = 25 °C, and R_L = 10 kΩ connected to $V_{CC}/2$ (unless otherwise specified) (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
AC performance						
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 100 pF	750	900		kHz
F_u	Unity gain frequency	R_L = 10 kΩ, C_L = 100 pF		750		kHz
Φ_m	Phase margin	R_L = 10 kΩ, C_L = 100 pF		55		degrees
G_m	Gain margin	R_L = 10 kΩ, C_L = 100 pF		9		dB
SR	Slew rate	R_L = 10 kΩ, C_L = 100 pF, V_{out} = 0.5 V to V_{CC} - 0.5 V		1.1		V/µs
$\int e_n$	Low-frequency peak-to-peak input noise	Bandwidth: f = 0.1 to 10 Hz		15		μV_{pp}
e_n	Equivalent input noise voltage density	f = 1 kHz f = 10 kHz		48 27		$\frac{nV}{\sqrt{Hz}}$
THD+N	Total harmonic distortion + noise	Follower configuration, f_{in} = 1 kHz, R_L = 100 kΩ, $V_{icm} = (V_{CC} - 1.5\ V)/2$, BW = 22 kHz, V_{out} = 5 V_{pp}		0.0005		%

1. See *Section 4.3: Input offset voltage drift over temperature on page 14*.
2. Typical value is based on the Vio drift observed after 1000 h at 125 °C extrapolated to 25 °C using the Arrhenius law and assuming an activation energy of 0.7 eV. The operational amplifier is aged in follower mode configuration.
3. Guaranteed by design.

Figure 2. Supply current vs. supply voltage at $V_{icm} = V_{CC}/2$

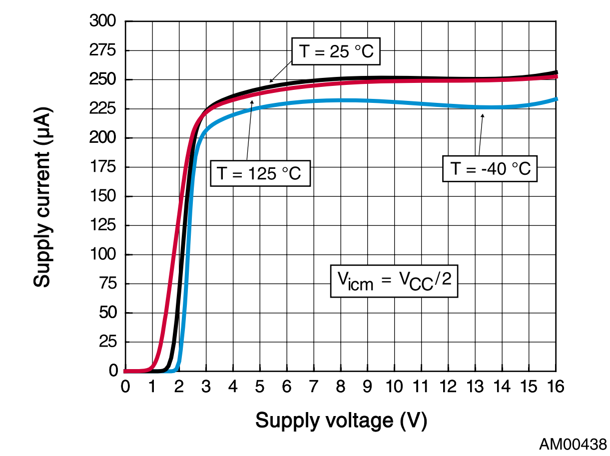


Figure 3. Input offset voltage distribution at V_{CC} = 16 V and V_{icm} = 8 V

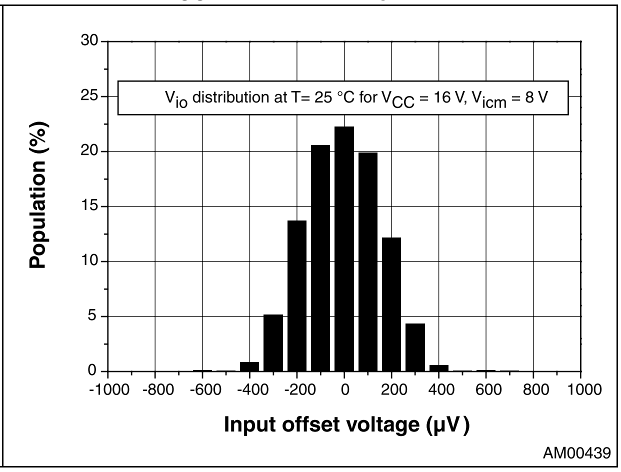


Figure 4. Input offset voltage temperature coefficient distribution at V_{CC} = 16 V and V_{icm} = 8 V

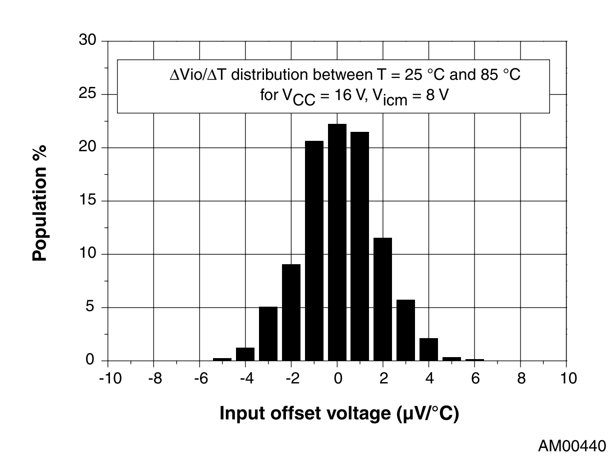


Figure 5. Input offset voltage vs. input common mode voltage at V_{CC} = 12 V

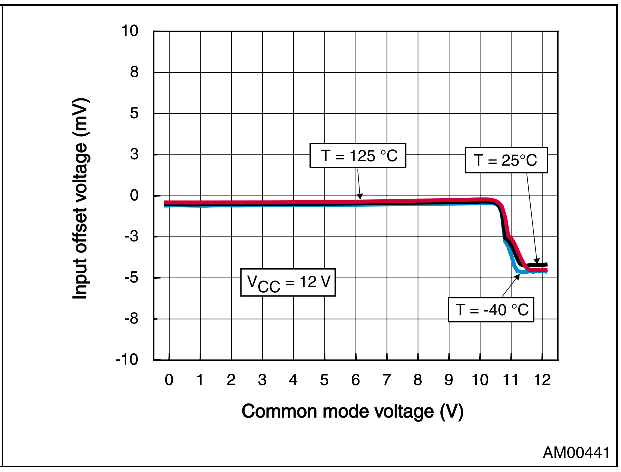


Figure 6. Input offset voltage vs. temperature at V_{CC} = 16 V

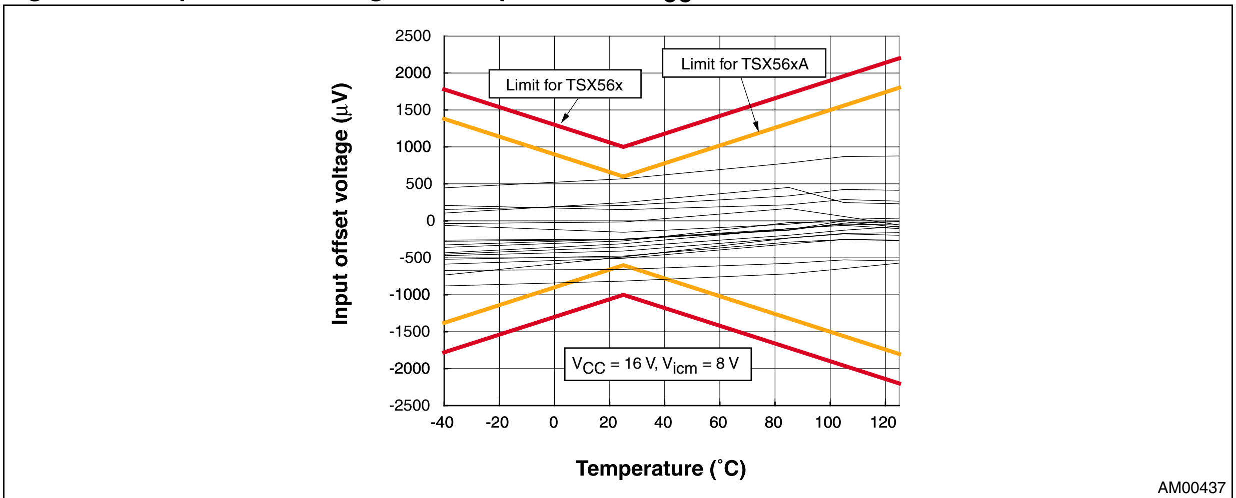


Figure 7. Output current vs. output voltage at V_{CC} = 3.3 V

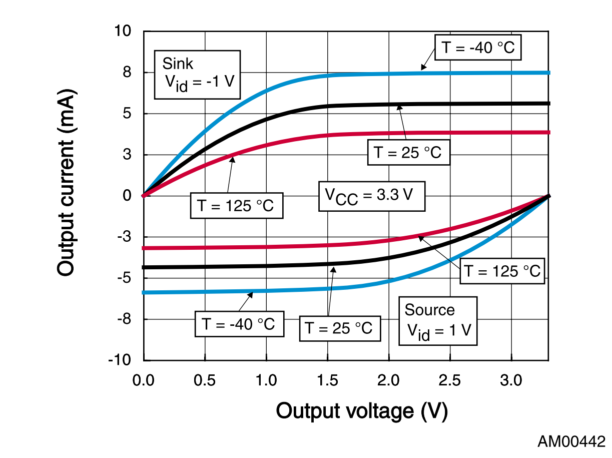


Figure 8. Output current vs. output voltage at V_{CC} = 5 V

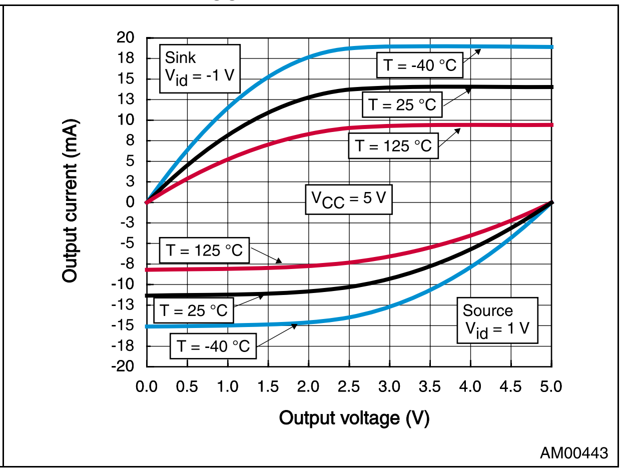


Figure 9. Output current vs. output voltage at V_{CC} = 16 V

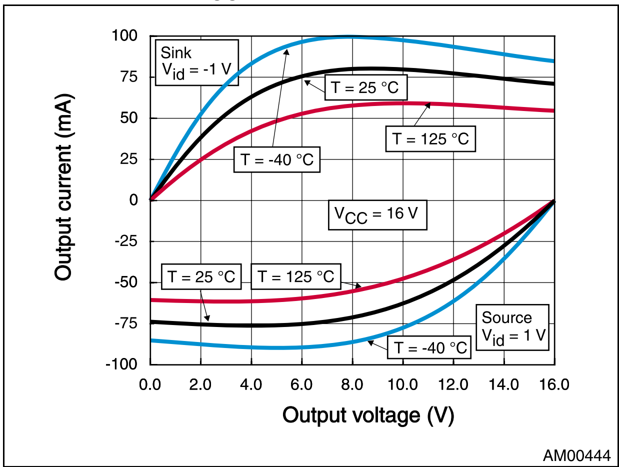


Figure 10. Bode diagram at V_{CC} = 3.3 V

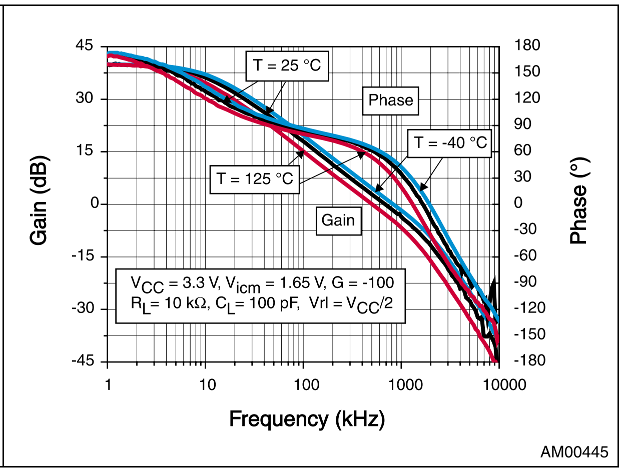


Figure 11. Bode diagram at V_{CC} = 5 V

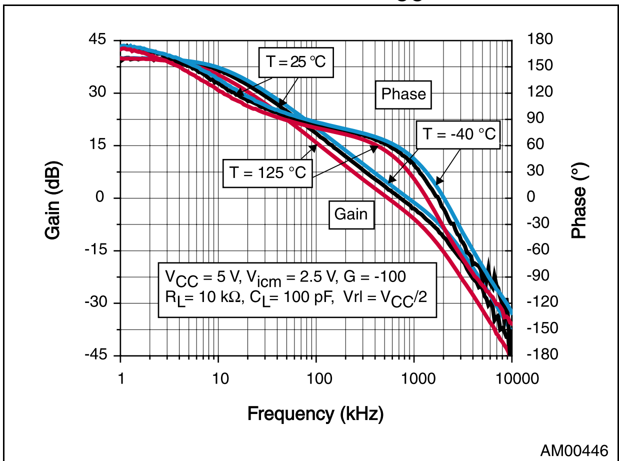


Figure 12. Bode diagram at V_{CC} = 16 V

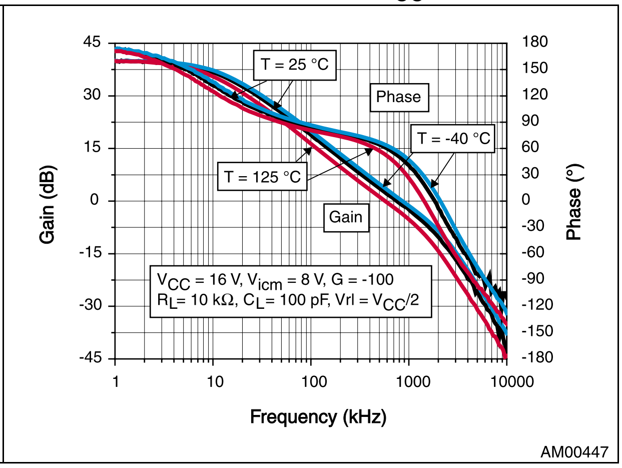


Figure 13. Phase margin vs. capacitive load at V_{CC} = 12 V

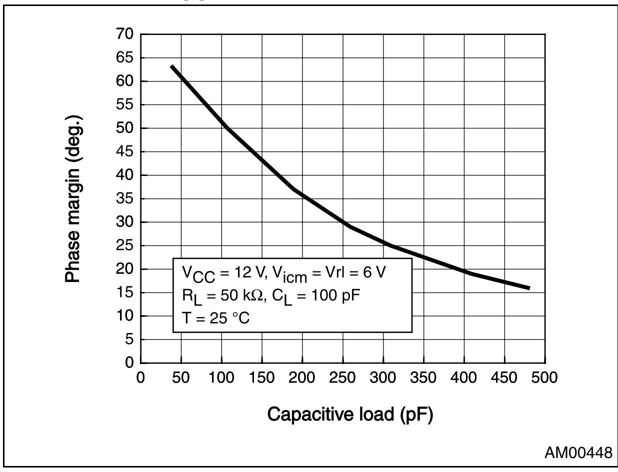


Figure 14. GBP vs. input common mode voltage at V_{CC} = 12 V

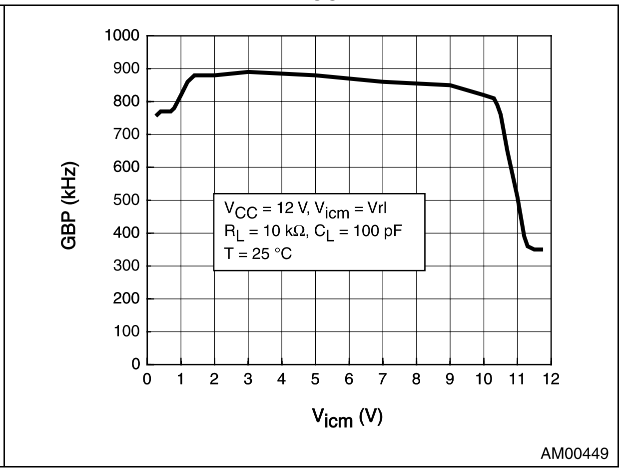


Figure 15. A_{vd} vs. input common mode voltage at V_{CC} = 12 V

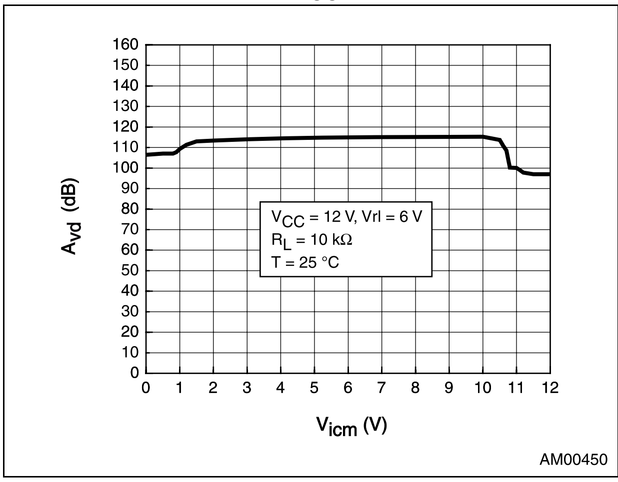


Figure 16. Slew rate vs. supply voltage

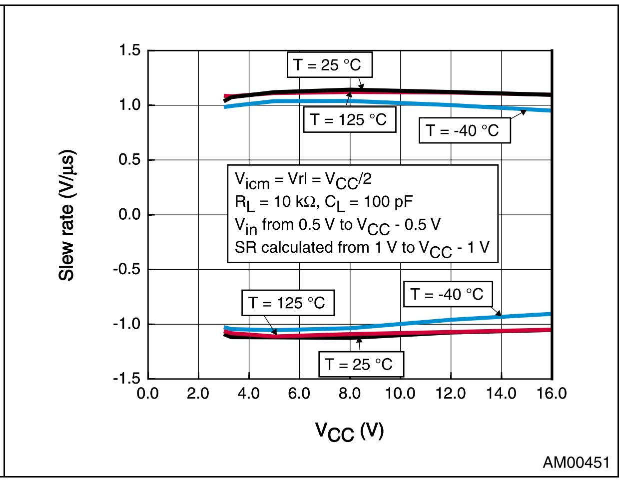


Figure 17. Noise vs. frequency at V_{CC} = 3.3 V

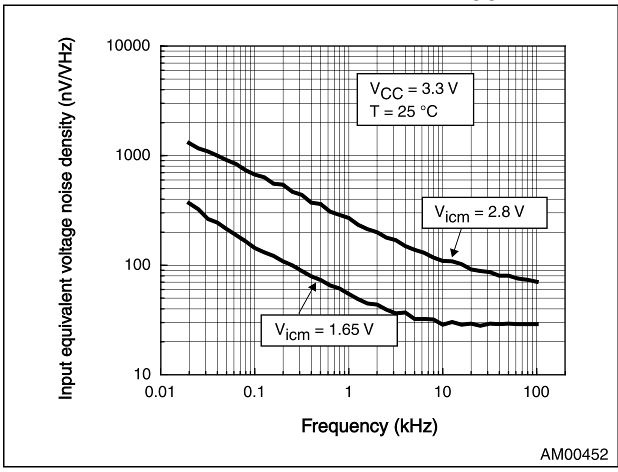


Figure 18. Noise vs. frequency at V_{CC} = 5 V

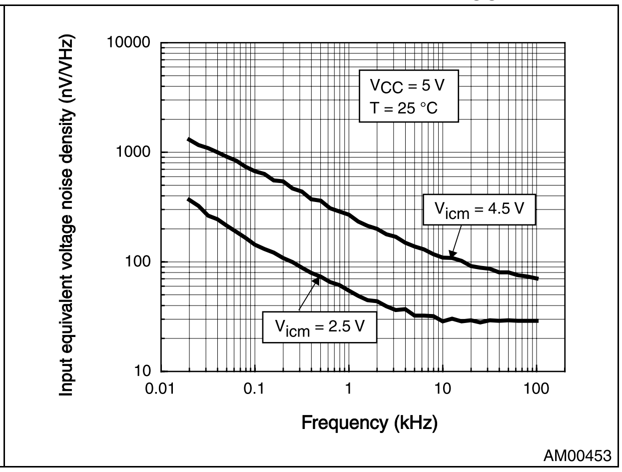


Figure 19. Noise vs. frequency at V_{CC} = 16 V

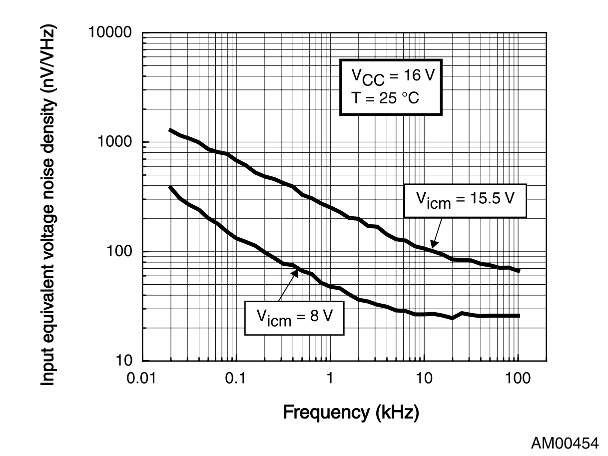


Figure 20. Distortion + noise vs. output voltage amplitude

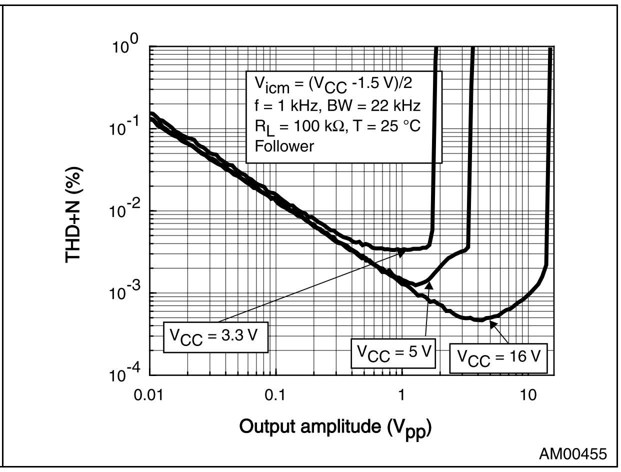


Figure 21. Distortion + noise vs. amplitude at $V_{icm} = V_{CC}/2$ and V_{CC} = 12 V

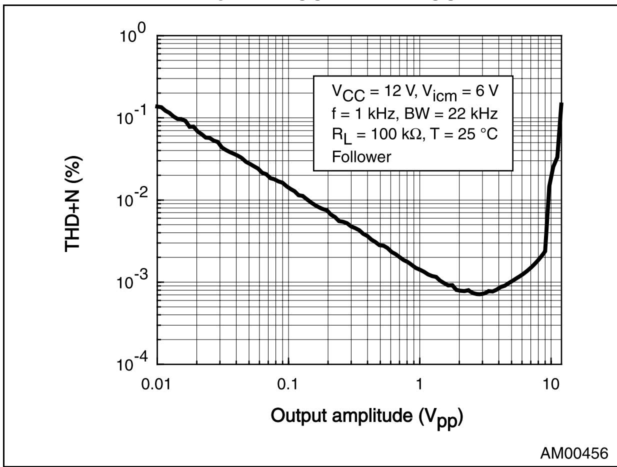
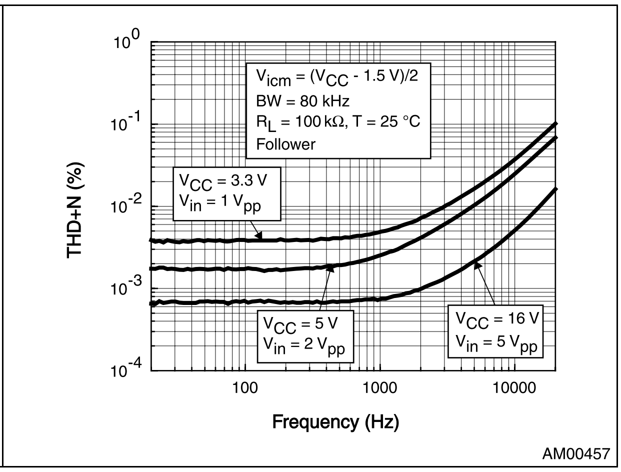


Figure 22. Distortion + noise vs. frequency



4 Application information

4.1 Operating voltages

The amplifiers of the TSX56x series can operate from 3 to 16 V. Their parameters are fully specified at 3.3, 5 and 16 V power supplies. However, the parameters are very stable in the full V_{CC} range. Additionally, the main specifications are guaranteed in extended temperature ranges from -40 to +125 ° C.

4.2 Rail-to-rail input

The TSX56x devices are built with two complementary PMOS and NMOS input differential pairs. The devices have a rail-to-rail input, and the input common mode range is extended from V_{CC-} - 0.1 V to V_{CC+} + 0.1 V. However, the performance of these devices is clearly optimized for the PMOS differential pairs (which means from V_{CC-} - 0.1 V to V_{CC+} - 1.5 V).

Beyond V_{CC+} - 1.5 V, the operational amplifiers are still functional but with degraded performance, as can be observed in the electrical characteristics section of this datasheet (mainly V_{io}, and GBP). These performances are suitable for a number of applications needing to be rail-to-rail.

The devices are designed to prevent phase reversal.

4.3 Input offset voltage drift over temperature

The maximum input voltage drift over the temperature variation is defined as the offset variation related to the offset value measured at 25 °C. The operational amplifier is one of the main circuits of the signal conditioning chain, and the amplifier input offset is a major contributor to the chain accuracy. The signal chain accuracy at 25 °C can be compensated during production at application level. The maximum input voltage drift over temperature enables the system designer to anticipate the effects of temperature variations.

The maximum input voltage drift over temperature is computed in *Equation 1*:

Equation 1

$$\frac{\Delta V_{io}}{\Delta T} = \max\left|\frac{V_{io}(T) - V_{io}(25°C)}{T - 25°C}\right|$$

with T = -40 °C and 125 °C.

The datasheet maximum value is guaranteed by measurement on a representative sample size ensuring a Cpk greater than 2.

4.4 Long term input offset voltage drift

In a product reliability evaluation, two types of stress acceleration are usable:

- Voltage acceleration, by changing the applied voltage
- Temperature acceleration, by changing the die temperature (below the maximum junction temperature allowed by the technology) with the ambient temperature.

The voltage acceleration has been defined based on the JEDEC results, and is defined by:

Equation 2

$$A_{FV} = e^{\beta \cdot (V_S - V_U)}$$

where:

A_{FV} is the voltage acceleration factor

β is the voltage acceleration constant in 1/V, constant technology parameter

V_S is the stress voltage used for the accelerated test

V_U is the use voltage for the application

The temperature acceleration is driven by the Arrhenius model, and is defined by:

Equation 3

$$A_{FT} = e^{\frac{E_a}{k} \cdot \left(\frac{1}{T_U} - \frac{1}{T_S}\right)}$$

where:

A_{FT} is the temperature acceleration factor

E_a is the activation energy of the technology based on failure rate

k is the Boltzmann's constant

T_U is the temperature of the die when V_U is used

T_S is the temperature of the die under temperature stress

The final acceleration factor, A_F is the multiplication of these two acceleration factors, which is:

Equation 4

$$A_F = A_{FT} \times A_{FV}$$

Based on this A_F calculated following the defined usage temperature and usage voltage of the product, the 1000 h duration of the stress corresponds to a number of equivalent months of usage.

Equation 5

$$\text{Months} = A_F \times 1000\ \text{h} \times 12\ \text{months} / (24\ \text{h} \times 365.25\ \text{days})$$

For the operational amplifier, a follower stress condition is used for the reliability evaluation, with V_{CC} defined in function of the maximum operating voltage and the absolute maximum rating (as recommended by the JEDEC standards).

The V_{io} drift, in µV, of the product after 1000 h duration of stress is tracked with parameters at different measurement conditions, as for example:

Equation 6

$$V_{CC} = \text{max. } V_{op} \text{ with } V_{icm} = V_{CC}/2.$$

Finally, knowing the calculated number of months and with the measured drift value of the V_{io} (corresponding to the electrical characteristics of the respective table) after 1000 h duration of stress, the ratio of the V_{io} drift over the square of months, ΔV_{io} in µV/√month, is defined as the long term drift parameter, the parameter estimating the reliability performance of the product.

Equation 7

$$\Delta V_{io} = V_{io} \text{ drift} / \sqrt{(\text{Months})}$$

4.5 PCB layouts

For correct operation, it is advised to add 10 nF decoupling capacitors as close as possible to the power supply pins.

4.6 Macromodel

Accurate macromodels of the TSX56x are available on STMicroelectronics™ website at www.st.com. This model is a trade-off between accuracy and complexity (that is, time simulation) of the TSX56x operational amplifiers. It emulates the nominal performance of a typical device within the specified operating conditions mentioned in the datasheet. It also helps to validate a design approach and to select the right operational amplifier, *but it does not replace onboard measurements*.

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

Figure 23. SOT23 - 5-lead small outline transistor package outline

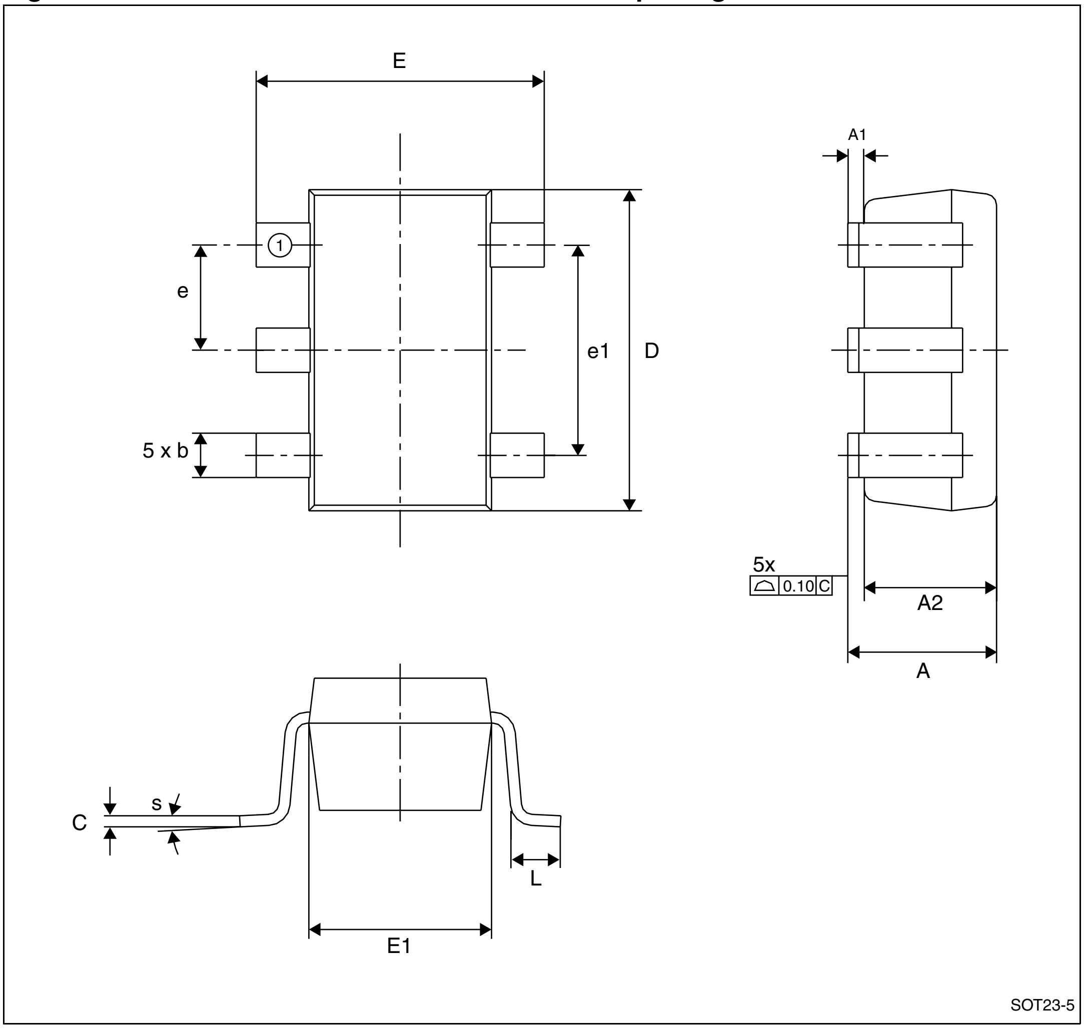
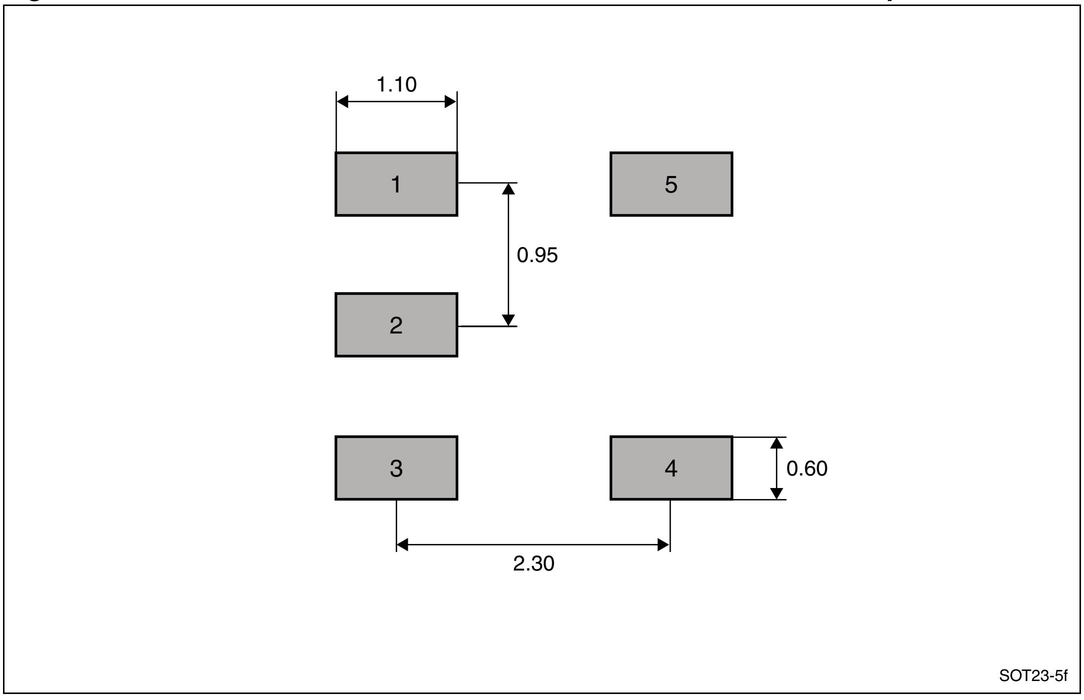


Table 6. SOT23 - 5-lead small outline transistor package mechanical data

Symbol	Dimensions					
	Millimeters			Inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			1.45			0.057
A1		0.00	0.15		0.000	0.006
A2	1.15	0.90	1.30	0.045	0.035	0.051
b		0.30	0.50		0.012	0.020
c		0.08	0.22		0.003	0.009
D	2.90			0.114		
E	2.80			0.110		
E1	1.60			0.063		
e	0.95			0.037		
e1	1.90			0.075		
L	0.45	0.30	0.60	0.018	0.012	0.024
θ	4	0	8	4	0	8
N	5			5		

Figure 24. SOT23 - 5-lead small outline transistor recommended footprint



6 Ordering information

Table 7. Order codes

Order code	Temperature range	Channel number	Package	Packing	Marking
TSX561ILT	-40 to 125 °C	1	SOT23-5	Tape and reel	K23
TSX561IYLT	-40 to 125 °C Automotive grade(1)	1	SOT23-5	Tape and reel	K116
TSX561AILT	-40 to 125 °C	1	SOT23-5	Tape and reel	K117
TSX561AIYLT	-40 to 125 °C Automotive grade(1)	1	SOT23-5	Tape and reel	K118

1. Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 and Q 002 or equivalent are ongoing.

7 Revision history

Table 8. Document revision history

Date	Revision	Changes
06-Jun-2012	1	Initial release.