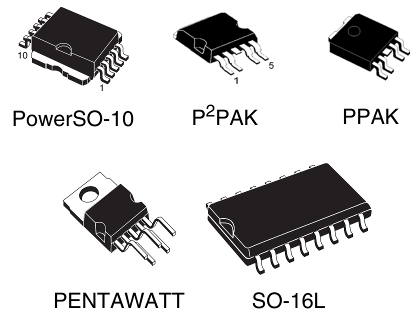
VN820-E

High-side driver

Features

Type	$R_{DS(on)}$	I_{OUT}	V_{CC}
VN820-E VN820SP-E VN820B5-E VN820SO-E VN820PT-E	40 mΩ	9 A	36 V

- CMOS compatible input
- On-state open load detection
- Off-state open load detection
- Shorted load protection
- Under-voltage and over-voltage shutdown
- Protection against loss of ground
- Very low standby current
- Reverse battery protection (see *Application schematic*)



Description

The VN820-E is a monolithic device designed in STMicroelectronic's VIPower M0-3 technology. The VN820-E is intended for driving any type of load with one side connected to ground. The active V_{CC} pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table).

Active current limitation combined with thermal shutdown and automatic restart protects the device against over-load. The device detects the open load condition in both the on and off-state. In the off-state the device detects if the output is shorted to V_{CC}. The device automatically turns off in the case where the ground pin becomes disconnected.

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
PENTAWATT	VN820-E	-
PowerSO-10	VN820SP-E	VN820SP13TR-E
P^2PAK	VN820B5-E	VN820B513TR-E
PPAK	VN820PT-E	VN820PT13TR-E
SO-16L	VN820SO-E	VN820SO13TR-E

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1 Block diagram and pin description

Figure 1. Block diagram

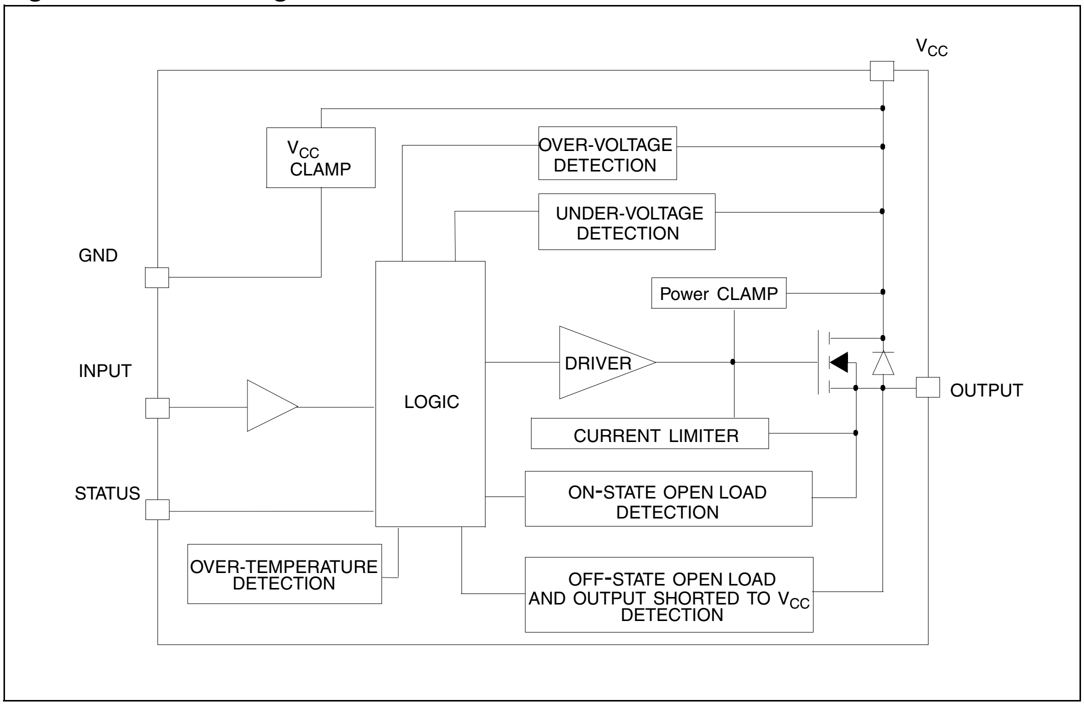


Figure 2. Configuration diagram (top view)

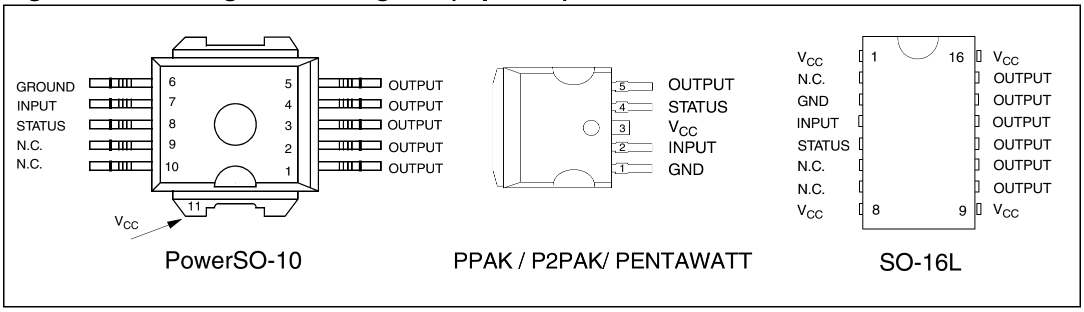
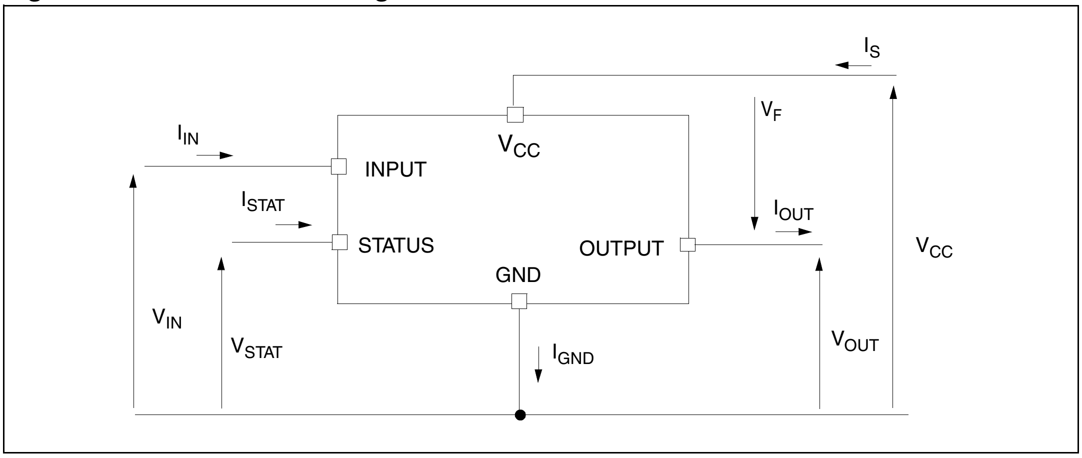


Table 2. Suggested connections for unused and not connected pins

Connection / pin	Status	N.C.	Output	Input
Floating	X	X	X	X
To ground		X		Through 10KΩ resistor

2 Electrical specifications

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to Absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics sure program and other relevant quality document.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value					Unit
		SO-16L	PowerSO-10	PENTAWATT	P^2PAK	PPAK	
V_{CC}	DC supply voltage	41					V
$- V_{CC}$	Reverse DC supply voltage	- 0.3					V
$- I_{gnd}$	DC reverse ground pin current	- 200					mA
I_{OUT}	DC output current	Internally limited					A
$- I_{OUT}$	Reverse DC output current	- 9					A
I_{IN}	DC input current	+/- 10					mA
I_{STAT}	DC Status current	+/- 10					mA
V_{ESD}	Electrostatic discharge (human body model: R = 1.5KΩ; C = 100pF) - INPUT - STATUS - OUTPUT - V_{CC}	 4000 4000 5000 5000					 V V V V

Table 3. Absolute maximum ratings (continued)

Symbol	Parameter	Value					Unit
		SO-16L	PowerSO-10	PENTAWATT	P^2PAK	PPAK	
E_{MAX}	Maximum switching energy ($L = 4mH$; $R_L = 0\Omega$; $V_{bat} = 13.5V$; $T_{jstart} = 150ºC$; $I_L = 13A$)	-	481	-	481	-	mJ
E_{MAX}	Maximum switching energy ($L = 3.7mH$; $R_L = 0\Omega$; $V_{bat} = 13.5V$; $T_{jstart} = 150ºC$; $I_L = 13A$)	438	-	-	-	-	mJ
E_{MAX}	Maximum switching energy ($L = 4.48mH$; $R_L = 0\Omega$; $V_{bat} = 13.5V$; $T_{jstart} = 150ºC$; $I_L = 13A$)	-	-	-	-	526	mJ
P_{tot}	Power dissipation $T_C = 25°C$	8.3	65.8	65.8	65.8	65.8	W
T_j	Junction operating temperature	Internally limited					°C
T_c	Case operating temperature	- 40 to 150					°C
T_{stg}	Storage temperature	- 55 to 150					°C

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Max. value					Unit
		SO-16L	PowerSO-10	PENTAWATT	P^2PAK	PPAK	
$R_{thj-case}$	Thermalresistance junction-case	-	1.9	1.9	1.9	1.9	°C/W
$R_{thj-lead}$	Thermalresistance junction-lead	15	-	-	-	-	°C/W
$R_{thj-amb}$	Thermalresistance junction-ambient	65(1)	51.9(2)	61.9(2)	51.9(2)	76.9(2)	°C/W
		48(3)	37(4)	-	37(4)	45(4)	°C/W

1. When mounted on FR4 printed circuit board with $0.5cm^2$ of Cu (at least 35µm thick) connected to all V_{CC} pins.
2. When mounted on a standard single-sided FR-4 board with $0.5cm^2$ of Cu (at least 35µm thick).
3. When mounted on FR4 printed circuit board with $6cm^2$ of Cu (at least 35µm thick) connected to all V_{CC} pins.
4. When mounted on a standard single-sided FR-4 board with $6cm^2$ of Cu (at least 35µm thick).

2.3 Electrical characteristics

Values specified in this section are for 8V < V_{CC} < 36V; -40°C < Tj < 150°C, unless otherwise stated.

Table 5. Power

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		5.5	13	36	V
V_{USD}	Under-voltage shutdown		3	4	5.5	V
$V_{USDhyst}$	Under-voltage shutdown hysteresis			0.5		V
V_{OV}	Over-voltage shutdown		36			V
R_{ON}	On-state resistance	I_{OUT} = 3A; T_j = 25°C; V_{CC} > 8V I_{OUT} = 3A; V_{CC} > 8V			40 80	mΩ mΩ
I_S	Supply current	Off-state; V_{CC} = 13V; V_{IN} = V_{OUT} = 0V Off-state; V_{CC} = 13V; V_{IN} = V_{OUT} = 0V; T_j = 25°C On-state; V_{CC} = 13V; V_{IN} = 5V; I_{OUT} = 0A		10 10 2	25 20 3.5	µA µA mA
$I_{L(off1)}$	Off-state output current	V_{IN} = V_{OUT} = 0V	0		50	µA
$I_{L(off2)}$	Off-state output current	V_{IN} = 0V; V_{OUT} = 3.5V	-75		0	µA
$I_{L(off3)}$	Off-state output current	V_{IN} = V_{OUT} = 0V; V_{CC} = 13V; T_j = 125°C			5	µA
$I_{L(off4)}$	Off-state output current	V_{IN} = V_{OUT} = 0V; V_{CC} = 13V; T_j = 25°C			3	µA

Table 6. Switching (V_{CC}=13V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	R_L = 4.3Ω from V_{IN} rising edge to V_{OUT} = 1.3V		30		µs
$t_{d(off)}$	Turn-off delay time	R_L = 4.3Ω from V_{IN} falling edge to V_{OUT} = 11.7V		30		µs
$dV_{OUT}/dt_{(on)}$	Turn-on voltage slope	R_L = 4.3Ω from V_{OUT} = 1.3V to V_{OUT}=10.4V	See *Figure 21.*			V/µs
$dV_{OUT}/dt_{(off)}$	Turn-off voltage slope	R_L = 4.3Ω from V_{OUT} = 11.7V to V_{OUT} = 1.3V	See *Figure 22.*			V/µs

Table 7. Input pin

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low-level				1.25	V
I_{IL}	Low-level input current	$V_{IN} = 1.25V$	1			µA
V_{IH}	Input high-level		3.25			V
I_{IH}	High-level input current	$V_{IN} = 3.25V$			10	µA
V_{hyst}	Input hysteresis voltage		0.5			V
V_{ICL}	Input clamp voltage	$I_{IN} = 1mA$ $I_{IN} = -1mA$	6	6.8 - 0.7	8	V V

Table 8. V_{CC} output diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_F	Forward on voltage	$- I_{OUT} = 2A$; $T_j = 150°C$			0.6	V

Table 9. Status pin

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{STAT}	Status low output voltage	$I_{STAT} = 1.6mA$			0.5	V
I_{LSTAT}	Status leakage current	Normal operation; $V_{STAT} = 5V$			10	µA
C_{STAT}	Status pin input capacitance	Normal operation; $V_{STAT} = 5V$			100	pF
V_{SCL}	Status clamp voltage	$I_{STAT} = 1mA$ $I_{STAT} = - 1mA$	6	6.8 - 0.7	8	V V

Table 10. Protections(1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature		135			°C
T_{hyst}	Thermal hysteresis		7	15		°C
t_{SDL}	Status delay in over-load condition	$T_j > T_{jsh}$			20	ms
I_{lim}	Current limitation	$9V < V_{CC} < 36V$ $5.5V < V_{CC} < 36V$	9	13	20 20	A A
V_{demag}	Turn-off output clamp voltage	$I_{OUT} = 3$ A; $V_{IN} = 0V$; L = 6mH	V_{CC} - 41	V_{CC} - 48	V_{CC} - 55	V

1. To ensure long term reliability under heavy over-load or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device operates under abnormal conditions this software must limit the duration and number of activation cycles.

Table 11. Open load detection

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{OL}	Open load on-state detection threshold	V_{IN} = 5V	70	150	300	mA
$t_{DOL(on)}$	Open load on-state detection delay	I_{OUT} = 0A			200	µs
V_{OL}	Open load off-state voltage detection threshold	V_{IN} = 0V	1.5	2.5	3.5	V
$t_{DOL(off)}$	Open load detection delay at turn-off				1000	µs

Figure 4. Status timings

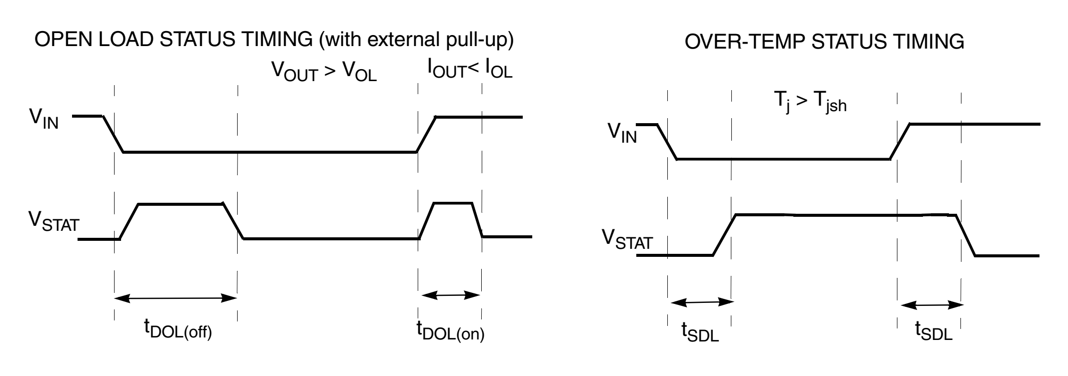


Figure 5. Switching time waveforms

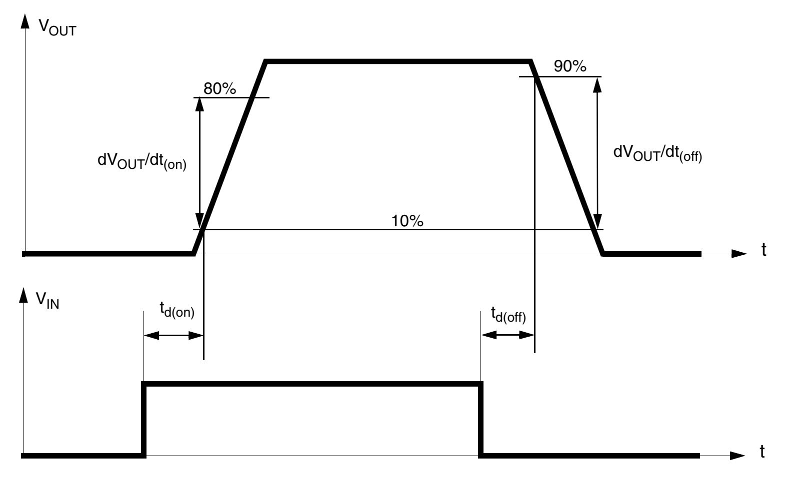


Table 12. Truth table

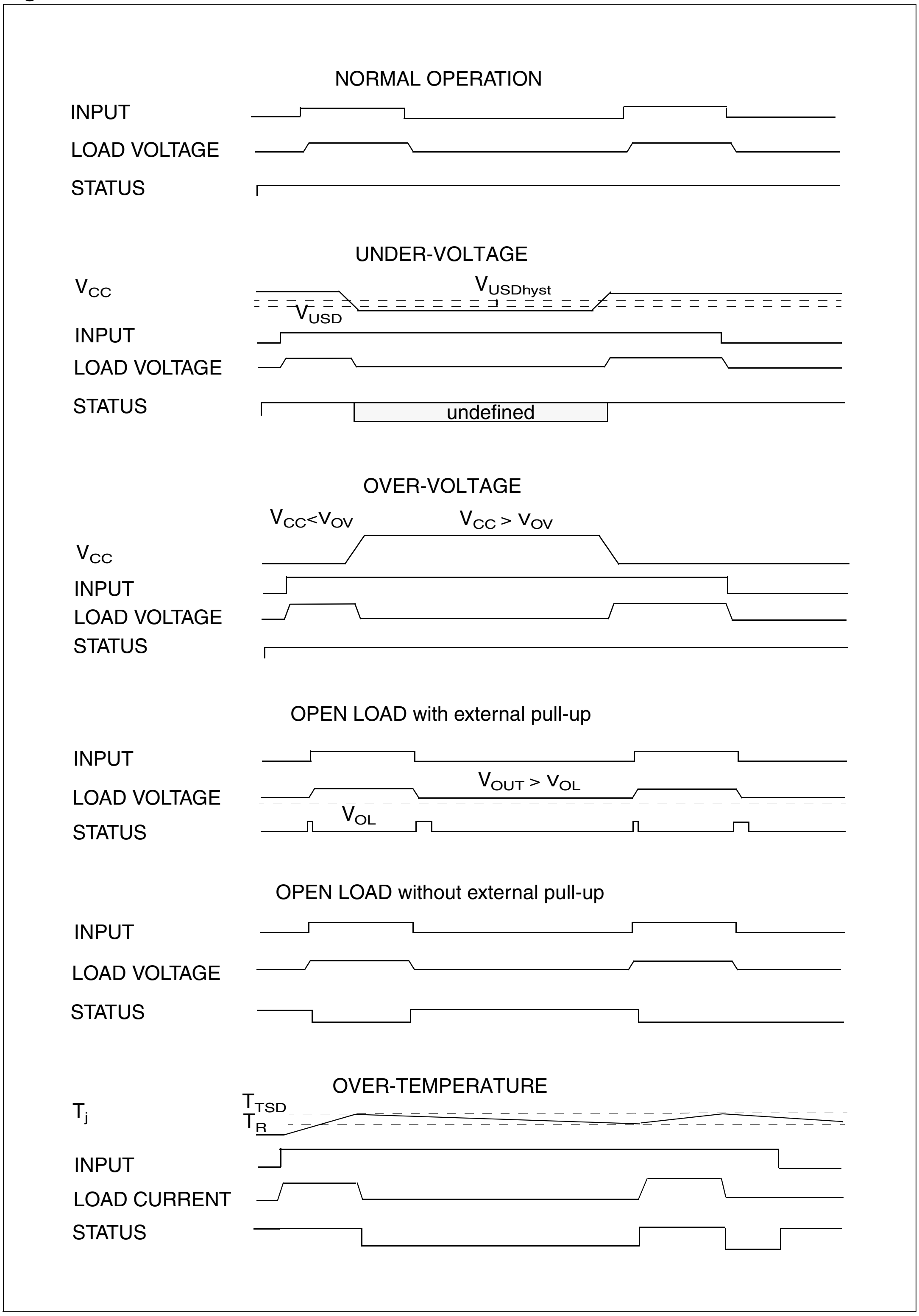
Conditions	Input	Output	Status
Normal operation	L H	L H	H H
Current limitation	L H H	L X X	H $(T_j < T_{TSD})$ H $(T_j > T_{TSD})$ L
Over-temperature	L H	L L	H L
Under-voltage	L H	L L	X X
Over-voltage	L H	L L	H H
Output voltage > V_{OL}	L H	H H	L H
Output current < I_{OL}	L H	L H	H L

Table 13. Electrical transient requirements

ISO T/R 7637/1 Test pulse	Test level				
	I	II	III	IV	Delays and impedance
1	- 25V(1)	- 50V(1)	- 75V(1)	- 100V(1)	2ms, 10Ω
2	+ 25V(1)	+ 50V(1)	+ 75V(1)	+ 100V(1)	0.2ms, 10Ω
3a	- 25V(1)	- 50V(1)	- 100V(1)	- 150V(1)	0.1µs, 50Ω
3b	+ 25V(1)	+ 50V(1)	+ 75V(1)	+ 100V(1)	0.1µs, 50Ω
4	- 4V(1)	- 5V(1)	- 6V(1)	- 7V(1)	100ms, 0.01Ω
5	+ 26.5V(1)	+ 46.5V(2)	+ 66.5V(2)	+ 86.5V(2)	400ms, 2Ω

1. All functions of the device are performed as designed after exposure to disturbance.
2. One or more functions of the device is not performed as designed after exposure and cannot be returned to proper operation without replacing the device.

Figure 6. Waveforms



2.4 Electrical characteristics curves

Figure 7. Off-state output current

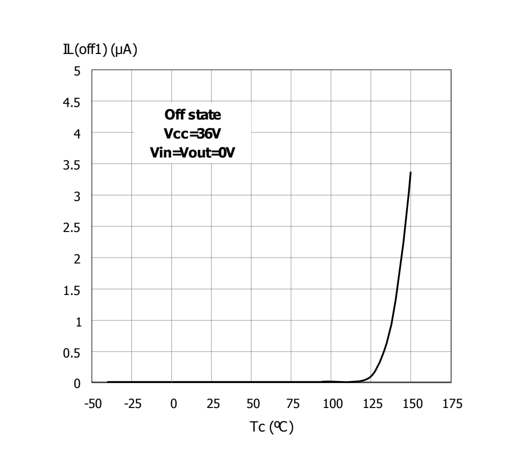


Figure 8. High-level input current

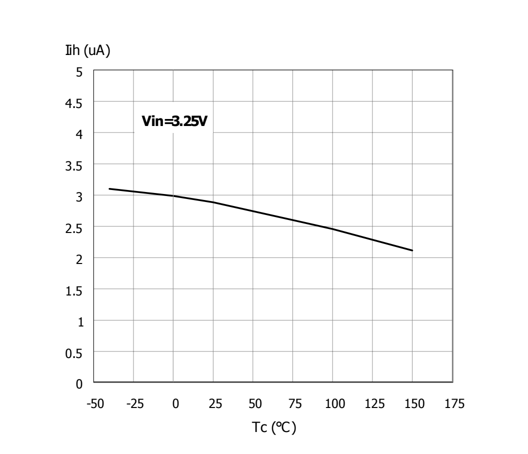


Figure 9. Input clamp voltage

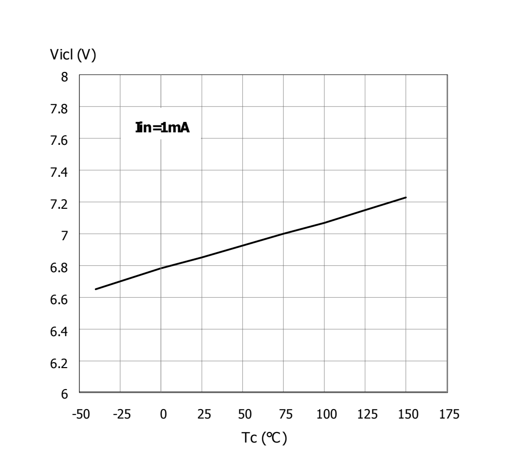


Figure 10. Status leakage current

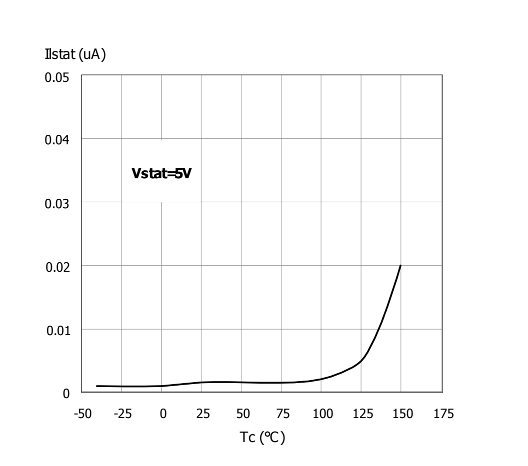


Figure 11. Status low output voltage

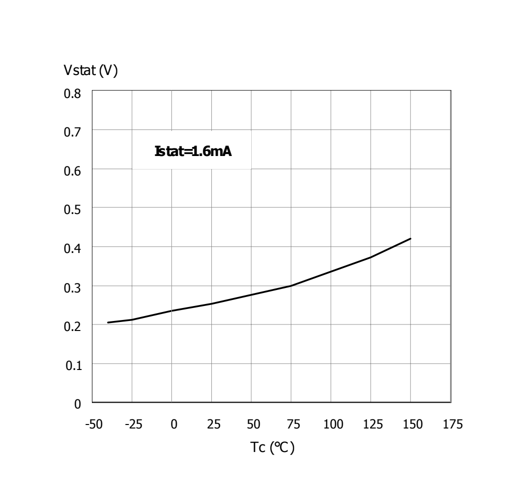


Figure 12. Status clamp voltage

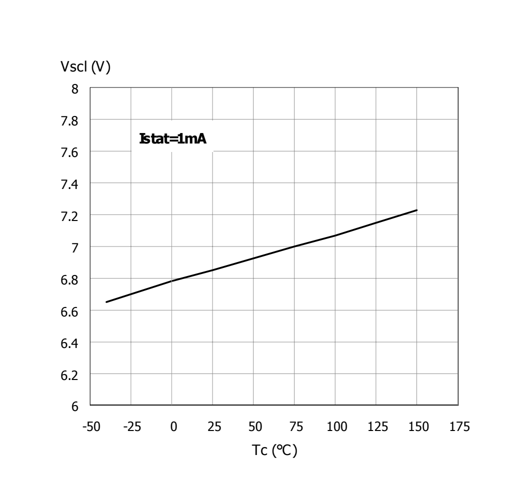


Figure 13. On-state resistance Vs T_{case}

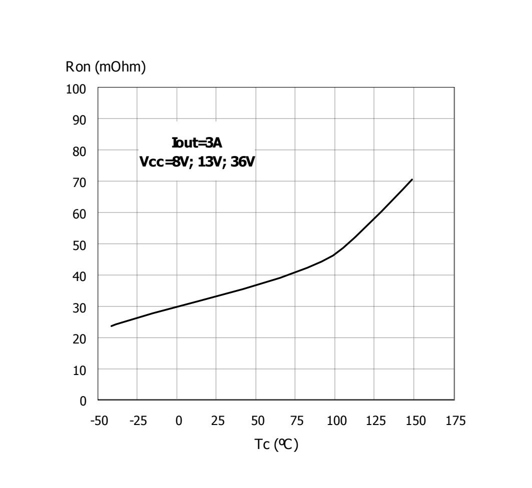


Figure 14. On-state resistance Vs V_{CC}

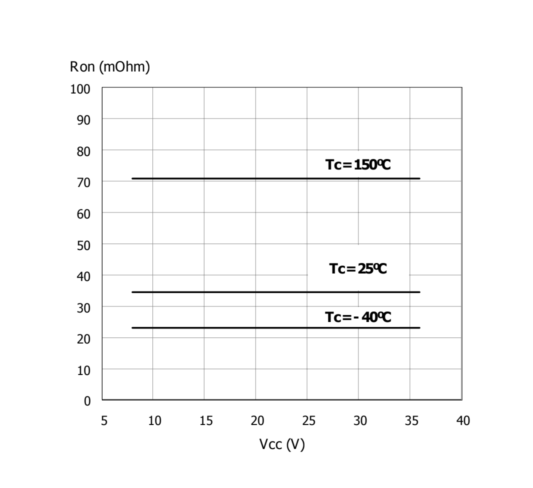


Figure 15. Open load on-state detection threshold

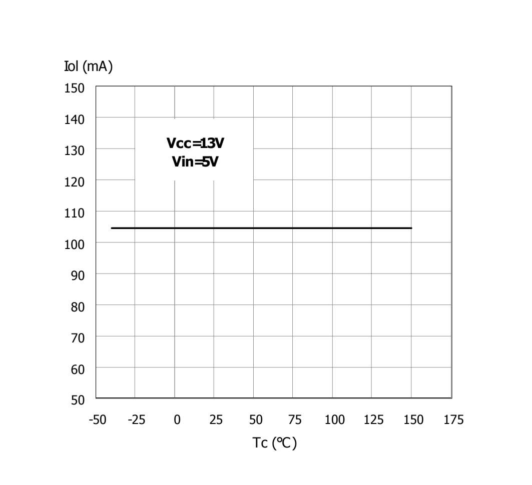


Figure 16. Input high-level

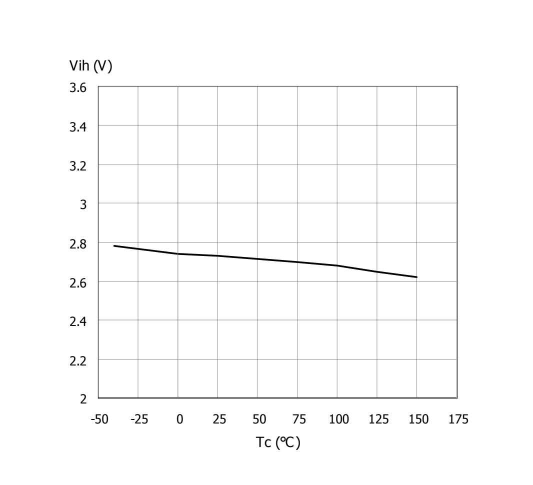


Figure 17. Input low-level

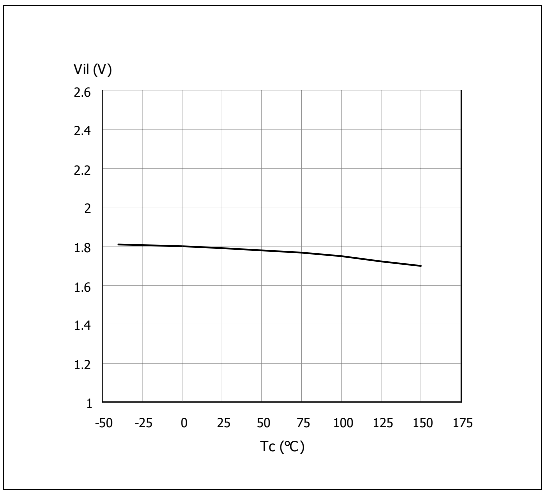


Figure 18. Input hysteresis voltage

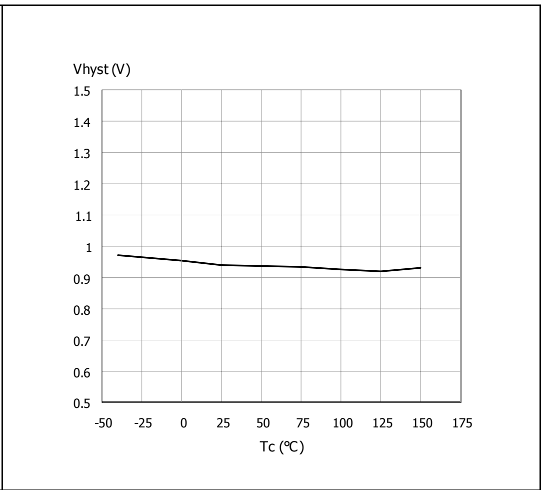


Figure 19. Over-voltage shutdown

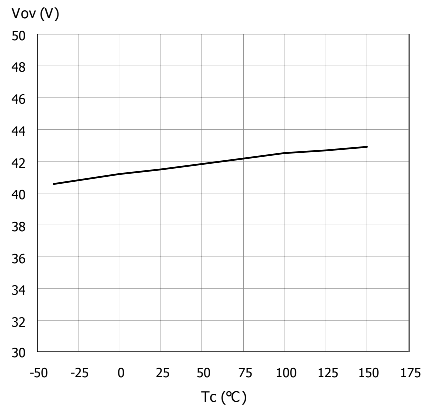


Figure 20. Open load off-state voltage detection threshold

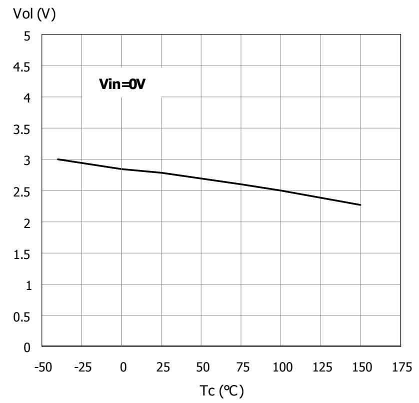


Figure 21. Turn-on voltage slope

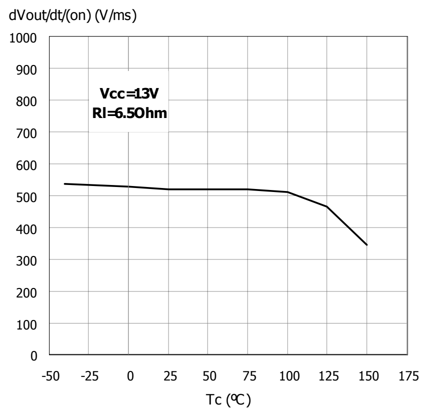


Figure 22. Turn-off voltage slope

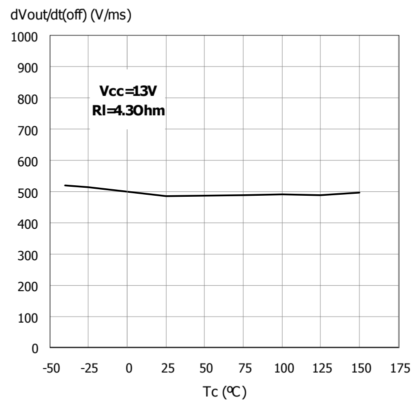
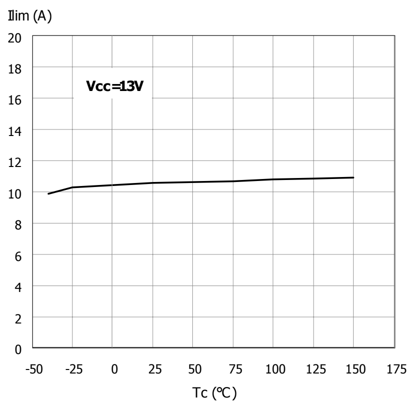
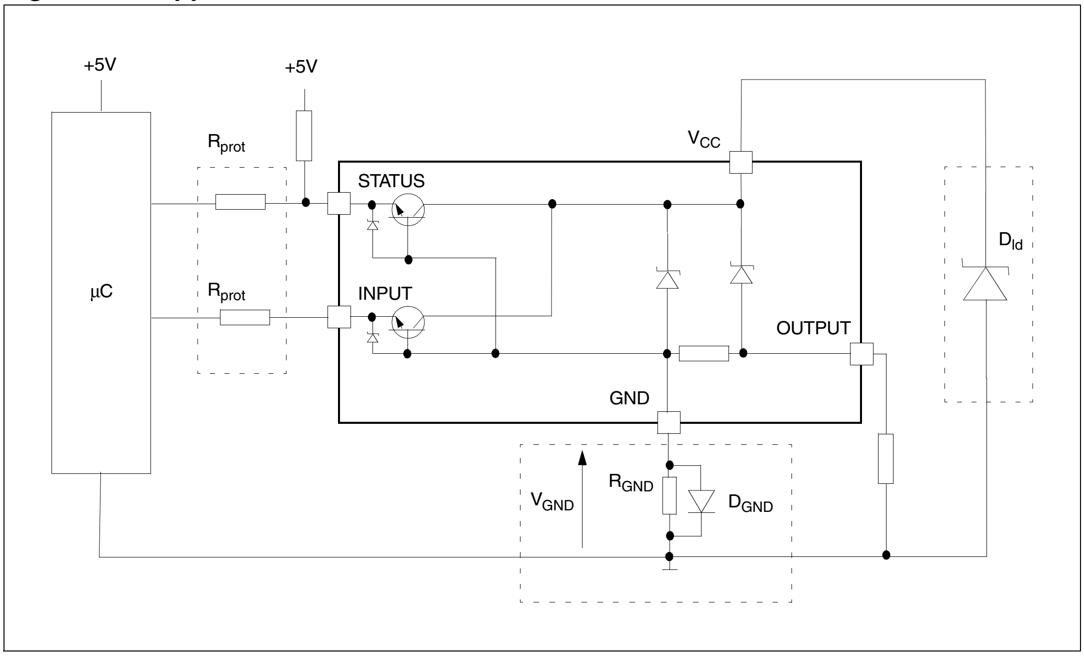


Figure 23. I_{lim} Vs T_{case}



3 Application information

Figure 24. Application schematic



3.1 GND protection network against reverse battery

3.1.1 Solution 1: resistor in the ground line (R_{GND} only)

This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

1. $R_{GND} \leq 600mV / (I_{S(on)max})$.
2. $R_{GND} \geq (- V_{CC}) / (- I_{GND})$

where - I_{GND} is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power Dissipation in R_{GND} (when $V_{CC} < 0$: during reverse battery situations) is:

$P_D = (- V_{CC})^2 / R_{GND}$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not shared by the device ground then the R_{GND} will produce a shift ($I_{S(on)max}$ * R_{GND}) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high-side drivers sharing the same R_{GND}.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then ST suggests to utilize Solution 2 (see below).

3.1.2 Solution 2: diode (D_{GND}) in the ground line

A resistor ($R_{GND} = 1k\Omega$) should be inserted in parallel to D_{GND} if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network will produce a shift ($\approx$ 600mV) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

Series resistor in INPUT and STATUS lines are also required to prevent that, during battery voltage transient, the current exceeds the absolute maximum rating.

Safest configuration for unused INPUT and STATUS pin is to leave them unconnected.

3.2 Load dump protection

D_{ld} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds the V_{CC} max DC rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in the ISO 7637-2: 2004(E) table.

3.3 MCU I/Os protection

If a ground protection network is used and negative transient are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the µC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of µC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of µC I/Os.

$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C}-V_{IH}-V_{GND}) / I_{IHmax}$

Calculation example:

For V_{CCpeak}= - 100V and $I_{latchup} \geq 20mA$; $V_{OH\mu C} \geq 4.5V$

$5k\Omega \leq R_{prot} \leq 65k\Omega$

Recommended values: $R_{prot} = 10k\Omega$.

3.4 Open load detection in off-state

Off-state open load detection requires an external pull-up resistor (R_{PU}) connected between OUTPUT pin and a positive supply voltage (V_{PU}) like the +5V line used to supply the microprocessor.

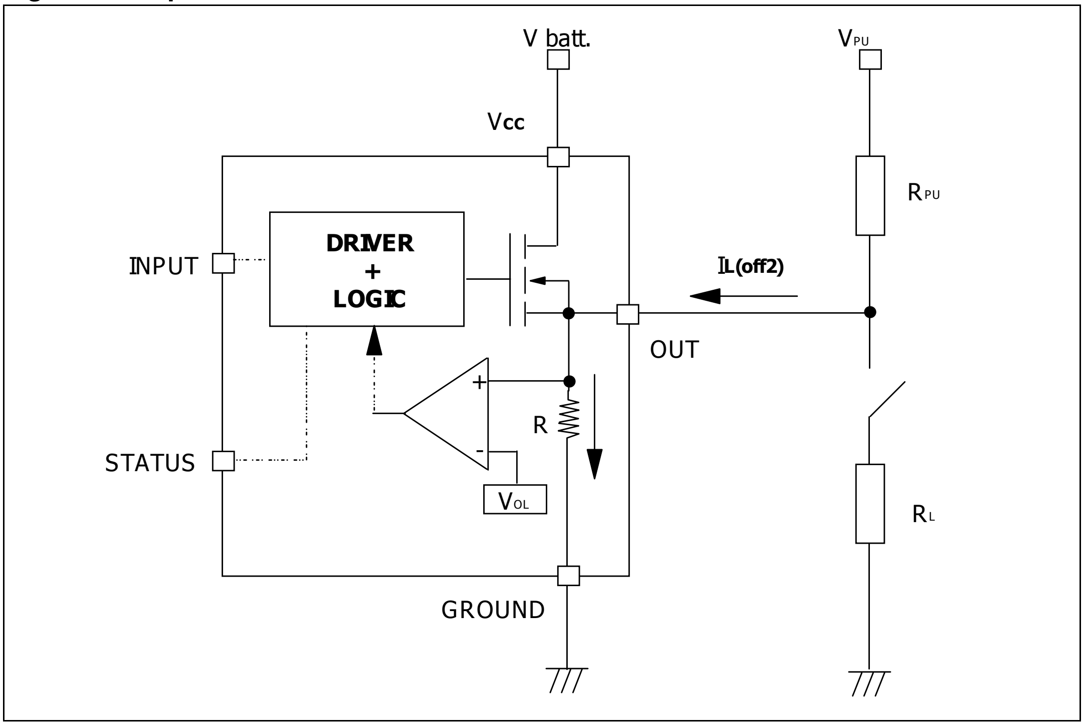
The external resistor has to be selected according to the following requirements:

1. no false open load indication when load is connected: in this case we have to avoid V_{OUT} to be higher than V_{Olmin}; this results in the following condition $V_{OUT} = (V_{PU} / (R_L + R_{PU})) R_L < V_{Olmin}$.
2. no misdetection when load is disconnected: in this case the V_{OUT} has to be higher than V_{OLmax}; this results in the following condition $R_{PU} < (V_{PU} - V_{OLmax}) / I_{L(off2)}$.

Because $I_{s(OFF)}$ may significantly increase if V_{out} is pulled high (up to several mA), the pull-up resistor R_{PU} should be connected to a supply that is switched off when the module is in standby.

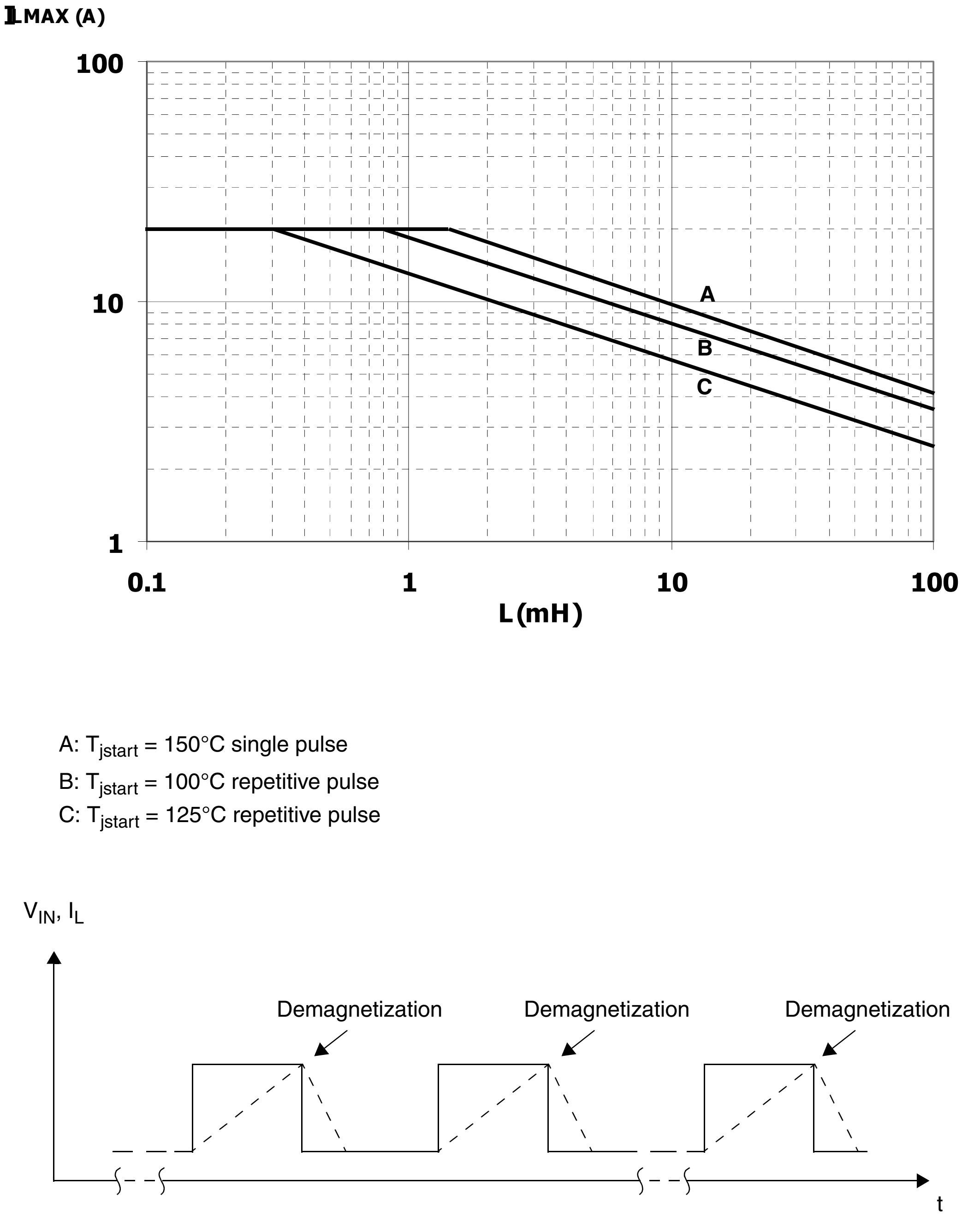
The values of V_{OLmin}, V_{OLmax} and $I_{L(off2)}$ are available in the electrical characteristics section.

Figure 25. Open load detection in off-state



3.5 PowerSO-10, P²PAK, PENTAWATT maximum demagnetization energy (V_{CC} = 13.5V)

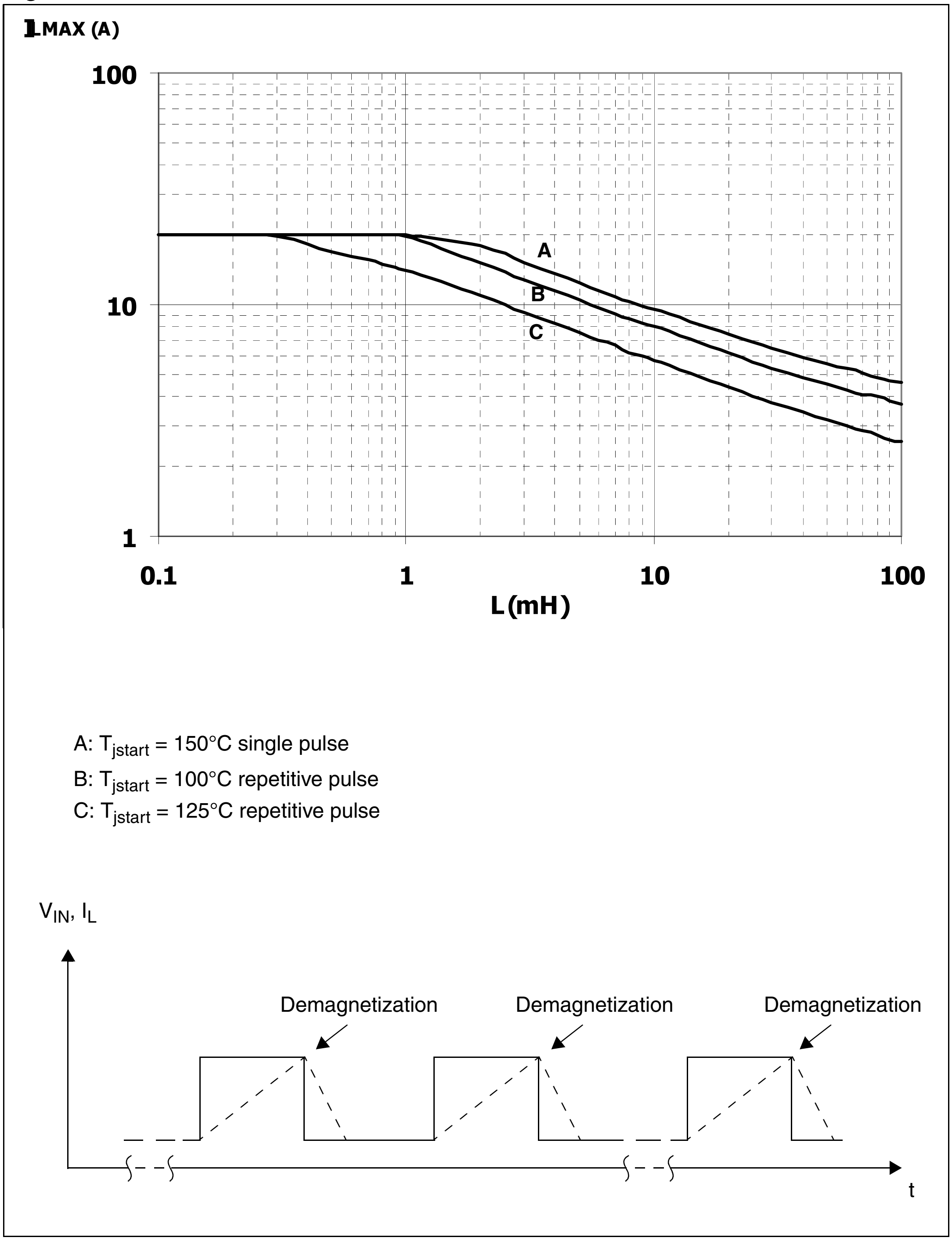
Figure 26. PowerSO-10, P²PAK, PENTAWATT maximum turn-off current versus inductance



Note: Values are generated with R_L =0 Ω. In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

3.6 PPAK maximum demagnetization energy (V_{CC} = 13.5V)

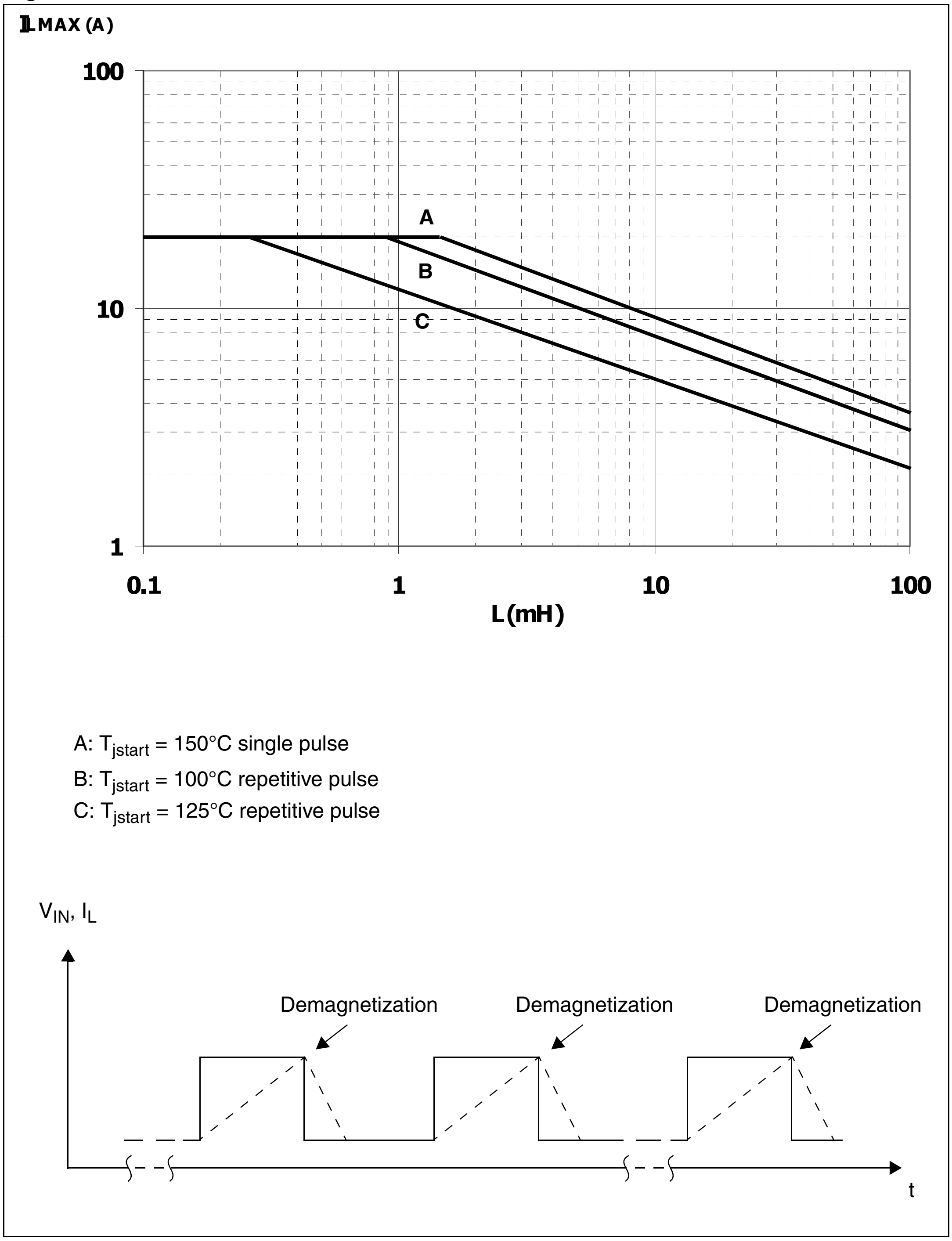
Figure 27. PPAK maximum turn-off current versus inductance



Note: *Values are generated with R_L =0 Ω. In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.*

3.7 SO-16L maximum demagnetization energy (V_{CC} = 13.5V)

Figure 28. SO-16L maximum turn-off current versus inductance

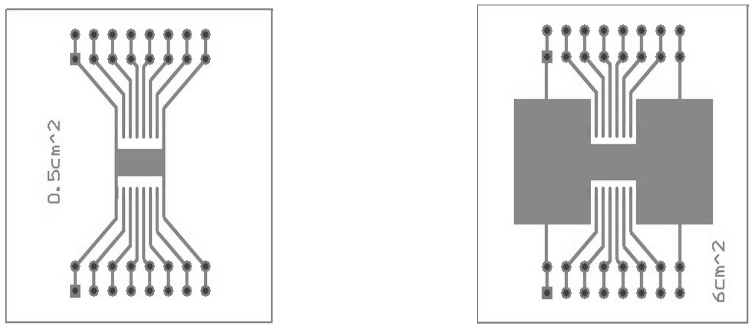


Note: Values are generated with R_L =0 Ω. In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

4 Package and PCB thermal data

4.1 SO-16L thermal data

Figure 29. SO-16L PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 41mm x 48mm, PCB thickness = 2mm, Cu thickness = 35µm, Copper areas: 0.5cm^2, 6cm^2).

Figure 30. SO-16L $R_{thj\text{-}amb}$ Vs PCB copper area in open box free air conditions

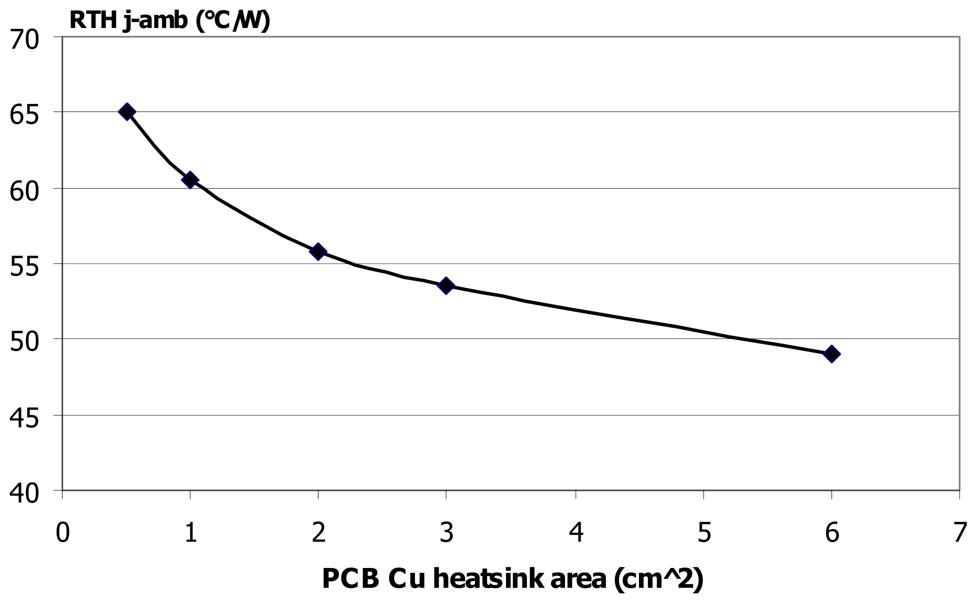
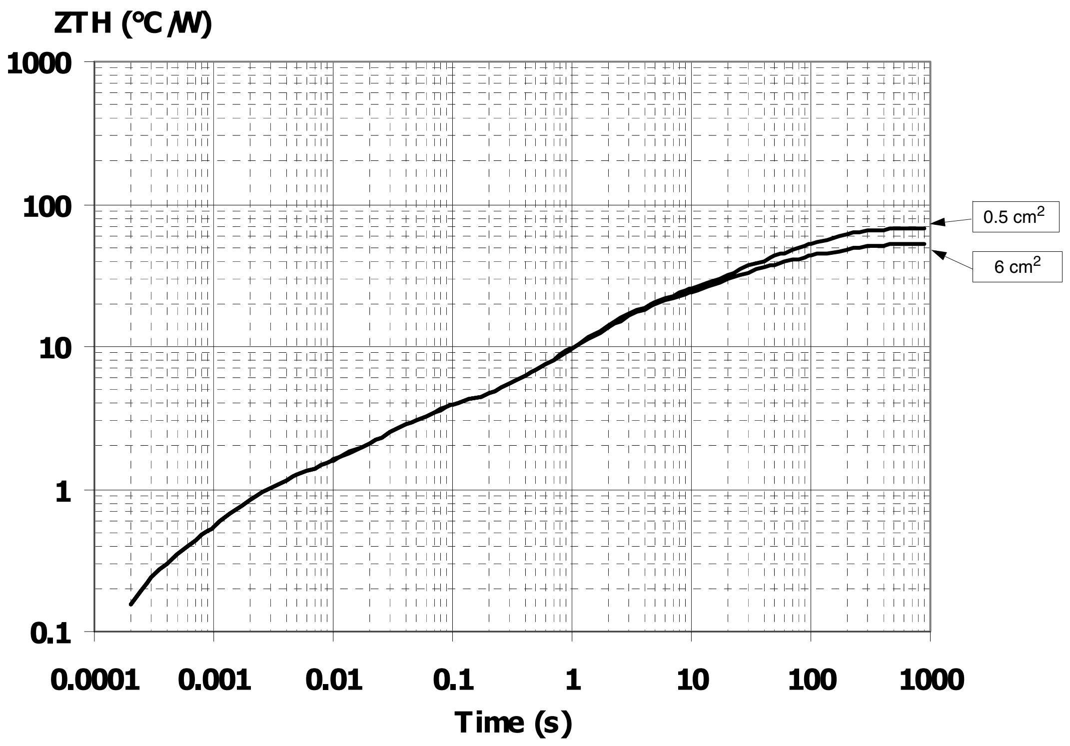


Figure 31. SO-16L thermal impedance junction ambient single pulse



Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1-\delta)$$

where $\delta = t_p / T$

Figure 32. Thermal fitting model of a single channel HSD in SO-16L

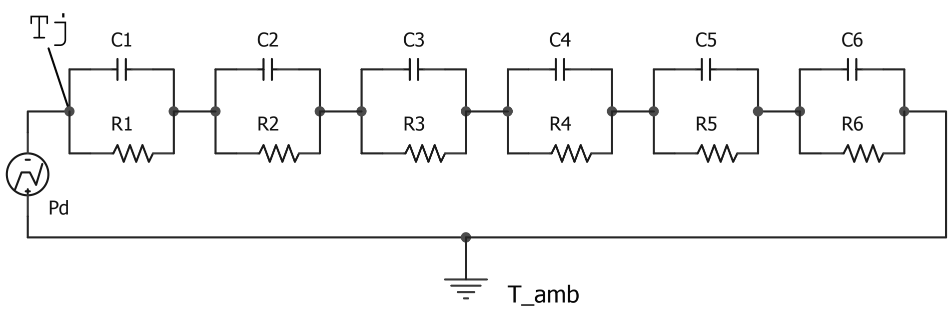
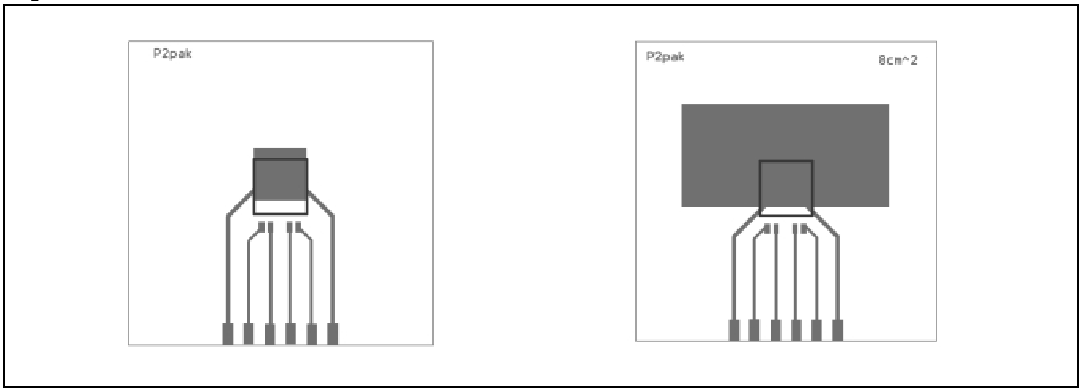


Table 14. SO-16L thermal parameters

Area / island (cm^2)	Footprint	6
R1 (°C/W)	0.04	
R2 (°C/W)	0.25	
R3 (°C/W)	2.2	
R4 (°C/W)	12	
R5 (°C/W)	15	
R6 (°C/W)	37	22
C1 (W.s/°C)	0.0008	
C2 (W.s/°C)	7E-03	
C3 (W.s/°C)	1.5E-02	
C4 (W.s/°C)	0.14	
C5 (W.s/°C)	1	
C6 (W.s/°C)	3	5

4.2 P²PAK thermal data

Figure 33. P²PAK PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 60mm x 60mm, PCB thickness = 2 mm, Cu thickness = 35µm , Copper areas: 0.97cm^2, 8cm^2).

Figure 34. P^2PAK $R_{thj-amb}$ Vs. PCB copper area in open box free air conditions

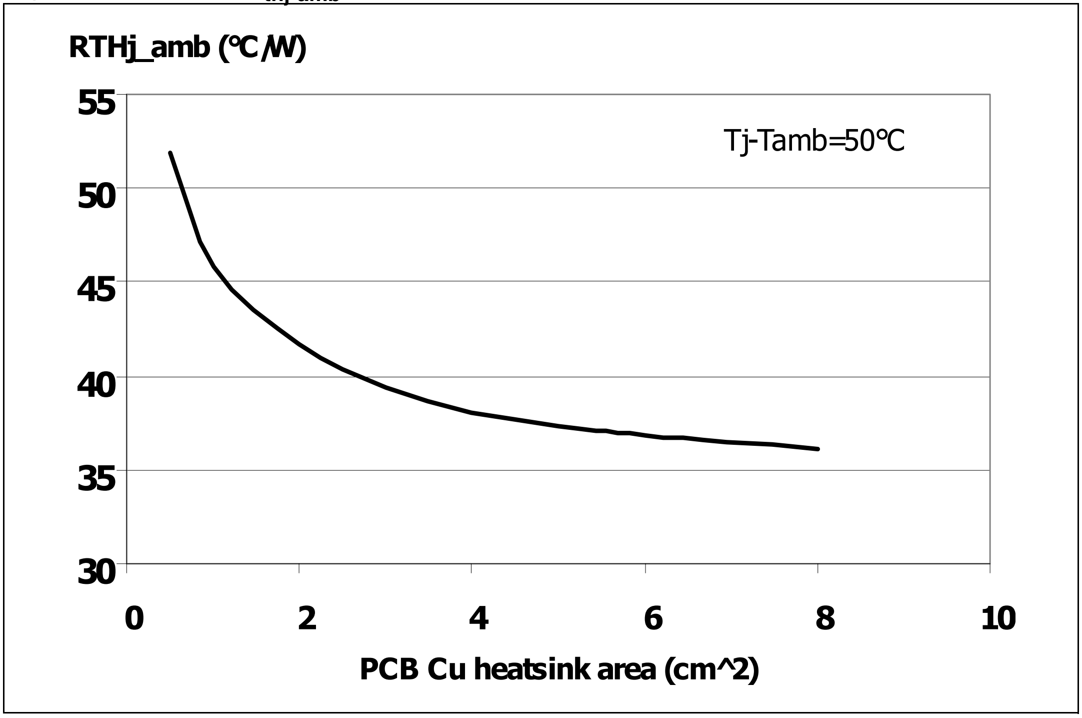
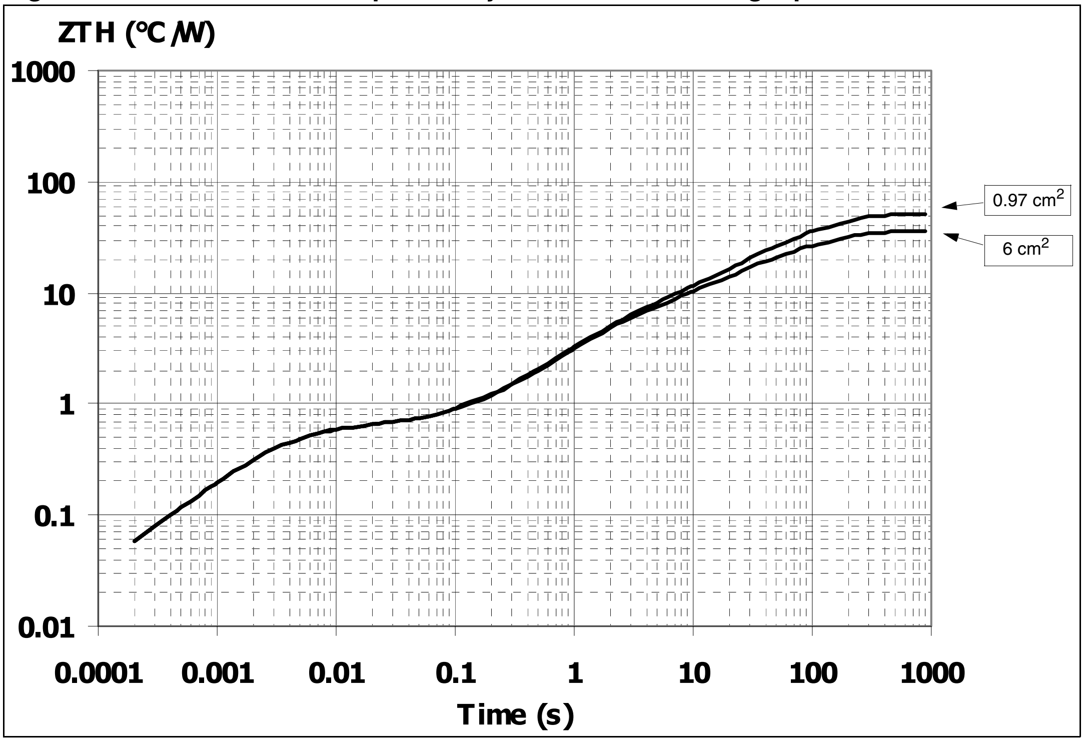


Figure 35. P^2PAK thermal impedance junction ambient single pulse



Equation 2: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_P/T$

Figure 36. Thermal fitting model of a single channel HSD in P^2PAK

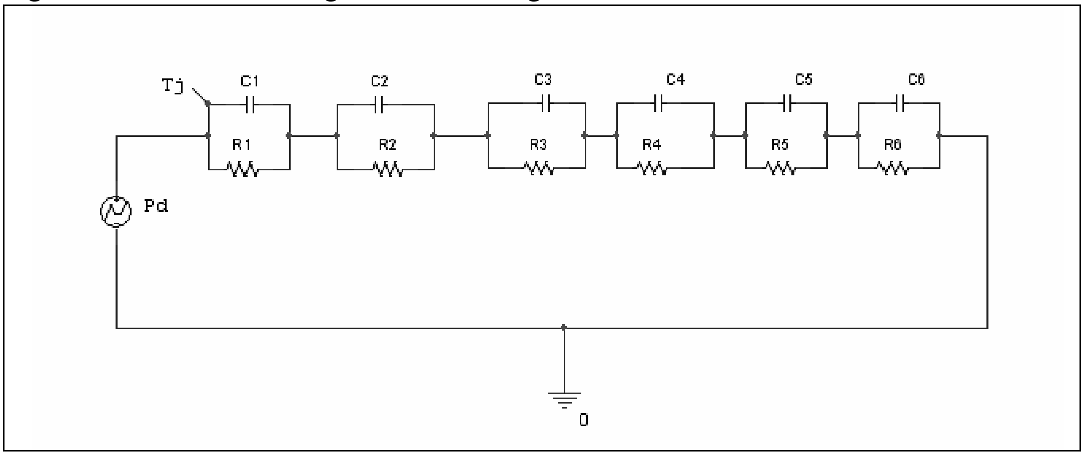
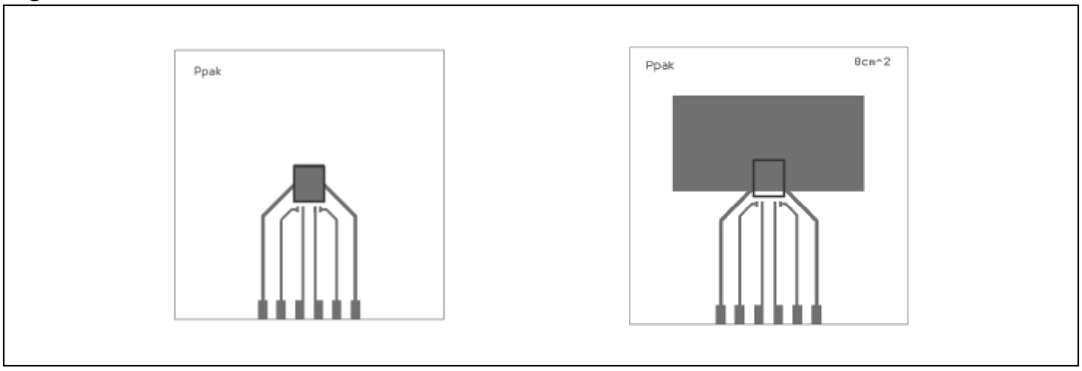


Table 15. P^2PAK thermal parameters

Area/island (cm^2)	0.97	6
R1 (°C/W)	0.04	
R2 (°C/W)	0.25	
R3 (°C/W)	0.3	
R4 (°C/W)	4	
R5 (°C/W)	9	
R6 (°C/W)	37	22
C1 (W·s/°C)	0.0008	
C2 (W·s/°C)	0.007	
C3 (W·s/°C)	0.015	
C4 (W·s/°C)	0.4	
C5 (W·s/°C)	2	
C6 (W·s/°C)	3	5

4.3 PPAK thermal data

Figure 37. PPAK PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 60mm x 60mm, PCB thickness = 2 mm, Cu thickness=35µm , Copper areas: 0.44 cm^2, 8 cm^2).

Figure 38. PPAK $R_{thj-amb}$ Vs. PCB copper area in open box free air conditions

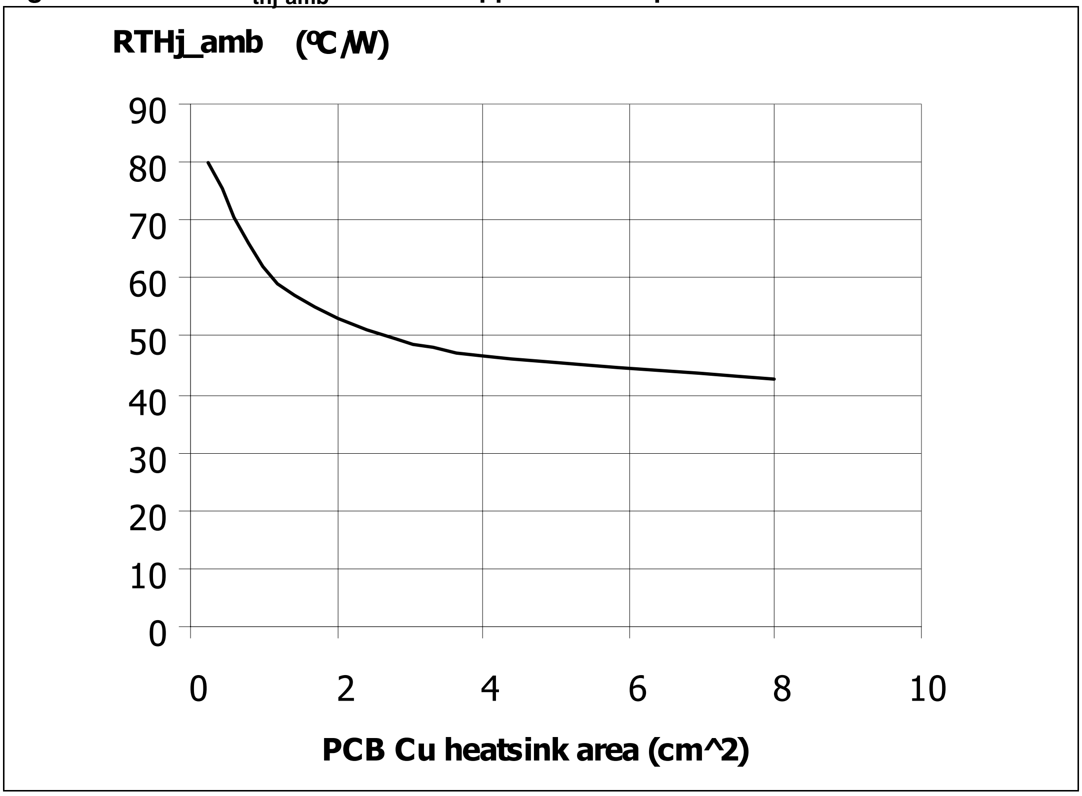
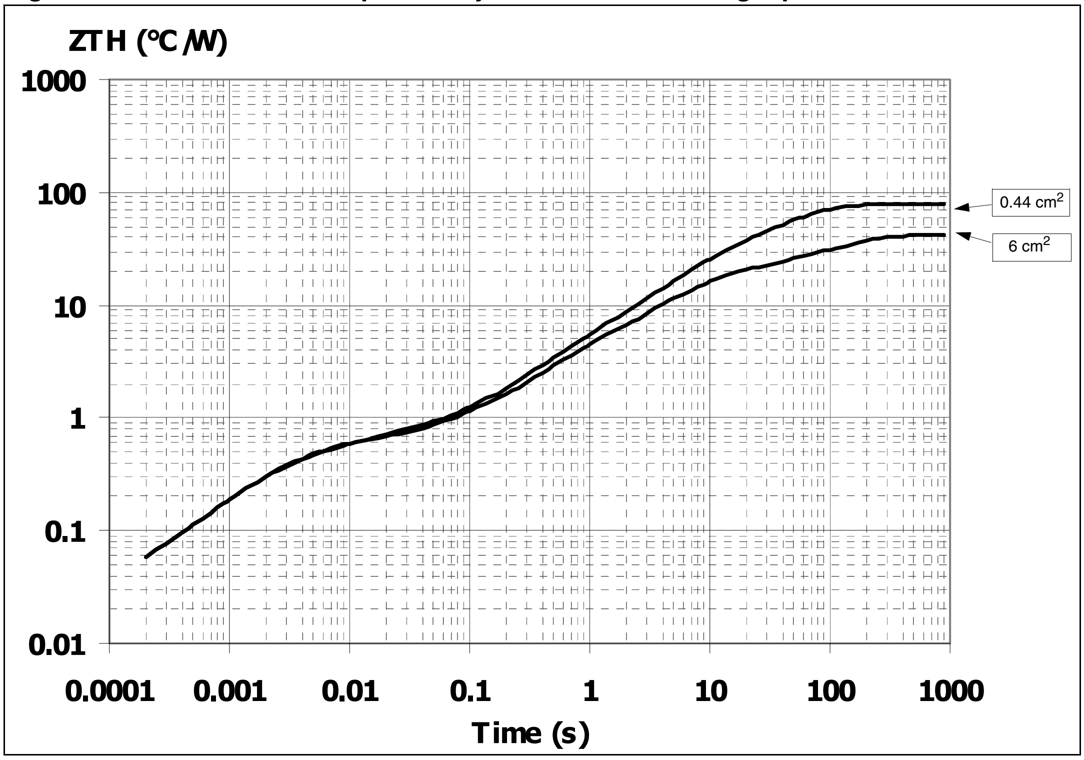


Figure 39. PPAK thermal impedance junction ambient single pulse



Equation 3: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_P/T$

Figure 40. Thermal fitting model of a single channel HSD in PPAK

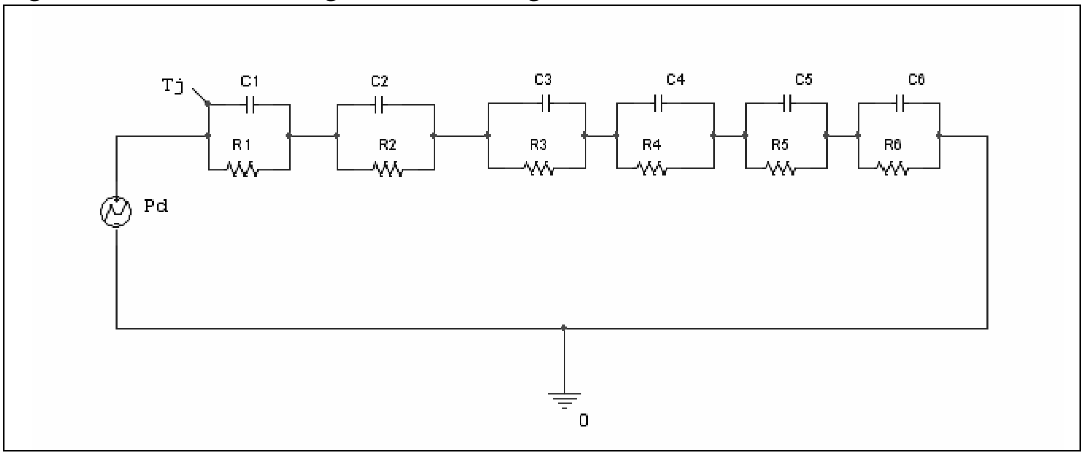
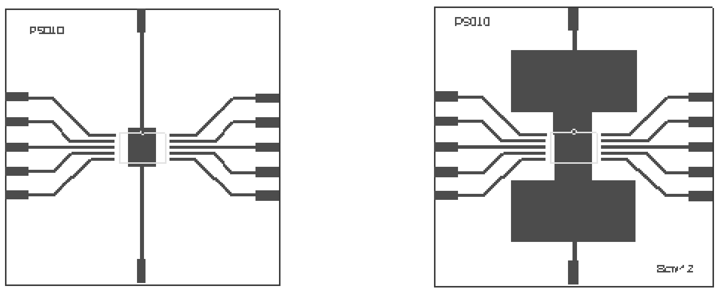


Table 16. PPAK thermal parameters

Area/island (cm^2)	0.44	6
R1 (°C/W)	0.04	
R2 (°C/W)	0.25	
R3 (°C/W)	0.3	
R4 (°C/W)	2	
R5 (°C/W)	15	
R6 (°C/W)	61	24
C1 (W·s/°C)	0.0008	
C2 (W·s/°C)	0.007	
C3 (W·s/°C)	0.02	
C4 (W·s/°C)	0.3	
C5 (W·s/°C)	0.45	
C6 (W·s/°C)	0.8	5

4.4 PowerSO-10 thermal data

Figure 41. PowerSO-10 PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 58mm x 58mm, PCB thickness = 2mm, Cu thickness = 35µm, Copper areas: from minimum pad lay-out to 8cm^2).

Figure 42. PowerSO-10 $R_{thj-amb}$ Vs PCB copper area in open box free air conditions

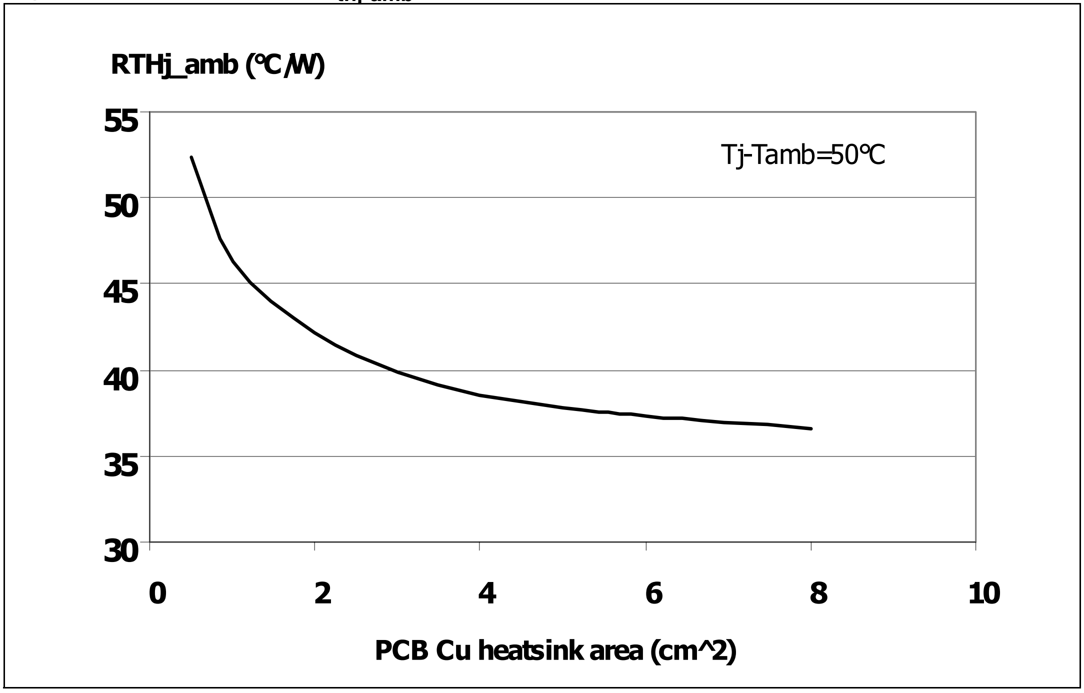
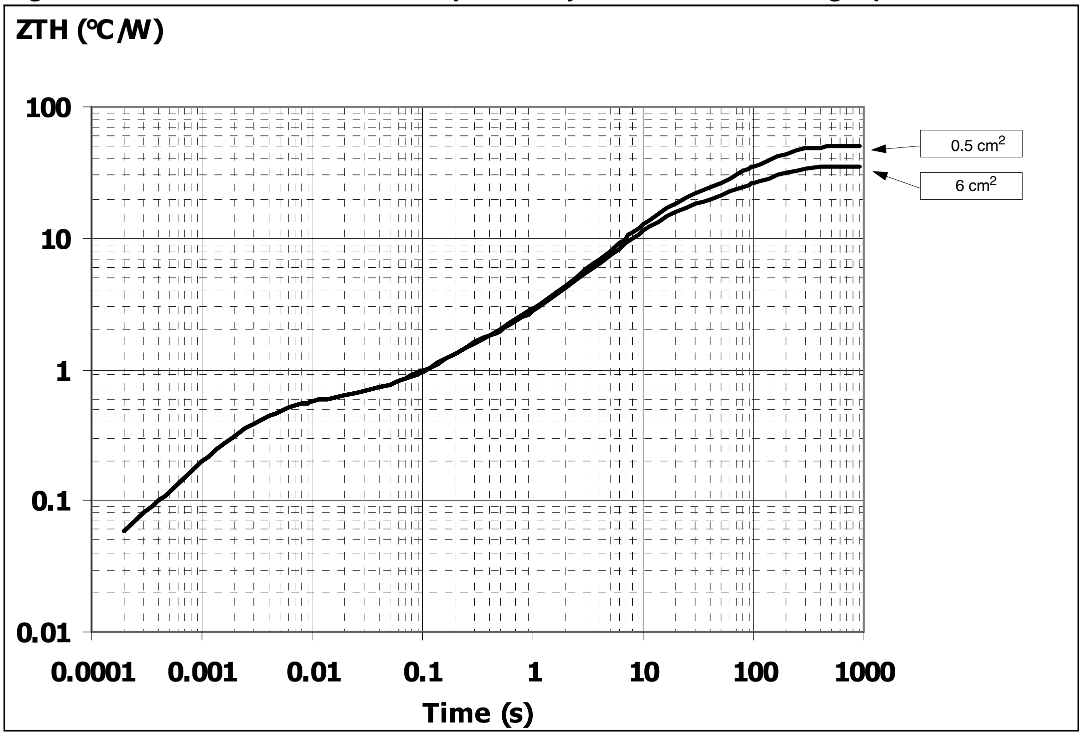


Figure 43. PowerSO-10 thermal impedance junction ambient single pulse



Equation 4: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p / T$

Figure 44. Thermal fitting model of a single channel HSD in PowerSO-10

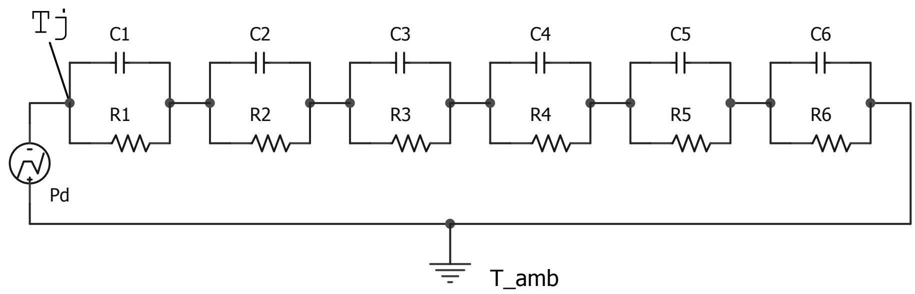


Table 17. PowerSO-10 thermal parameters

Area / island (cm^2)	Footprint	6
R1 (°C/W)	0.04	
R2 (°C/W)	0.25	
R3 (°C/W)	0.25	
R4 (°C/W)	0.8	
R5 (°C/W)	12	
R6 (°C/W)	37	22
C1 (W.s/°C)	0.0008	
C2 (W.s/°C)	7E-03	
C3 (W.s/°C)	0.015	
C4 (W.s/°C)	0.3	
C5 (W.s/°C)	0.75	
C6 (W.s/°C)	3	5

5 Package and packing information

5.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 45. SO-16L package dimensions

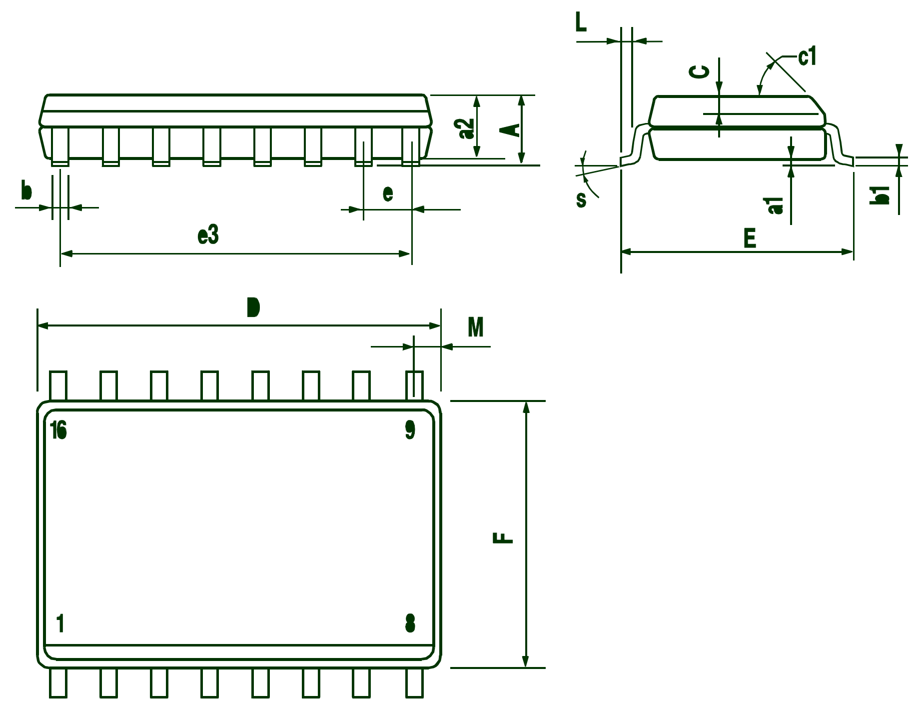


Table 18. SO-16L mechanical data

DIM.	mm.		
	Min.	Typ.	Max.
A			2.65
a1	0.1		0.2
a2			2.45
b	0.35		0.49
b1	0.23		0.32
C		0.5	
c1	45° (typ.)		

Table 18. SO-16L mechanical data (continued)

DIM.	mm.		
	Min.	Typ.	Max.
D	10.1		10.5
E	10.0		10.65
e		1.27	
e3		8.89	
F	7.4		7.6
L	0.5		1.27
M			0.75
S	8° (max.)		

5.2 PENTAWATT mechanical data

Figure 46. PENTAWATT package dimensions

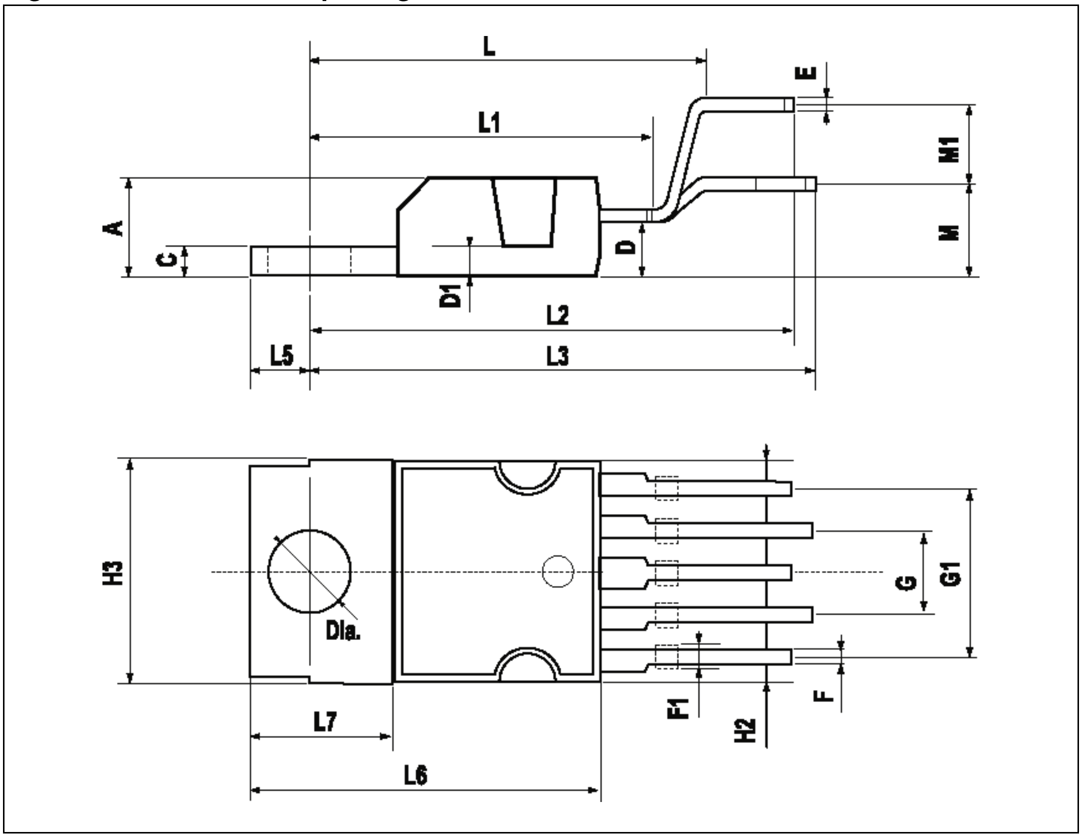


Table 19. PENTAWATT mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			4.8
C			1.37
D	2.4		2.8
D1	1.2		1.35
E	0.35		0.55
F	0.8		1.05
F1	1		1.4
G	3.2	3.4	3.6
G1	6.6	6.8	7
H2			10.4
H3	10.05		10.4
L		17.85	
L1		15.75	
L2		21.4	
L3		22.5	
L5	2.6		3
L6	15.1		15.8
L7	6		6.6
M		4.5	
M1		4	
Diam.	3.65		3.85

5.3 P2PAK mechanical data

Figure 47. P2PAK package dimensions

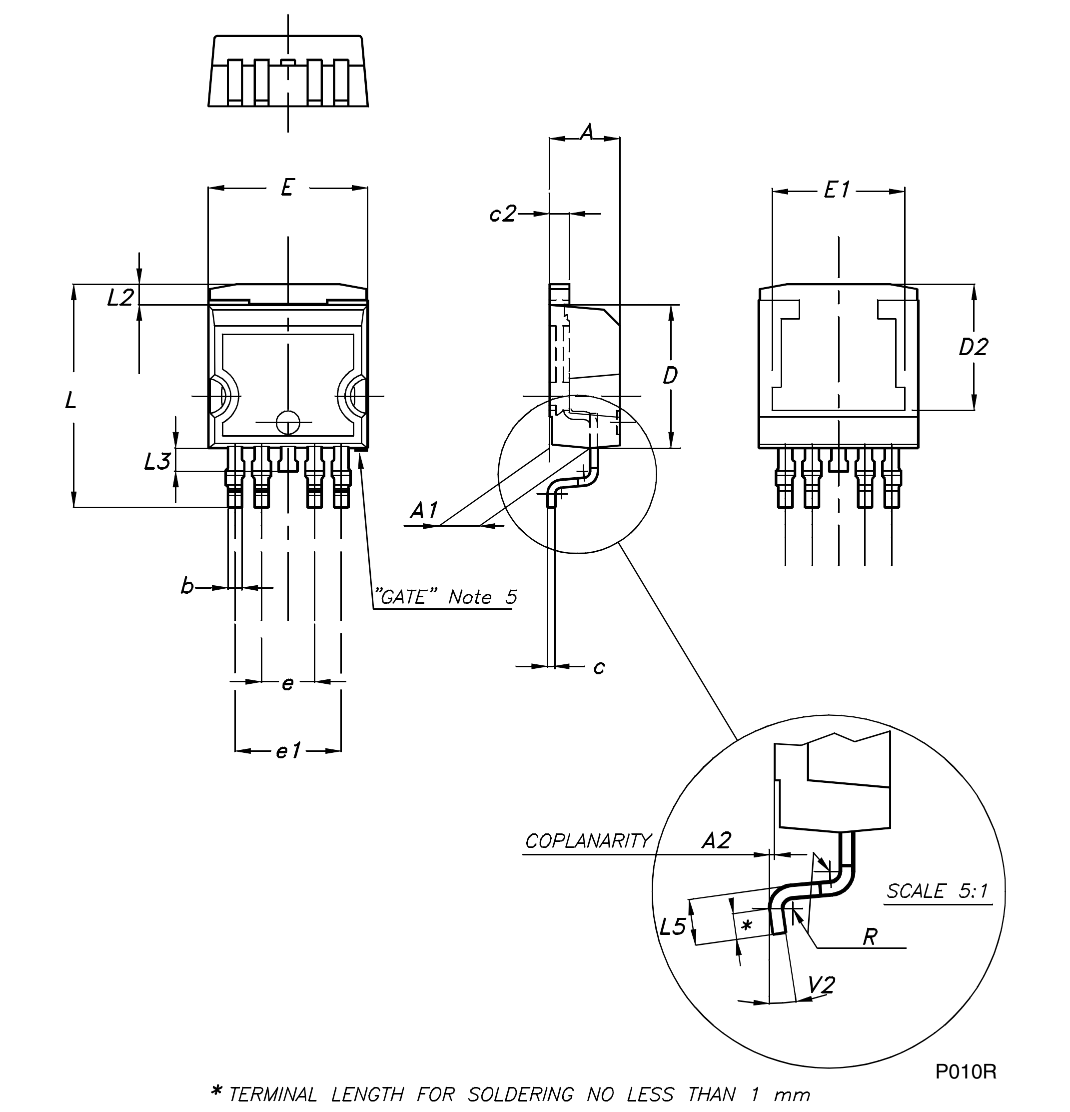


Table 20. P^2PAK mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30		4.80
A1	2.40		2.80
A2	0.03		0.23
b	0.80		1.05
c	0.45		0.60
c2	1.17		1.37
D	8.95		9.35
D2		8.00	
E	10.00		10.40
E1		8.50	
e	3.20		3.60
e1	6.60		7.00
L	13.70		14.50
L2	1.25		1.40
L3	0.90		1.70
L5	1.55		2.40
R		0.40	
V2	0º		8º
Package weight	1.40 Gr (typ)		

5.4 PPAK mechanical data

Figure 48. PPAK package dimensions

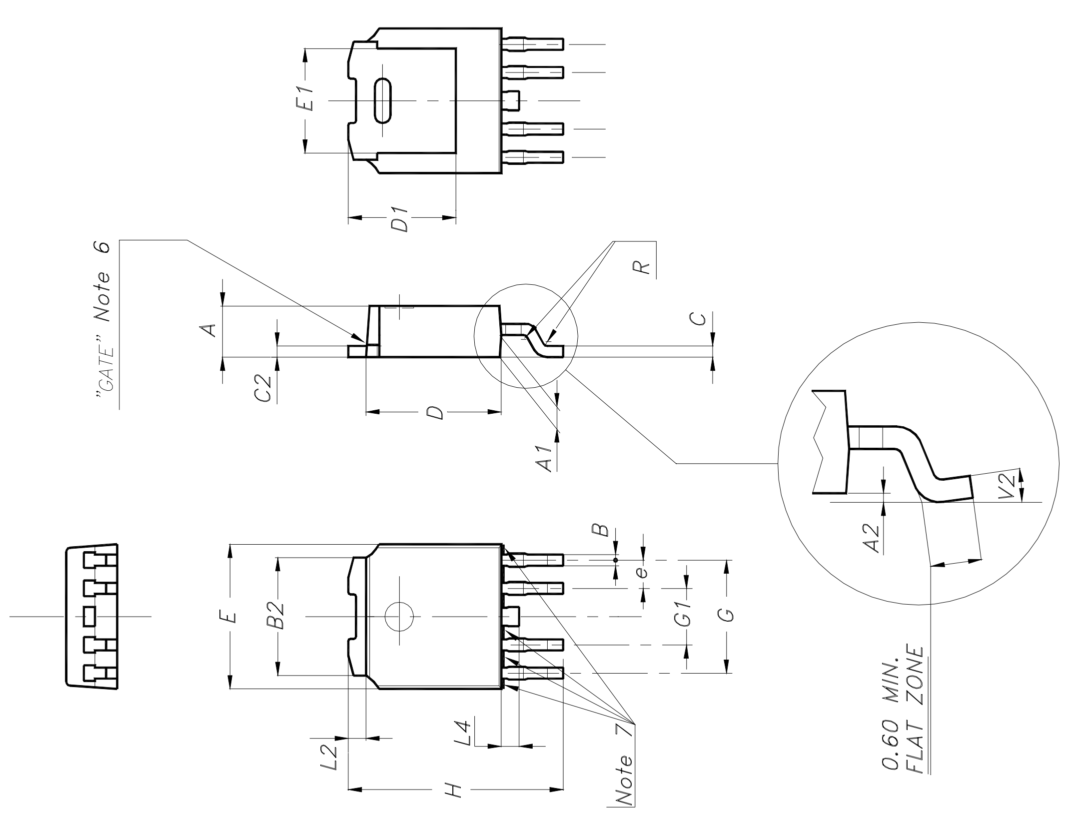


Table 21. PPAK mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
B	0.40		0.60
B2	5.20		5.40
C	0.45		0.60
C2	0.48		0.60
D1		5.1	
D	6.00		6.20
E	6.40		6.60

Table 21. PPAK mechanical data (continued)

Dim.	mm		
	Min.	Typ.	Max.
E1		4.7	
e		1.27	
G	4.90		5.25
G1	2.38		2.70
H	9.35		10.10
L2		0.8	1.00
L4	0.60		1.00
R		0.2	
V2	0º		8º
Package weight	Gr. 0.3		

5.5 PowerSO-10 mechanical data

Figure 49. PowerSO-10 package dimensions

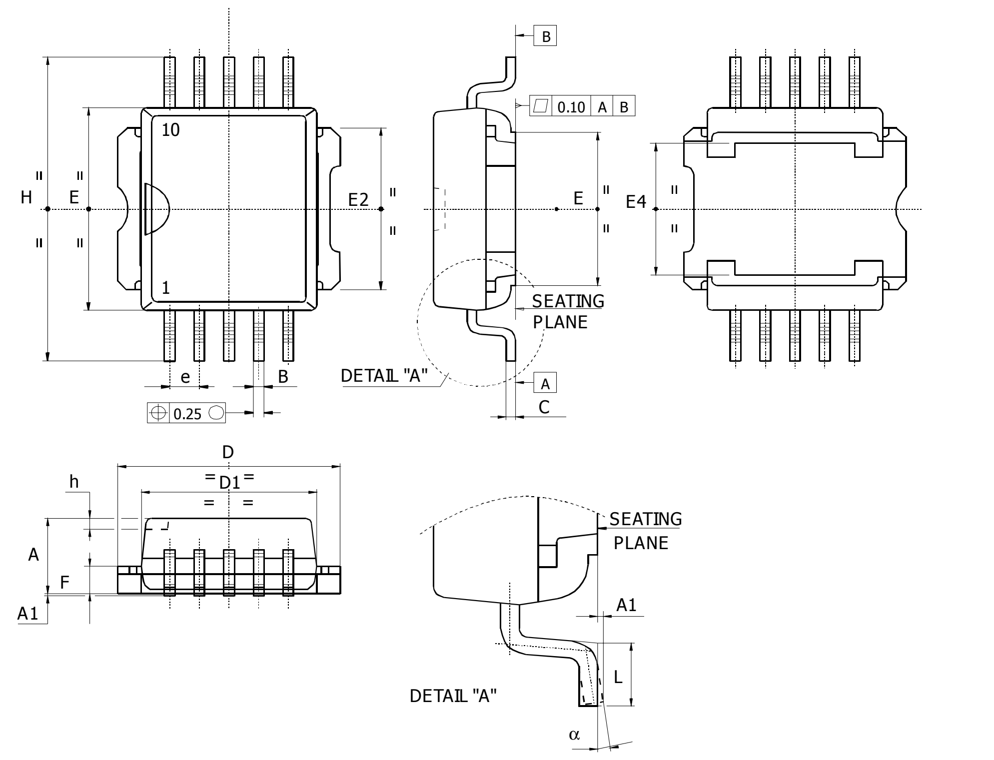


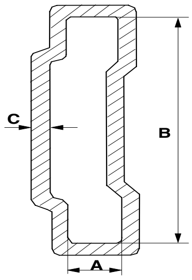
Table 22. PowerSO-10 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	3.35		3.65
A(1)	3.4		3.6
A1	0		0.10
B	0.40		0.60
B(1)	0.37		0.53
C	0.35		0.55
C(1)	0.23		0.32
D	9.40		9.60
D1	7.40		7.60
E	9.30		9.50
E2	7.20		7.60
E2(1)	7.30		7.50
E4	5.90		6.10
E4(1)	5.90		6.30
e		1.27	
F	1.25		1.35
F(1)	1.20		1.40
H	13.80		14.40
H(1)	13.85		14.35
h		0.50	
L	1.20		1.80
L(1)	0.80		1.10
α	0°		8°
α(1)	2°		8°

1. Muar only POA P013P.

5.6 SO-16L packing information

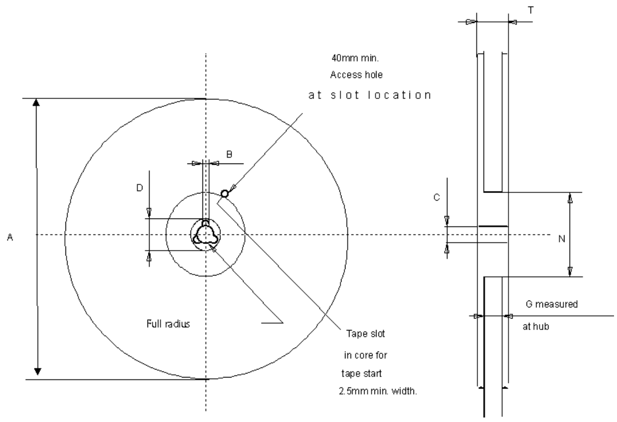
Figure 50. SO-16L tube shipment (no suffix)



Base Q.ty	50
Bulk Q.ty	1000
Tube length (± 0.5)	532
A	3.5
B	13.8
C (± 0.1)	0.6

All dimensions are in mm.

Figure 51. SO-16L tape and reel shipment (suffix "TR")



Reel dimensions

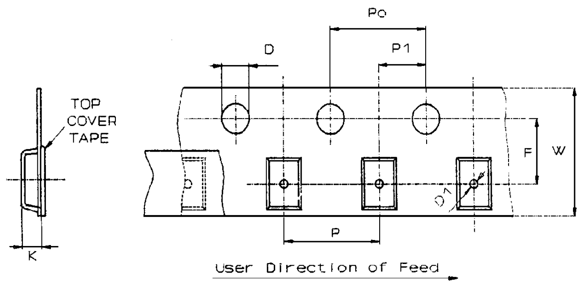
Base Q.ty	1000
Bulk Q.ty	1000
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	16.4
N (min)	60
T (max)	22.4

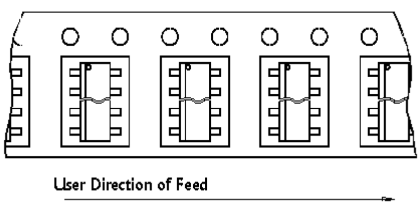
Tape dimensions

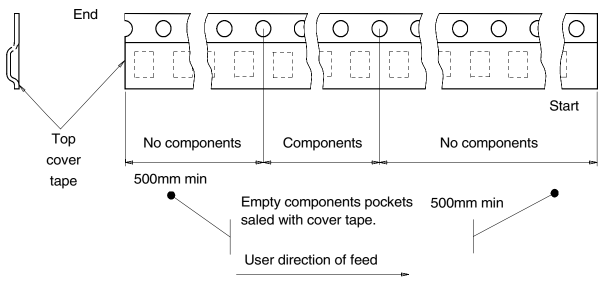
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	**W**	16
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	12
Hole Diameter	**D (± 0.1/-0)**	1.5
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.05)**	7.5
Compartment Depth	**K (max)**	6.5
Hole Spacing	**P1 (± 0.1)**	2

All dimensions are in mm.

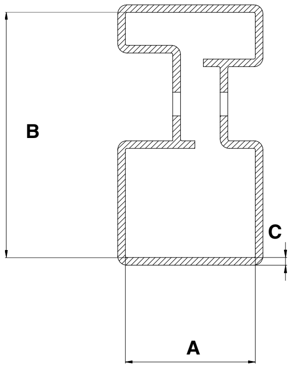






5.7 PENTAWATT packing information

Figure 52. PENTAWATT tube shipment (no suffix)

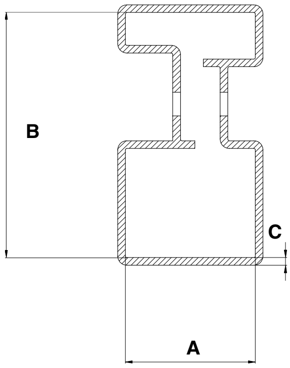


Base Q.ty	50
Bulk Q.ty	1000
Tube length (± 0.5)	532
A	18
B	33.1
C (± 0.1)	1

All dimensions are in mm.

5.8 P^2PAK packing information

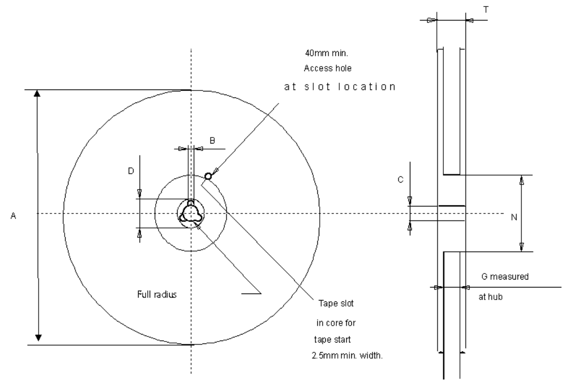
Figure 53. P^2PAK tube shipment (no suffix)



Base Q.ty	50
Bulk Q.ty	1000
Tube length (± 0.5)	532
A	18
B	33.1
C (± 0.1)	1

All dimensions are in mm.

Figure 54. P^2PAK tape and reel (suffix "13TR")



REEL DIMENSIONS

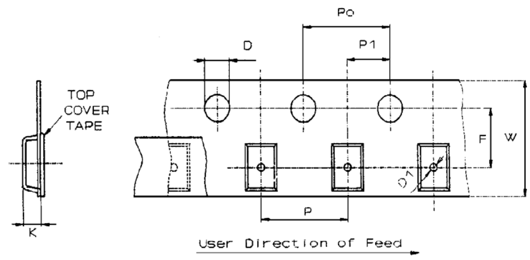
All dimensions are in mm.

Base Q.ty	1000
Bulk Q.ty	1000
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	24.4
N (min)	60
T (max)	30.4

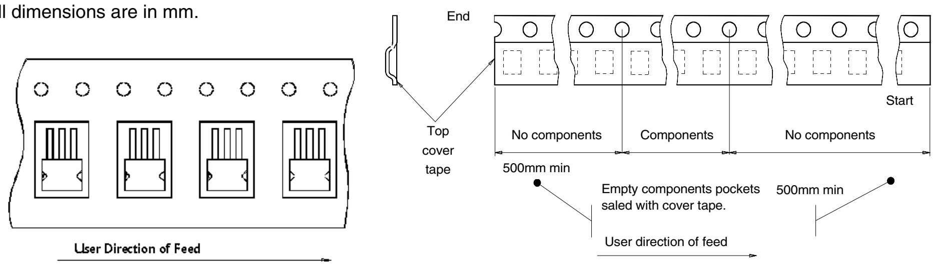
TAPE DIMENSIONS

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

Tape width	**W**	24
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	12
Hole Diameter	**D (± 0.1/-0)**	1.5
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.05)**	11.5
Compartment Depth	**K (max)**	6.5
Hole Spacing	**P1 (± 0.1)**	2



All dimensions are in mm.



5.9 PPAK packing information

Figure 55. PPAK suggested pad layout

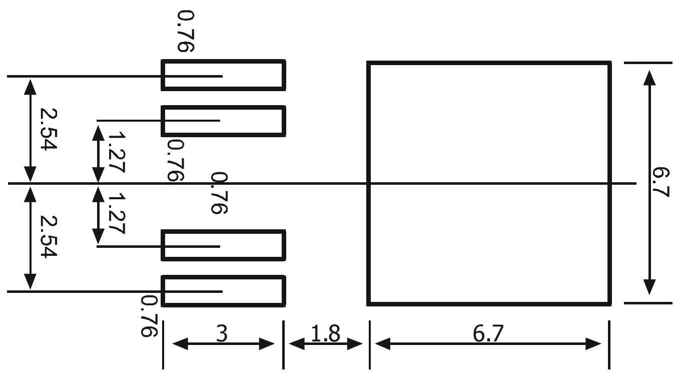
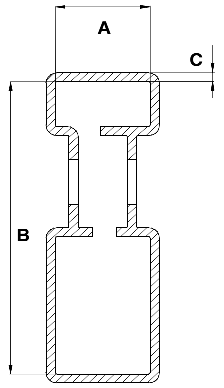


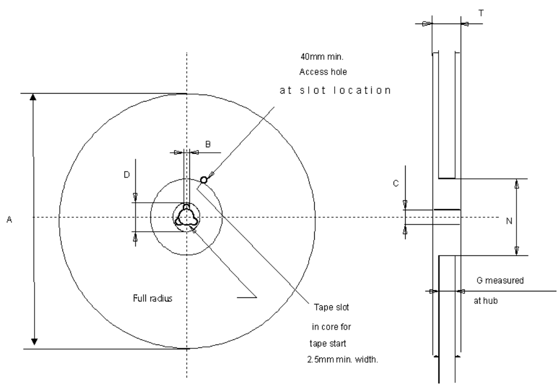
Figure 56. PPAK tube shipment (no suffix)



Base Q.ty	75
Bulk Q.ty	3000
Tube length (± 0.5)	532
A	6
B	21.3
C (± 0.1)	0.6

All dimensions are in mm.

Figure 57. PPAK tape and reel (suffix “13TR”)



REEL DIMENSIONS

All dimensions are in mm.

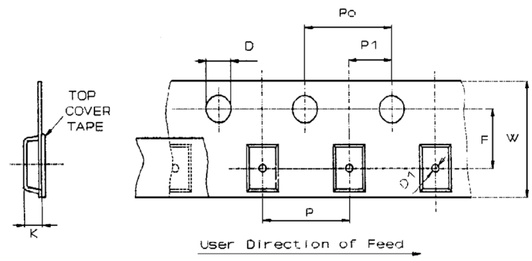
Base Q.ty	2500
Bulk Q.ty	2500
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	16.4
N (min)	60
T (max)	22.4

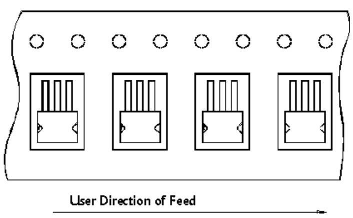
TAPE DIMENSIONS

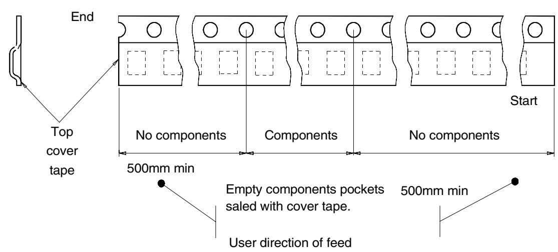
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

Tape width	W	16
Tape Hole Spacing	P0 (± 0.1)	4
Component Spacing	P	8
Hole Diameter	D (± 0.1/-0)	1.5
Hole Diameter	D1 (min)	1.5
Hole Position	F (± 0.05)	7.5
Compartment Depth	K (max)	2.75
Hole Spacing	P1 (± 0.1)	2

All dimensions are in mm.







5.10 PowerSO-10 packing information

Figure 58. PowerSO-10 suggested pad layout

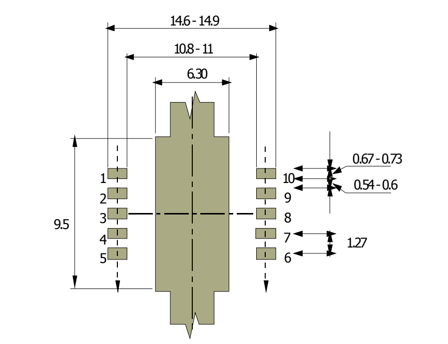
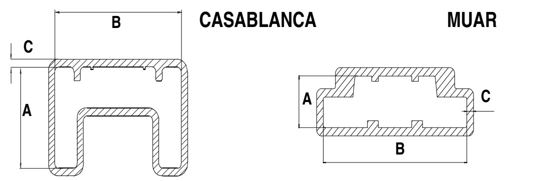


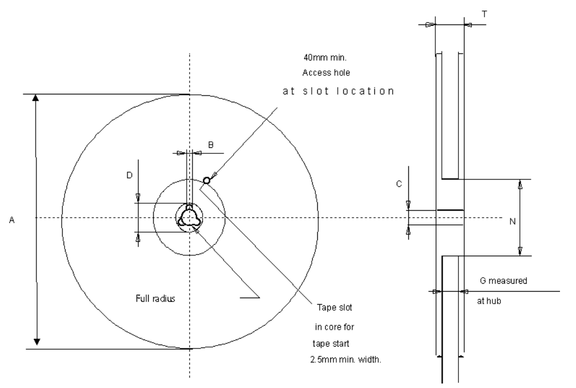
Figure 59. PowerSO-10 tube shipment (no suffix)



All dimensions are in mm.

	Base Q.ty	Bulk Q.ty	Tube length (± 0.5)	A	B	C (± 0.1)
Casablanca	50	1000	532	10.4	16.4	0.8
Muar	50	1000	532	4.9	17.2	0.8

Figure 60. PowerSO-10 tape and reel shipment (suffix “TR”)



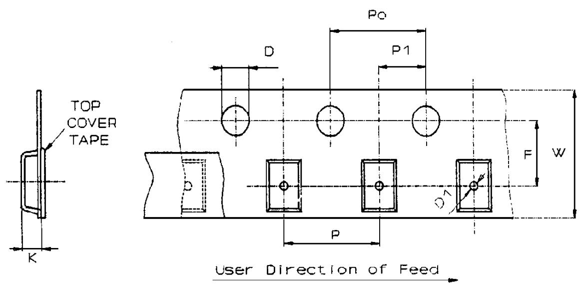
Reel dimensions

Base Q.ty	600
Bulk Q.ty	600
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	24.4
N (min)	60
T (max)	30.4

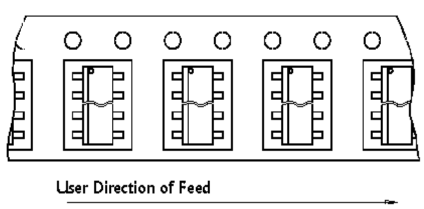
Tape dimensions

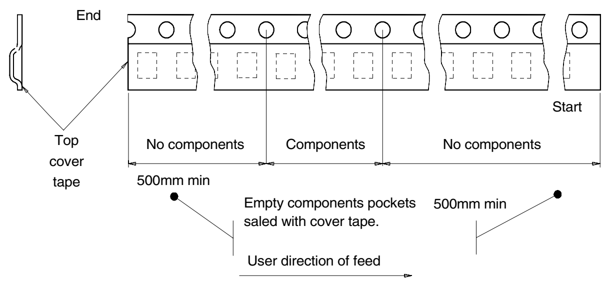
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	W	24
Tape Hole Spacing	P0 (± 0.1)	4
Component Spacing	P	24
Hole Diameter	D (± 0.1/-0)	1.5
Hole Diameter	D1 (min)	1.5
Hole Position	F (± 0.05)	11.5
Compartment Depth	K (max)	6.5
Hole Spacing	P1 (± 0.1)	2



All dimensions are in mm.





6 Revision history

Table 23. Document revision history

Date	Revision	Changes
07-Dec-2004	1	Initial release.
09-Feb-2005	2	Text changed.
23-Mar-2005	3	Configuration diagram (PowerSO-10) modification.
03-May-2006	4	SO-16L mechanical and shipment data insertion.
17-Dec-2008	5	Document reformatted and restructured. Added content, list of figures and tables. Added *ECOPACK® packages* information. Updated *Figure 54.: P^2PAK tape and reel (suffix “13TR”)*: – changed component spacing (P) in tape dimensions table from 16 mm to 12 mm.