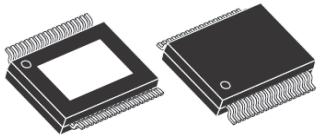
VND7012AY-E

Double channel high-side driver with MultiSense analog feedback for automotive applications

Datasheet - target specification



PowerSSO-36

Features

Max transient supply voltage	V_{CC}	41 V
Operating voltage range	V_{CC}	4 to 28 V
Typ. on-state resistance (per Ch)	R_{ON}	12 mΩ
Current limitation (typ)	I_{LIMH}	75 A
Standby current (max)	I_{STBY}	0.5 µA

- General
  - Double channel smart high side driver with MultiSense analog feedback
  - Very low standby current
  - Compatible with 3 V and 5 V CMOS outputs
- MultiSense diagnostic functions
  - Multiplexed analog feedback of: load current with high precision proportional current mirror, V_{CC} supply voltage and T_{CHIP} device temperature
  - Overload and short to ground (power limitation) indication
  - Thermal shutdown indication
  - Off-state open-load detection
  - Output short to V_{CC} detection
  - Sense enable/ disable
- Protections
  - Undervoltage shutdown
  - Overvoltage clamp
  - Load current limitation
  - Self limiting of fast thermal transients
  - Configurable latch-off on overtemperature or power limitation with dedicated fault reset pin
  - Loss of ground and loss of V_{CC}
  - Reverse battery through self turn-on
  - Electrostatic discharge protection

Applications

- All types of Automotive resistive, inductive and capacitive loads
- Specially intended for Automotive Turn Indicators (up to 3 x P27W or SAE1156 and 2 x R5W paralleled or Automotive Headlamps)

Description

The VND7012AY-E is a double channel high-side driver manufactured using ST proprietary VIPower® M0-7 technology and housed in PowerSSO-36 package. The device is designed to drive 12 V automotive grounded loads through a 3 V and 5 V CMOS-compatible interface, providing protection and diagnostics.

The device integrates advanced protective functions such as load current limitation, overload active management by power limitation and overtemperature shutdown with configurable latch-off.

A $\overline{\text{FaultRST}}$ pin unlatches the output in case of fault or disables the latch-off functionality.

A dedicated multifunction multiplexed analog output pin delivers sophisticated diagnostic functions including high precision proportional load current sense, supply voltage feedback and chip temperature sense, in addition to the detection of overload and short circuit to ground, short to V_{CC} and off-state open-load.

A sense enable pin allows off-state diagnosis to be disabled during the module low-power mode as well as external sense resistor sharing among similar devices.

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1 Block diagram and pin description

Figure 1. Block diagram

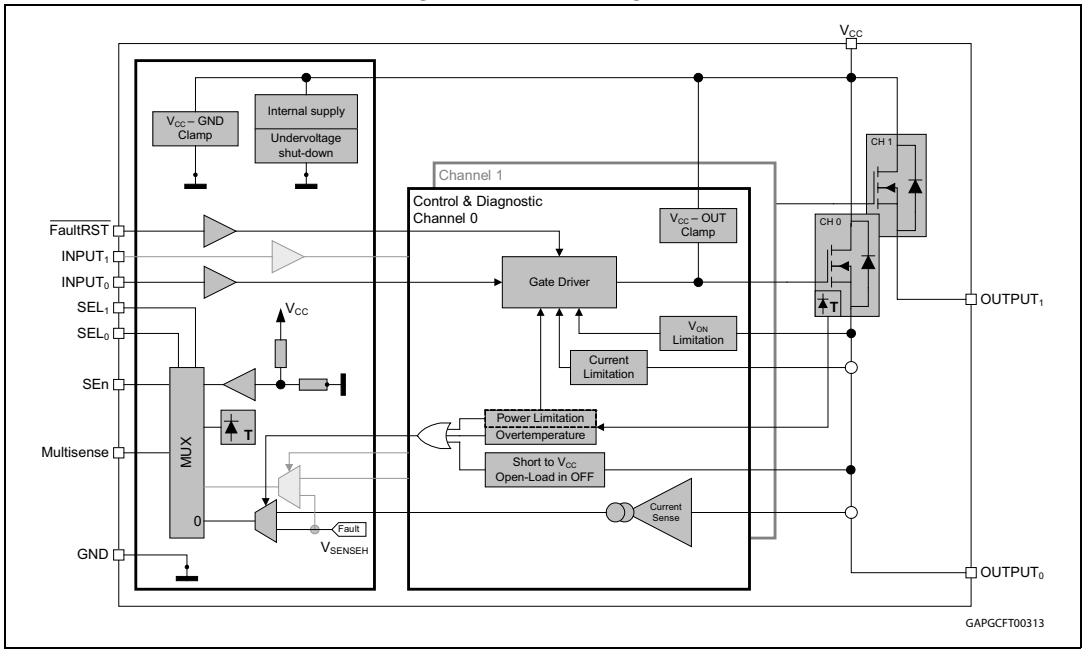


Table 1. Pin functions

Name	Function
V_{CC}	Battery connection.
$OUTPUT_{0,1}$	Power output.
GND	Ground connection.
$INPUT_{0,1}$	Voltage controlled input pin with hysteresis, compatible with 3V and 5V CMOS outputs. They control output switch state.
MultiSense	Multiplexed analog sense output pin; delivers a current proportional to the selected diagnostic: load current, supply voltage or chip temperature.
SEn	Active high compatible with 3V and 5V CMOS outputs; it enables the MultiSense diagnostic pin.
$SEL_{0,1}$	Active high compatible with 3V and 5V CMOS outputs; they address the MultiSense multiplexer.
$\overline{\text{FaultRST}}$	Active low compatible with 3V and 5V CMOS outputs; unlatches the output in case of fault; if kept low, sets the outputs in auto-restart mode.

Figure 2. Configuration diagram (top view)

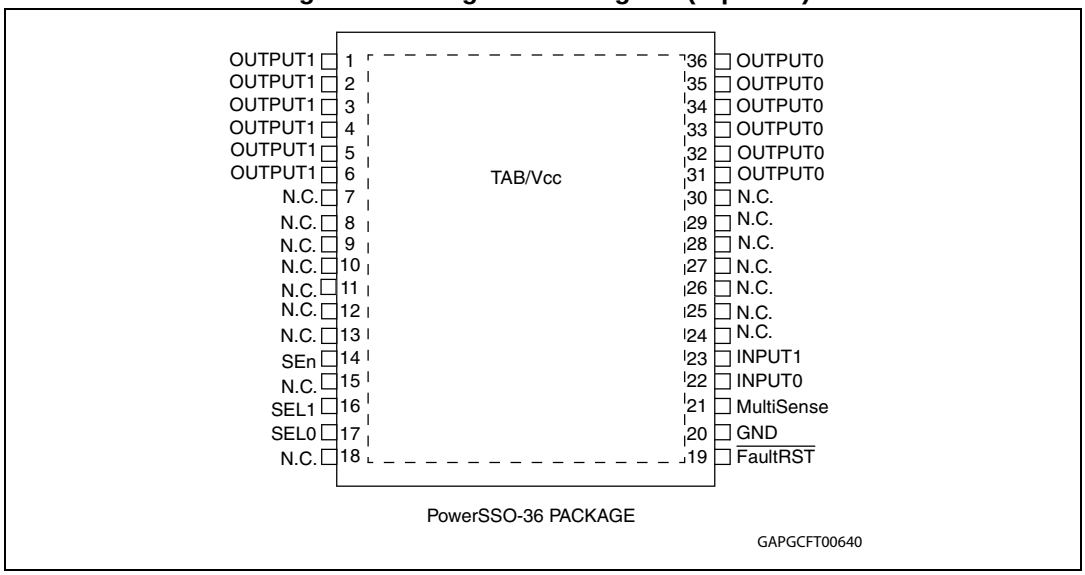


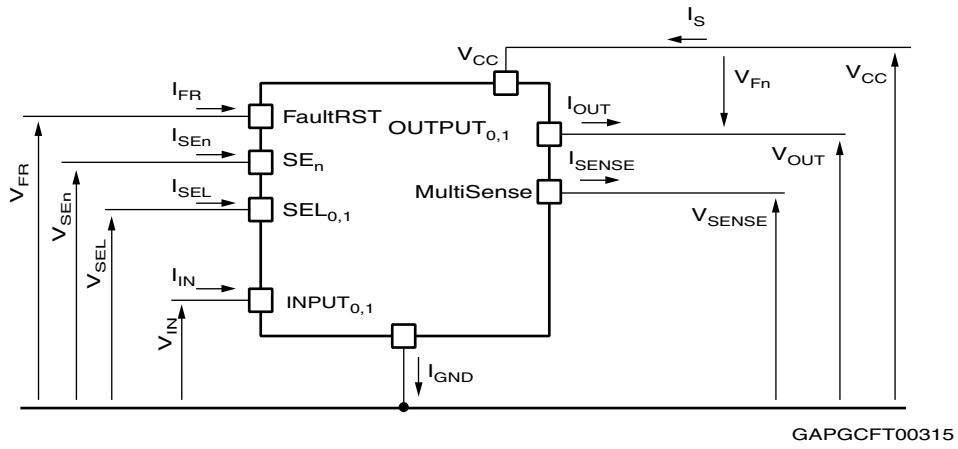
Table 2. Suggested connections for unused and not connected pins

Connection/pin	MultiSense	N.C.	Output	Input	SEn, SELx, $\overline{\text{FaultRST}}$
Floating	Not allowed	X(1)	X	X	X
To ground	Through 1 kΩ resistor	X	Not allowed	Through 15 kΩ resistor	Through 15 kΩ resistor

1. X: do not care.

2 Electrical specification

Figure 3. Current and voltage conventions



Note: $V_{Fn} = V_{OUTn} - V_{CC}$ during reverse battery condition.

2.1 Absolute maximum ratings

Stressing the device above the rating listed in *Table 3* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	38	V
$-V_{CC}$	Reverse DC supply voltage	16	
V_{CCPK}	Maximum transient supply voltage (ISO7637-2:2004 Pulse 5b level IV clamped to 40 V; R_L = 4 Ω)	40	
V_{CCJS}	Maximum jump start voltage for single pulse short circuit protection	28	
$-I_{GND}$	DC reverse ground pin current	200	mA
I_{OUT}	$OUTPUT_{0,1}$ DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	22	
I_{IN}	$INPUT_{0,1}$ DC input current	-1 to 10	mA
I_{SEn}	SEn DC input current		
I_{SEL}	$SEL_{0,1}$ DC input current		
I_{FR}	FaultRST DC input current		

Table 3. Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
V_{FR}	FaultRST DC input voltage	7.5	V
I_{SENSE}	MultiSense pin DC output current (V_{GND} = V_{CC} and V_{SENSE} < 0 V)	10	mA
	MultiSense pin DC output current in reverse (V_{CC} < 0 V)	-20	
E_{MAX}	Maximum switching energy (single pulse) (T_{DEMAG} = 0.4 ms; T_{jstart} = 150°C)	TBD	mJ
V_{ESD}	Electrostatic discharge (JDEC 22 A-114 F) – $INPUT_{0,1}$ – MultiSense – SEn, $SEL_{0,1}$, FaultRST – $OUTPUT_{0,1}$ – V_{CC}	 4000 2000 4000 4000 4000	 V V V V V
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T_j	Junction operating temperature	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Typ. value	Unit
$R_{thj\text{-}board}$	Thermal resistance junction-board (JEDEC JESD 51-5 / 51-8)(1)(2)	TBD	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient (JEDEC JESD 51-5)(1)(3)	TBD	
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient (JEDEC JESD 51-7)(1)(2)	TBD	

1. One channel ON.
2. Device mounted on four-layers 2s2p PCB
3. Device mounted on two-layers 2s0p PCB with 2 cm^2 heatsink copper trace

2.3 Main electrical characteristics

7 V < V_{CC} < 28 V; -40°C < T_j < 150°C, unless otherwise specified.

All typical values refer to V_{CC} = 13 V; T_j = 25°C, unless otherwise specified.

Table 5. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4	13	28	V
V_{USD}	Undervoltage shutdown				4	
$V_{USDReset}$	Undervoltage shutdown reset				5	
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.3		
R_{ON}	On-state resistance(1)	I_{OUT} = 7 A; T_j = 25°C		12		mΩ
		I_{OUT} = 7 A; T_j = 150°C			24	
		I_{OUT} = 7 A; V_{CC} = 4 V; T_j = 25°C			18	
R_{ON_REV}	On-state resistance in reverse battery	I_{OUT} = -7 A; V_{CC} = -13 V; T_j = 25°C		12		mΩ
V_{clamp}	Clamp voltage	I_S = 20 mA; 25°C < T_j < 150°C	41	46	52	V
		I_S = 20 mA; T_j = -40 °C	38			V
I_{STBY}	Supply current in standby at V_{CC} = 13 V (2)	V_{CC} = 13 V; $V_{IN0,1}$ = $V_{OUT0,1}$ = V_{FR} = V_{SEn} 0 V; $V_{SEL0,1}$ = 0 V; T_j = 25°C			0.5	µA
		V_{CC} = 13 V; $V_{IN0,1}$ = $V_{OUT0,1}$ = V_{FR} = V_{SEn} 0 V; $V_{SEL0,1}$ = 0 V; T_j = 85°C (3)			0.5	µA
		V_{CC} = 13 V; $V_{IN0,1}$ = $V_{OUT0,1}$ = V_{FR} = V_{SEn} 0 V; $V_{SEL0,1}$ = 0 V; T_j = 125°C			3	µA
t_{D_STBY}	Standby mode blanking time	V_{CC} = 13 V; $V_{IN0,1}$ = $V_{OUT0,1}$ = V_{FR} = $V_{SEL0,1}$ = 0 V; V_{SEn} = 5 V to 0 V	60	300	550	µA
$I_{S(ON)}$	Supply current	V_{CC} = 13 V; V_{SEn} = V_{FR} = $V_{SEL0,1}$ = 0 V; $V_{IN0,1}$ = 5 V; I_{OUT0} = 0 A; I_{OUT1} = 0 A		5	8	mA
$I_{GND(ON)}$	Control stage current consumption in ON state. All channels active.	V_{CC} = 13 V; V_{SEn} = 5 V; V_{FR} = $V_{SEL0,1}$ = 0 V; $V_{IN0,1}$ = 5 V; I_{OUT0} = 7 A; I_{OUT1} = 7 A			10	mA

Table 5. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{L(off)}$	Off-state output current at V_{CC} = 13 V (1)	$V_{IN0,1} = V_{OUT0,1}$ = 0 V; V_{CC} = 13 V; T_j = 25°C	0	0.01	0.5	µA
		$V_{IN0,1} = V_{OUT0,1}$ = 0 V; V_{CC} = 13 V; T_j = 125°C	0		3	
V_F	Output - V_{CC} diode voltage(1)	I_{OUT} = -2.5 A; T_j = 150 °C			0.7	V

1. For each channel.
2. PowerMOS leakage included.
3. Parameter specified by design; not subject to production test.

Table 6. Switching (V_{CC} = 13 V; -40 °C < T_j < 150 °C, unless otherwise specified)(1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time at T_j = 25 °C	R_L = 1.84 Ω	10	70	120	µs
$t_{d(off)}$	Turn-off delay time at T_j = 25 °C		10	50	100	
$(dV_{OUT}/dt)_{on}$	Turn-on voltage slope at T_j = 25 °C	R_L = 1.84 Ω	0.1	0.26	0.7	V/µs
$(dV_{OUT}/dt)_{off}$	Turn-off voltage slope at T_j = 25 °C		0.1	0.28	0.7	
W_{ON}	Switching energy losses at turn-on (t_{won})	R_L = 1.84 Ω	—	1	1.4(2)	mJ
W_{OFF}	Switching energy losses at turn-off (t_{woff})	R_L = 1.84 Ω	—	0.9	1.3(2)	mJ
t_{SKEW}	Differential pulse skew (t_{PHL} - t_{PLH}) see *Figure 4*	R_L = 1.84 Ω	-25	25	75	µs

1. See *Figure 4: Switching times and Pulse skew.*
2. Parameter guaranteed by design and characterization, not subject to production test.

Table 7. Logic Inputs (7 V < V_{CC} < 28 V; -40°C < T_j < 150°C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$INPUT_{0,1}$ characteristics						
V_{IL}	Input low level voltage				0.9	V
I_{IL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{IH}	Input high level voltage		2.1			V
I_{IH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{I(hyst)}$	Input hysteresis voltage		0.2			V
V_{ICL}	Input clamp voltage	I_{IN} = 1 mA	5.3		7.2	V
		I_{IN} = -1 mA		-0.7		
$\overline{\text{FaultRST}}$ characteristics						
V_{FRL}	Input low level voltage				0.9	V

Table 7. Logic Inputs (7 V < V_{CC} < 28 V; -40°C < T_j < 150°C) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{FRL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{FRH}	Input high level voltage		2.1			V
I_{FRH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{FR(hyst)}$	Input hysteresis voltage		0.2			V
V_{FRCL}	Input clamp voltage	I_{IN} = 1 mA	5.3		7.5	V
		I_{IN} = -1 mA		-0.7		
$SEL_{0,1}$ characteristics (7 V < V_{CC} < 18 V)						
V_{SELL}	Input low level voltage				0.9	V
I_{SELL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{SELH}	Input high level voltage		2.1			V
I_{SELH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{SEL(hyst)}$	Input hysteresis voltage		0.2			V
V_{SELCL}	Input clamp voltage	I_{IN} = 1 mA	5.3		7.2	V
		I_{IN} = -1 mA		-0.7		
SEn characteristics (7 V < V_{CC} < 18 V)						
V_{SEnL}	Input low level voltage				0.9	V
I_{SEnL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{SEnH}	Input high level voltage		2.1			V
I_{SEnH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{SEn(hyst)}$	Input hysteresis voltage		0.2			V
V_{SEnCL}	Input clamp voltage	I_{IN} = 1 mA	5.3		7.2	V
		I_{IN} = -1 mA		-0.7		

Table 8. Protections (7 V < V_{CC} < 18 V; -40°C < T_j < 150°C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{LIMH}	DC short circuit current	V_{CC} = 13 V	60	75	96	A
		4 V < V_{CC} < 18 V(1)			96	
I_{LIML}	Short circuit current during thermal cycling	V_{CC} = 13 V; T_R < T_j < T_{TSD}		25		
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature(1)		T_{RS} + 1	T_{RS} + 5		
T_{RS}	Thermal reset of fault diagnostic indication	V_{FR} = 0 V; V_{SEn} = 5 V	135			
T_{HYST}	Thermal hysteresis (T_{TSD} - T_R)(1)			5		

Table 8. Protections (7 V < V_{CC} < 18 V; -40°C < T_j < 150°C) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
ΔT_{J_SD}	Dynamic temperature			60		K
t_{LATCH_RST}	Fault reset time for output unlatch(1)	V_{FR} = 5 V to 0 V; V_{SEn} = 5 V; $V_{IN0,1}$ = 5 V; $V_{SEL0,1}$ = 0 V	3	10	20	µs
V_{DEMAG}	Turn-off output voltage clamp	I_{OUT} = 2 A; L = 6 mH; T_j = -40 °C	V_{CC} - 38			V
		I_{OUT} = 2 A; L = 6 mH; T_j = 25°C to 150°C	V_{CC} - 41	V_{CC} - 46	V_{CC} - 52	
V_{ON}	Output voltage drop limitation	I_{OUT} = 0.7 A		20		mV

1. Parameter guaranteed by design and characterization; not subject to production test.

Table 9. MultiSense (7 V < V_{CC} < 18 V; -40°C < T_j < 150°C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SENSE_CL}	MultiSense clamp voltage	V_{SEn} = 0 V; I_{SENSE} = 1 mA	-17		-12	V
		V_{SEn} = 0 V; I_{SENSE} = -1 mA		7		
Current Sense characteristics						
K_{OL}	I_{OUT}/I_{SENSE}	I_{OUT} = 10 mA; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	TBD			
dK_{cal}/K_{cal}(1)(2)	Current sense ratio drift at calibration point	I_{CAL} = 130 mA; I_{OUT} = 10 mA to 250 mA; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	TBD		TBD	%
K_{LED}	I_{OUT}/I_{SENSE}	I_{OUT} = 250 mA; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	TBD	TBD	TBD	
K_0	I_{OUT}/I_{SENSE}	I_{OUT} = 0.7 A; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	2680	5360	8040	
dK_0/K_0(1)(2)	Current sense ratio drift	I_{OUT} = 0.7 A; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	-25		25	%
K_1	I_{OUT}/I_{SENSE}	I_{OUT} = 1.4 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	3630	5190	6750	
dK_1/K_1(1)(2)	Current sense ratio drift	I_{OUT} = 1.4 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	-20		20	%
K_2	I_{OUT}/I_{SENSE}	I_{OUT} = 7 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	4150	5190	6230	
dK_2/K_2(1)(2)	Current sense ratio drift	I_{OUT} = 7 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	-10		10	%
K_3	I_{OUT}/I_{SENSE}	I_{OUT} = 21 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	4670	5190	5710	
dK_3/K_3(1)(2)	Current sense ratio drift	I_{OUT} = 21 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	-5		5	%

Table 9. MultiSense (7 V < V_{CC} < 18 V; -40°C < T_j < 150°C) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SENSE0}	MultiSense leakage current	MultiSense disabled: V_{SEn} = 0 V;	0		0.5	µA
		MultiSense disabled: -1 V < V_{SENSE} < 5 V(1)	-0.5		0.5	µA
		MultiSense enabled: V_{SEn} = 5 V; All channel ON; I_{OUTX} = 0 A; Ch_X diagnostic selected; – E.g. Ch_0: V_{IN0} = 5 V; V_{IN1} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; I_{OUT0} = 0 A; I_{OUT1} = 7 A	0		2	µA
		MultiSense enabled: V_{SEn} = 5 V; Ch_X channel OFF; Ch_X diagnostic selected; – E.g. Ch_0: V_{IN0} = 0 V; V_{IN1} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; I_{OUT1} = 7 A	0		2	µA
V_{OUT_MSD}(1)	Output Voltage for MultiSense shutdown	V_{SEn} = 5 V; R_{SENSE} = 2.7 kΩ – E.g. Ch_0: V_{IN0} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; I_{OUT0} = 7 A		5		V
V_{SENSE_SAT}	Multisense saturation voltage	V_{CC} = 7 V; R_{SENSE} = 2.7 K; V_{SEn} = 5 V; V_{IN0} = 5 V; $V_{SEL0,1}$ = 0 V; I_{OUT0} = 21 A; T_j = 150°C	5			V
I_{SENSE_SAT}(1)	CS saturation current	V_{CC} = 7 V; V_{SENSE} = 4 V; V_{SEn} = 5 V; V_{IN0} = 5 V; $V_{SEL0,1}$ = 0 V; T_j = 150°C	4			mA
I_{OUT_SAT}(1)	Output saturation current	V_{CC} = 7 V; V_{SENSE} = 4 V; V_{IN0} = 5 V; V_{SEn} = 5 V; $V_{SEL0,1}$ = 0 V; T_j = 150°C	26.7			A
Off-state diagnostic						
V_{OL}	Off-state open-load voltage detection threshold	V_{SEn} = 5 V; Ch_X OFF; Ch_X diagnostic selected – E.g: Ch_0 V_{IN0} = 0 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V;	2	3	4	V
$I_{L(off2)}$	OFF state output sink current	V_{IN} = 0 V; V_{OUT} = V_{OL}; T_j = -40°C to 125°C	-100		-15	µA

Table 9. MultiSense (7 V < V_{CC} < 18 V; -40°C < T_j < 150°C) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{DSTKON}	Off-state diagnostic delay time from falling edge of INPUT (see XXX)	V_{SEn} = 5 V; Ch_X ON to OFF transition Ch_X diagnostic selected – E.g: Ch_0 V_{IN0} = 5 V to 0 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; I_{OUT0} = 0 A; V_{OUT} = 4 V	100	350	700	µs
$t_{D\_OL\_V}$	Settling time for valid OFF-state open load diagnostic indication from rising edge of SEn	V_{IN0} = 0 V; V_{IN1} = 0 V; V_{FR} = 0 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; V_{OUT0} = 4 V; V_{SEn} = 0 V to 5 V			60	µs
t_{D_VOL}	Off-state diagnostic delay time from rising edge of V_{OUT}	V_{SEn} = 5 V; Ch_X OFF Ch_X diagnostic selected – E.g: Ch_0 V_{IN0} = 0 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; V_{OUT} = 0 V to 4 V		5	30	µs
Chip temperature analog feedback						
V_{SENSE_TC}	MultiSense output voltage proportional to chip temperature	V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 5 V; $V_{IN0,1}$ = 0 V; R_{SENSE} = 1 KΩ; T_j = -40°C	2.325	2.41	2.495	V
		V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 5 V; $V_{IN0,1}$ = 0 V; R_{SENSE} = 1 KΩ; T_j = 25°C	1.985	2.07	2.155	V
		V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 5 V; $V_{IN0,1}$ = 0 V; R_{SENSE} = 1 KΩ; T_j = 125°C	1.435	1.52	1.605	V
dV_{SENSE_TC}/dT(1)	Temperature coefficient	T_j = -40°C to 150°C		-5.5		mV/K
Transfer function		V_{SENSE_TC} (T) = V_{SENSE_TC} (T_0) + dV_{SENSE_TC} / dT * (T - T_0)				
V_{CC} supply voltage analog feedback						
V_{SENSE_VCC}	MultiSense output voltage proportional to V_{CC} supply voltage	V_{CC} = 13 V; V_{SEn} = 5 V; V_{SEL0} = 5 V; V_{SEL1} = 5 V; $V_{IN0,1}$ = 0 V; R_{SENSE} = 1 KΩ	3.16	3.23	3.3	V
Transfer function(3)		V_{SENSE_VCC} = V_{CC} / 4				
Fault diagnostic feedback (see *Table 10*)						
V_{SENSEH}	MultiSense output voltage in fault condition	V_{CC} = 13 V; R_{SENSE} = 1 kΩ – E.g: Ch_0 in open load V_{IN0} = 0 V; V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; I_{OUT0} = 0 A; V_{OUT} = 4 V	5		6.6	V

Table 9. MultiSense (7 V < V_{CC} < 18 V; -40°C < T_j < 150°C) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SENSEH}	MultiSense output current in fault condition	V_{CC} = 13 V; V_{SENSE} = 5 V	7	20	30	mA
MultiSense timings (current sense mode - see *Figure 5*)(4)						
$t_{DSENSE1H}$	Current sense settling time from rising edge of SEn	V_{IN} = 5 V; V_{SEn} = 0 V to 5 V; R_{SENSE} = 1 kΩ; R_L = 1.84 Ω			60	µs
$t_{DSENSE1L}$	Current sense disable delay time from falling edge of SEn	V_{IN} = 5 V; V_{SEn} = 5 V to 0 V; R_{SENSE} = 1 kΩ; R_L = 1.84 Ω		5	20	µs
$t_{DSENSE2H}$	Current sense settling time from rising edge of INPUT	V_{IN} = 0 V to 5 V; V_{SEn} = 5 V; R_{SENSE} = 1 kΩ; R_L = 1.84 Ω		100	250	µs
$\Delta t_{DSENSE2H}$	Current sense settling time from rising edge of I_{OUT} (dynamic response to a step change of I_{OUT})	V_{IN} = 5 V; V_{SEn} = 5 V; R_{SENSE} = 1 kΩ; R_L = 1.84 Ω			100	µs
$t_{DSENSE2L}$	Current sense turn-off delay time from falling edge of INPUT	V_{IN} = 5 V to 0 V; V_{SEn} = 5 V; R_{SENSE} = 1 kΩ; R_L = 1.84 Ω		50	250	µs
MultiSense timings (chip temperature sense mode - see *Figure 6*)(4)						
$t_{DSENSE3H}$	V_{SENSE_TC} settling time from rising edge of SEn	V_{SEn} = 0 V to 5 V; V_{SEL0} = 0 V; V_{SEL1} = 5 V; R_{SENSE} = 1 kΩ			60	µs
$t_{DSENSE3L}$	V_{SENSE_TC} disable delay time from falling edge of SEn	V_{SEn} = 5 V to 0 V; V_{SEL0} = 0 V; V_{SEL1} = 5 V; R_{SENSE} = 1 kΩ			20	µs
MultiSense timings (V_{CC} voltage sense mode - see *Figure 6*)(4)						
$t_{DSENSE4H}$	V_{SENSE_VCC} settling time from rising edge of SEn	V_{SEn} = 0 V to 5 V; V_{SEL0} = 5 V; V_{SEL1} = 5 V; R_{SENSE} = 1 kΩ			60	µs
$t_{DSENSE4L}$	V_{SENSE_VCC} disable delay time from falling edge of SEn	V_{SEn} = 5 V to 0 V; V_{SEL0} = 5 V; V_{SEL1} = 5 V; R_{SENSE} = 1 kΩ			20	µs
MultiSense timings (Multiplexer transition times)(4)						
t_{D_XtoY}	MultiSense transition delay from Ch_X to Ch_Y	V_{IN0} = 5 V; V_{IN1} = 5 V; V_{SEn} = 5 V; V_{SEL1} = 0 V; V_{SEL0} = 0 V to 5 V; I_{OUT0} = 0A; I_{OUT1} = 3 A; R_{SENSE} = 1 kΩ			20	µs

Table 9. MultiSense (7 V < V_{CC} < 18 V; -40°C < T_j < 150°C) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{D_CStoTC}	MultiSense transition delay from current sense to T_C sense	V_{IN0} = 5 V; V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V to 5 V; I_{OUT0} = 3.5 A; R_{SENSE} = 1 kΩ			60	µs
t_{D_TCtoCS}	MultiSense transition delay from T_C sense to current sense	V_{IN0} = 5 V; V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 5 V to 0 V; I_{OUT0} = 3.5 A; R_{SENSE} = 1 kΩ			20	µs
$t_{D\_CStoVCC}$	MultiSense transition delay from current sense to V_{CC} sense	V_{IN1} = 5 V; V_{SEn} = 5 V; V_{SEL0} = 5 V; V_{SEL1} = 0 V to 5 V; I_{OUT1} = 3.5A; R_{SENSE} = 1 kΩ			60	µs
$t_{D\_VCCtoCS}$	MultiSense transition delay from V_{CC} sense to current sense	V_{IN1} = 5 V; V_{SEn} = 5 V; V_{SEL0} = 5 V; V_{SEL1} = 5 V to 0 V; I_{OUT1} = 3.5 A; R_{SENSE} = 1 kΩ			20	µs
$t_{D\_TCtoVCC}$	MultiSense transition delay from T_C sense to V_{CC} sense	V_{CC} = 13 V; T_j = 125°C; V_{SEn} = 5 V; V_{SEL0} = 0 V to 5 V; V_{SEL1} = 5 V; R_{SENSE} = 1 kΩ			20	µs
$t_{D\_VCCtoTC}$	MultiSense transition delay from V_{CC} sense to T_C sense	V_{CC} = 13 V; T_j = 125°C; V_{SEn} = 5 V; V_{SEL0} = 5 V to 0 V; V_{SEL1} = 5 V; R_{SENSE} = 1 kΩ			20	µs
$t_{D\_CStoVSENSEH}$	MultiSense transition delay from stable current sense on Ch_X to V_{SENSEH} on Ch_Y	V_{IN0} = 5 V; V_{IN1} = 0 V; V_{SEn} = 5 V; V_{SEL1} = 0 V; V_{SEL0} = 0 V to 5 V; I_{OUT0} = 7 A; V_{OUT1} = 4 V; R_{SENSE} = 1 kΩ			20	µs

1. Parameter specified by design; not subject to production test.
2. All values refer to V_{CC} = 13 V; T_j = 25 °C, unless otherwise specified.
3. V_{CC} sensing and T_C sensing are referred to GND potential.
4. Transition delay are measured up to +/- 10% of final conditions.

Figure 4. Switching times and Pulse skew

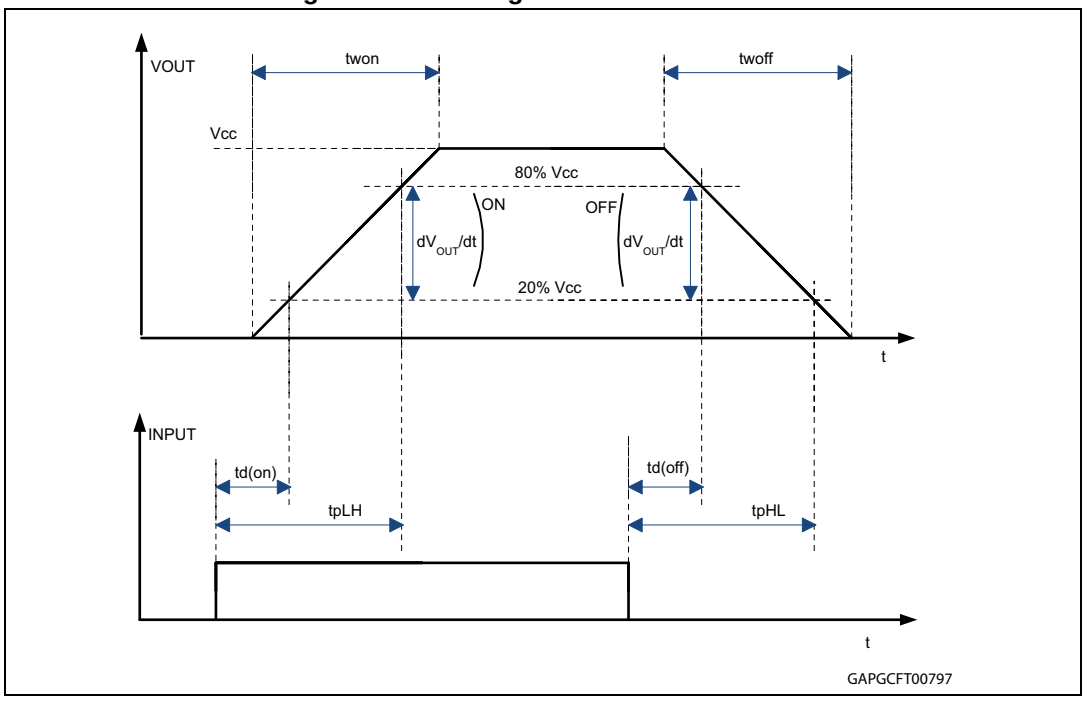


Figure 5. MultiSense timings (current sense mode)

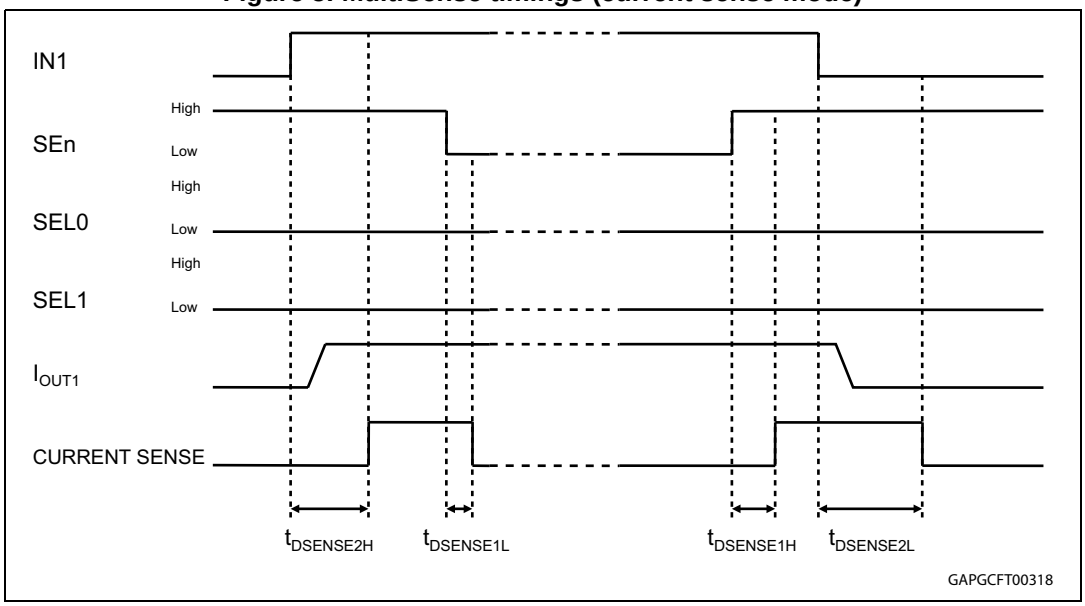


Figure 6. MultiSense timings (chip temperature and V_{CC} sense mode)

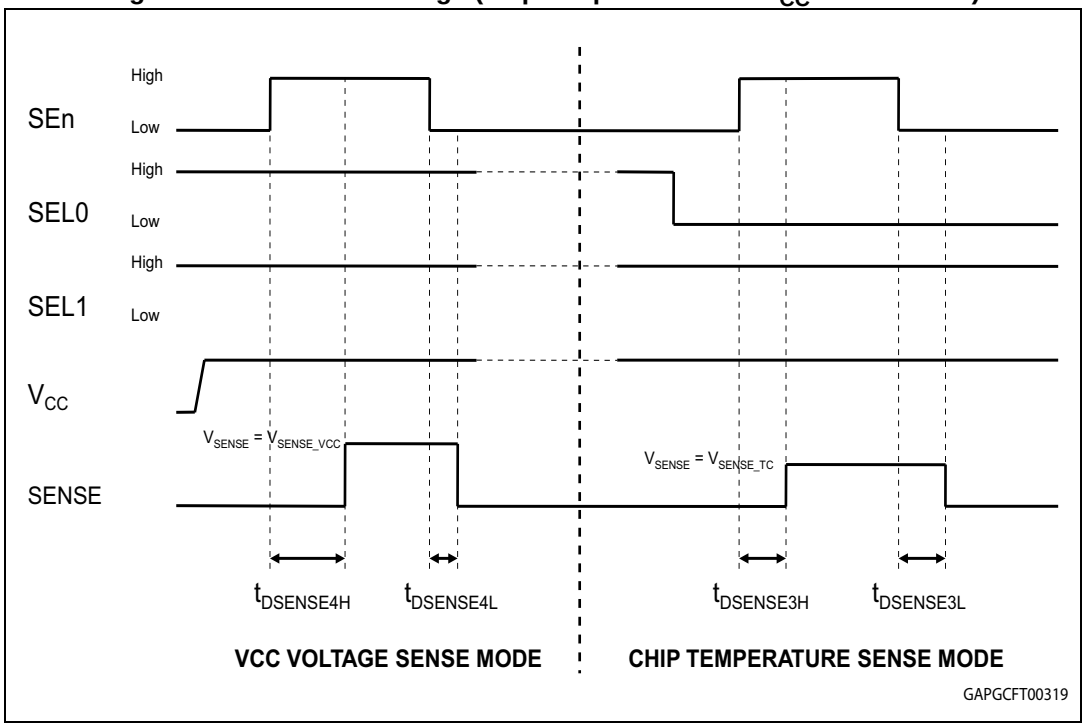


Figure 7. T_{DSKON}

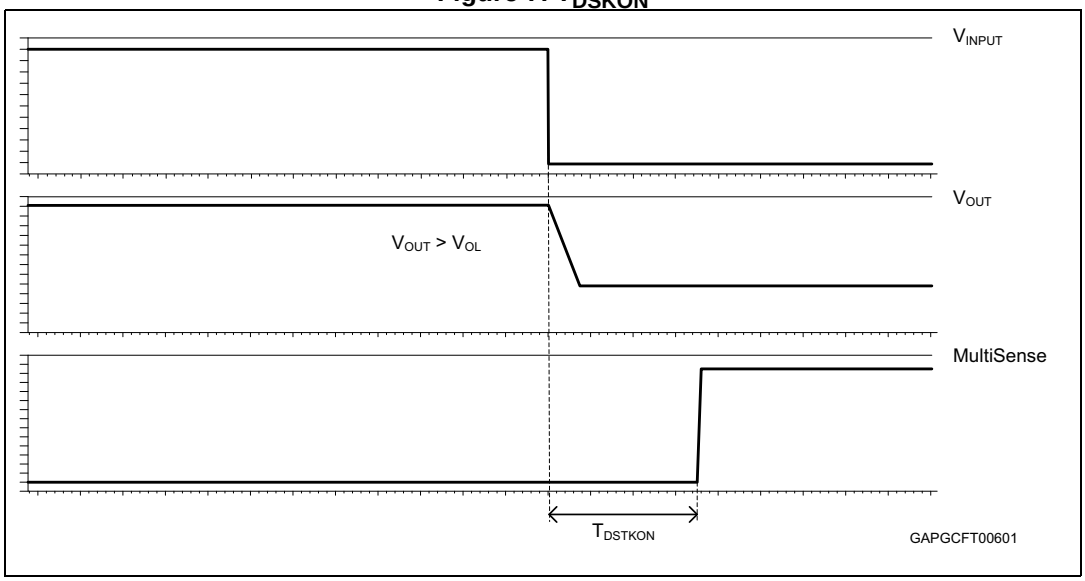


Table 10. Truth table

Mode	Conditions	IN_X	FR	SEn	SEL_X	OUT_X	MultiSense	Comments
Standby	All logic inputs low	L	L	L	L	L	Hi-Z	Low quiescent current consumption
Normal	Nominal load connected; T_j < 150°C	L	X	Refer to *Table 11*		L	Refer to *Table 11*	
		H	L			H		Outputs configured for auto-restart
		H	H			H		Outputs configured for latch off
Overload	Overload or short to GND causing: $T_j > T_{TSD}$ or $\Delta T_j > \Delta T_{j\_SD}$	L	X	Refer to *Table 11*		L	Refer to *Table 11*	
		H	L			H		Output cycles with temperature hysteresis
		H	H			L		Output latches off
Under-voltage	$V_{CC} < V_{USD}$ (falling)	X	X	X	X	L L	Hi-Z Hi-Z	Re-start when $V_{CC} > V_{USD} + V_{USDhyst}$ (rising)
Off-state diagnostics	Short to V_{CC}	L	X	Refer to *Table 11*		H	Refer to *Table 11*	
	Open-load	L	X			H		External pull up
Negative output voltage	Inductive loads turn-off	L	X	Refer to *Table 11*		< 0 V	Refer to *Table 11*	

Table 11. MultiSense multiplexer addressing

SEn	SEL_1	SEL_0	MUXchannel	MultiSense output			
				Normal mode	Overload	Off-state diag.(1)	Negative output
L	X	X		Hi-Z			
H	L	L	Channel 0 diagnostic	I_{SENSE} = 1/K * I_{OUT0}	V_{SENSE} = V_{SENSEH}	V_{SENSE} = V_{SENSEH}	Hi-Z
H	L	H	Channel 1 diagnostic	I_{SENSE} = 1/K * I_{OUT1}	V_{SENSE} = V_{SENSEH}	V_{SENSE} = V_{SENSEH}	Hi-Z
H	H	L	T_{CHIP} Sense	$V_{SENSE} = V_{SENSE\_TC}$			
H	H	H	V_{CC} Sense	$V_{SENSE} = V_{SENSE\_VCC}$			

1. In case the output channel corresponding to the selected MUX channel is latched off while the relevant input is low, Multisense pin delivers feedback according to OFF-State diagnostic.
Example 1: FR = 1; IN_0 = 0; OUT_0 = L (latched); MUX channel = channel 0 diagnostic; Mutisense = 0
Example 2: FR = 1; IN_0 = 0; OUT_0 = latched, $V_{OUT0} > V_{OL}$; MUX channel = channel 0 diagnostic; Mutisense = V_{SENSEH}

Table 12. Electrical transient requirements (part 1)

ISO 7637-2: 2004(E) test pulse	Test levels (1)		Number of pulses or test times	Burst cycle / pulse repetition time		Delays and impedance
	III	IV		Min.	Max.	
1	-75V	-100V	5000 pulses	0.5s	5s	2 ms, 10Ω
2a	+37V	+50V	5000 pulses	0.2s	5s	50µs, 2Ω
3a	-100V	-150V	1h	90ms	100ms	0.1µs, 50Ω
3b	+75V	+100V	1h	90ms	100ms	0.1µs, 50Ω
4	-6V	-7V	1 pulse			100ms, 0.01Ω
5b(2)	+65V	+87V	1 pulse			400ms, 2Ω

1. The above test levels must be considered referred to V_{CC} = 13.5 V except for pulse 5b.
2. Valid in case of external load dump clamp: 40V maximum referred to ground.

Table 13. Electrical transient requirements (part 2)

ISO 7637-2: 2004E test pulse	Test level results	
	III	VI
1	C	C
2a	C	C
3a	C	C
3b	C	C
4	C	C
5b(1)	C	C

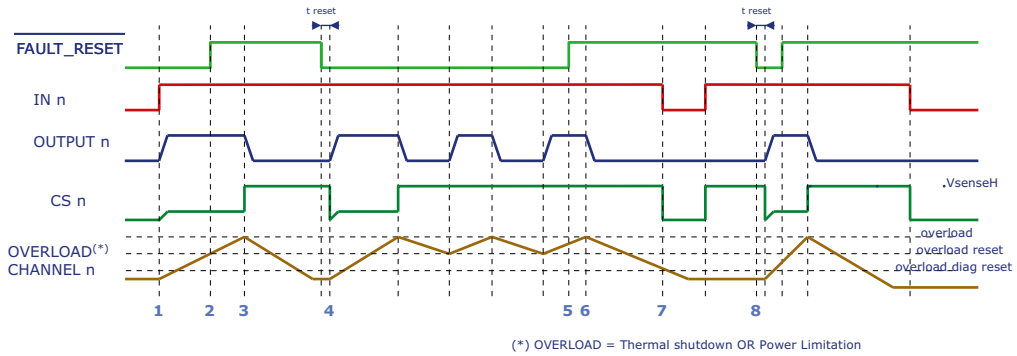
1. Valid in case of external load dump clamp: 40V maximum referred to ground.

Table 14. Electrical transient requirements (part 3)

Class	Contents
C	All functions of the device performed as designed after exposure to disturbance.
E	One or more functions of the device did not perform as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

2.4 Waveforms

Figure 8. Fault reset description



(*) OVERLOAD = Thermal shutdown OR Power Limitation

1: OUTPUTn and CSn controlled by INn.
2: FAULT_RESET from '0' to '1' → no action on CSn pin
3: Overload latch-off. INn high → CSn high
4: FAULT_RESET low AND Temp channeln < overload_reset → Overload latch reset after t_reset
4 to 5: FAULT_RESET low AND INn high → thermal cycling, CSn high
5: FAULT_RESET high → latch-off reset disabled
6 to 7: Overload event and FAULT_RESET high → latch-off, no thermal cycling
7 to 8: Overload diagnostic disabled/enabled by the input
8: Overload latch-off reset by FAULT_RESET

GAPGCFT00320

3 Package information

3.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at *www.st.com*.

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3.2 PowerSSO-36 mechanical data

Figure 9. PowerSSO-36 package dimensions

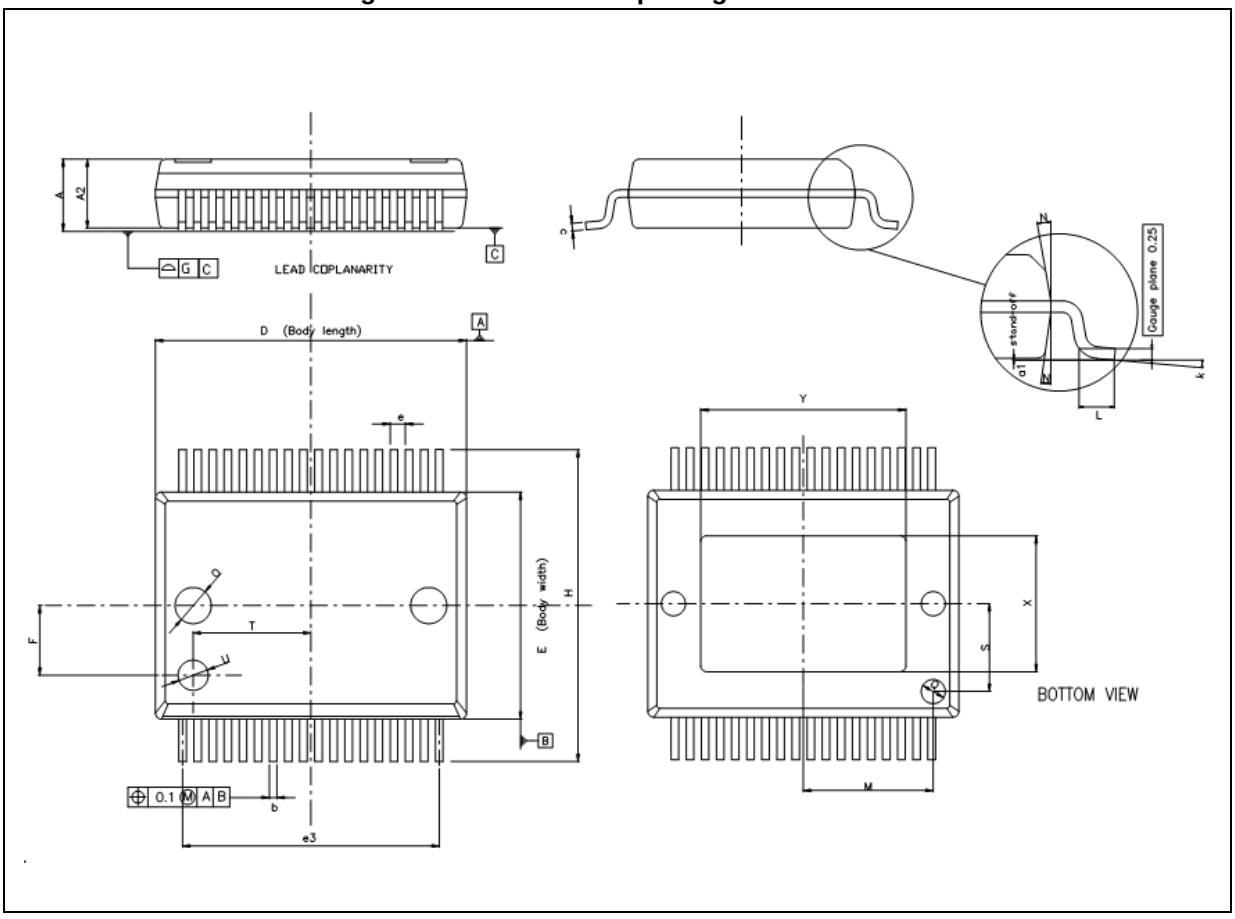


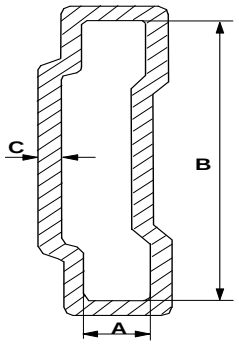
Table 15. PowerSSO-36 mechanical data

Symbol	millimeters		
	Min	Typ	Max
A	2.15	-	2.45
A2	2.15	-	2.35
a1	0	-	0.1
b	0.18	-	0.36
c	0.23	-	0.32
D	10.10	-	10.50
E	7.4	-	7.6
e	-	0.5	-
e3	-	8.5	-
F	-	2.3	-
G	-	-	0.1
H	10.1	-	10.5
h	-	-	0.4
k	0°	-	8°
L	0.55	-	0.85
M	-	4.3	-
N	-	-	10°
O	-	1.2	
Q	-	0.8	-
S	-	2.9	-
T	-	3.65	-
U	-	1.0	-
X(1)	4.3	-	5.2
Y(1)	6.9	-	7.5

1. Corresponding to internal variation C.

3.3 Packing information

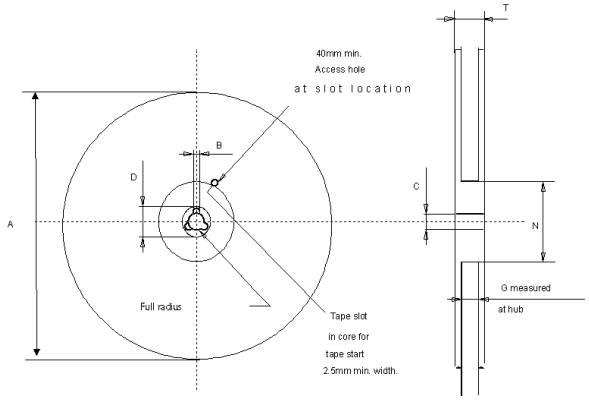
Figure 10. PowerSSO-36 tube shipment (no suffix)



Base q.ty	49
Bulk q.ty	1225
Tube length (± 0.5)	532
A	3.5
B	13.8
C (± 0.1)	0.6

All dimensions are in mm.

Figure 11. PowerSSO-36 tape and reel shipment (suffix "TR")



REEL DIMENSIONS

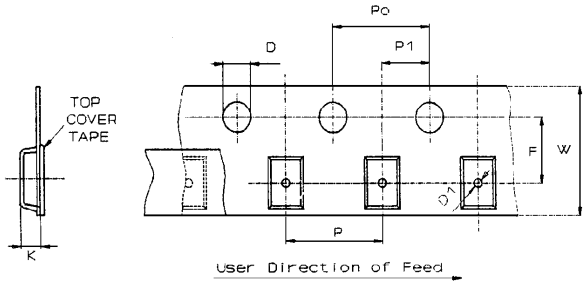
Base q.ty	1000
Bulk q.ty	1000
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	24.4
N (min)	100
T (max)	30.4

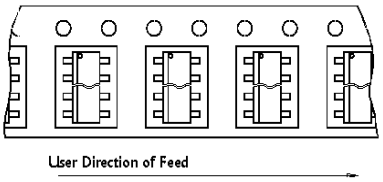
TAPE DIMENSIONS

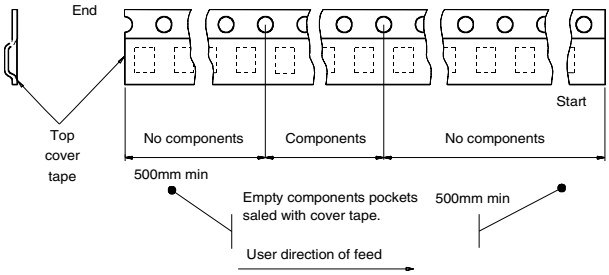
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

Tape width	**W**	24
Tape hole spacing	**P0 (± 0.1)**	4
Component spacing	**P**	12
Hole diameter	**D (± 0.05)**	1.55
Hole diameter	**D1 (min)**	1.5
Hole position	**F (± 0.1)**	11.5
Compartment depth	**K (max)**	2.85
Hole spacing	**P1 (± 0.1)**	2

All dimensions are in mm.







4 Order codes

Table 16. Device summary

Package	Order codes	
	Tube	Tape and reel
PowerSSO-36	VND7012AY-E	VND7012AYTR-E

5 Revision history

Table 17. Document revision history

Date	Revision	Changes
05-Mar-2012	1	Initial release.
18-Feb-2013	2	*Table 1: Pin functions*: – GND: updated functions definitions Updated *Figure 2: Configuration diagram (top view)*
25-Mar-2013	3	Updated *Features* list *Table 3: Absolute maximum ratings*: – $-I_{OUT}$, V_{ESD}: updated value – I_{SENSE}, E_{MAX}: updated parameter and value Updated *Table 4: Thermal data* *Table 5: Power section*: – V_{clamp}: added test conditions and value – I_{STBY}, t_{D_STBY}, $I_{L(off)}$: updated test conditions – $I_{GND(ON)}$: updated test conditions and value – V_F: added row Updated *Table 6: Switching (V_{CC} = 13 V; -40 °C < T_j < 150 °C, unless otherwise specified)* *Table 8: Protections (7 V < V_{CC} < 18 V; -40°C < T_j < 150°C)*: – I_{LIMH}: added note – T_R, T_{HYST}: added note and updated value – ΔT_{J_SD}: updated test conditions – t_{LATCH_RST}: added note and updated test conditions *Table 9: MultiSense (7 V < V_{CC} < 18 V; -40°C < T_j < 150°C)*: – V_{SENSE_CL}, $t_{DSENSE1H}$, $t_{DSENSE1L}$, $t_{DSENSE2H}$, $\Delta t_{DSENSE2L}$, $t_{DSENSE2L}$, t_{D_CStoTC}, t_{D_TCtoCS}, $t_{D\_CStoVCC}$, $t_{D\_VCCtoCS}$, $t_{D\_CStoVSENSEH}$: updated test conditions – K_{OL}, dK_{cal}/K_{cal}, K_{LED}, I_{OUT_SAT}: added rows – K_0, dK_0/K_0, K_1, dK_1/K_1, K_2, dK_2/K_2, K_3, dK_3/K_3, $t_{D\_OL\_V}$, V_{SENSEH}, I_{SENSEH}: updated values – I_{SENSE0}: added test conditions and values – V_{SENSE_SAT}, I_{SENSE_SAT}, $I_{L(off2)}$, V_{SENSE_TC}, V_{SENSE_CC}: updated test conditions and values Removed *Figure: Switching times* and *Figure: Pulse skew* Added *Figure 4: Switching times and Pulse skew* and *Figure 7: T_{DSKON}* *Table 10: Truth table*: – Updated overload condition *Table 11: MultiSense multiplexer addressing*: – Added note and updated negative output

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