# VNH7100AS

## Automotive fully integrated H-bridge motor driver

**Datasheet - production data**


**SO-16N**

## Features

| Type | $R_{DS(on)}$ | $I_{out}$ | $V_{CCmax}$ |
|---|---|---|---|
| VNH7100AS | 100 mΩ typ (per leg) | 12 A | 41 V |

- Automotive qualified
- Output current: 15 A
- 3 V CMOS-compatible inputs
- Undervoltage shutdown
- Overvoltage clamp
- Thermal shutdown
- Cross-conduction protection
- Current and power limitation
- Very low standby power consumption
- Protection against loss of ground and loss of $V_{CC}$
- PWM operation up to 20 kHz
- MultiSense diagnostic functions
  - Analog motor current feedback
  - Output short to ground detection
  - Thermal shutdown indication
  - OFF-state open-load detection
  - Output short to $V_{CC}$ detection
- Output protected against short to ground and short to $V_{CC}$
- Standby Mode
- Half Bridge Operation
- Package: ECOPACK®

## Description

The device is a full bridge motor driver intended for a wide range of automotive applications. The device incorporates a dual monolithic high-side driver and two low-side switches.

Both switches are designed using STMicroelectronics' well known and proven proprietary VIPower® M0 technology that allows to efficiently integrate on the same die a true Power MOSFET with an intelligent signal/protection circuitry. The three dies are assembled in SO-16N package on electrically isolated leadframes.

Moreover, its fully symmetrical mechanical design allows superior manufacturability at board level. The input signals $IN_A$ and $IN_B$ can directly interface the microcontroller to select the motor direction and the brake condition. A SEL0 pin is available to address the information available on the MultiSense to the microcontroller. The MultiSense pin allows to monitor the motor current by delivering a current proportional to the motor current value.

The PWM, up to 20 kHz, allows to control the speed of the motor in all possible conditions. In all cases, a low level state on the PWM pin turns off both the $LS_A$ and $LS_B$ switches.

**Table 1. Device summary**

| Package | Order codes | |
|---|---|---|
| | Tube | Tape and reel |
| SO-16N | — | VNH7100ASTR |

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# 1 Block diagram and pin description

**Figure 1. Block diagram**

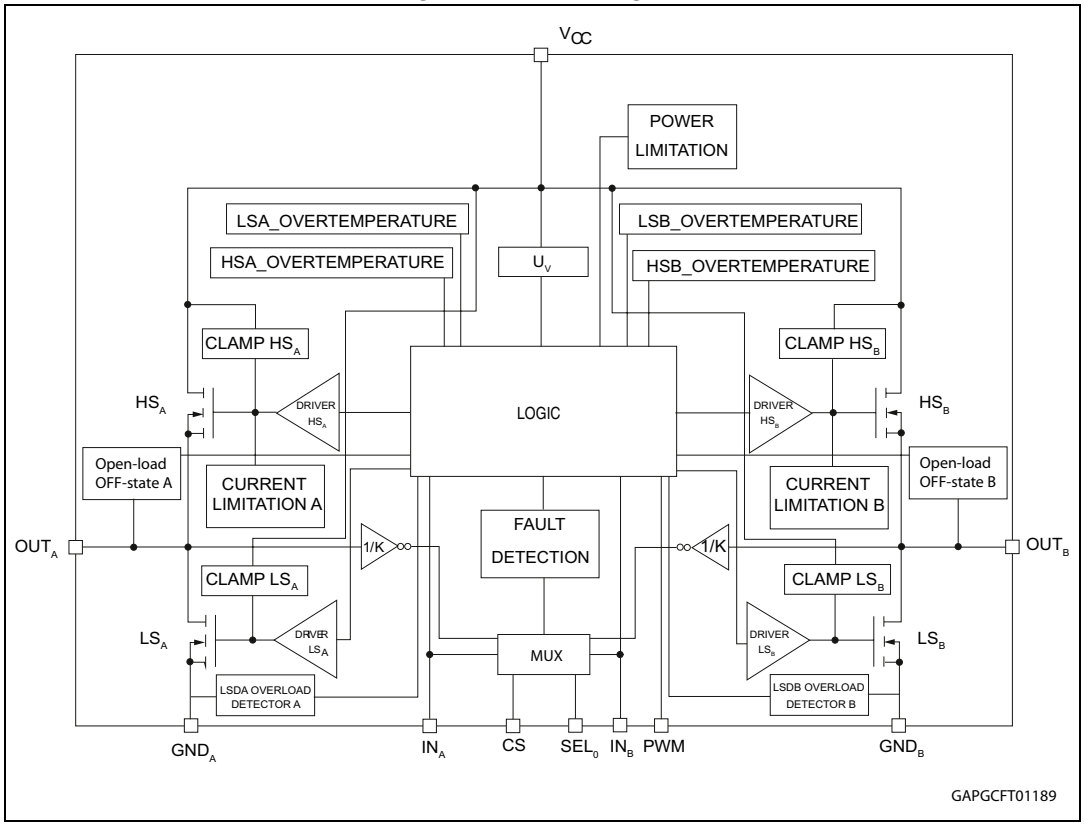



**Table 2. Block description**

| Name | Description |
|---|---|
| Logic control | Allows the turn-on and the turn-off of the high-side and the low-side switches according to the truth table. |
| Undervoltage | Shuts down the device for battery voltage lower than 4 V. |
| High-side and low-side clamp voltage | Protect the high-side and the low-side switches from the high voltage on the battery line. |
| High-side and low-side driver | Drive the gate of the concerned switch to allow a proper $R_{on}$ for the leg of the bridge. |
| Current limitation | Limits the motor current in case of short circuit. |
| High-side and low-side overtemperature protection | In case of short-circuit with the increase of the junction temperature, it shuts down the concerned driver to prevent degradation and to protect the die. |
| Low-side overload detector | Detects when low side current exceeds shutdown current and latches off the concerned Low side. |

**Table 2. Block description (continued)**

| Name | Description |
|---|---|
| Fault detection | Signalizes the abnormal behavior of the switch through MultiSense pin. |
| Power limitation | Limits the power dissipation of the high-side driver inside safe range in case of short to ground condition. |

**Figure 2. Configuration diagram (top view)**

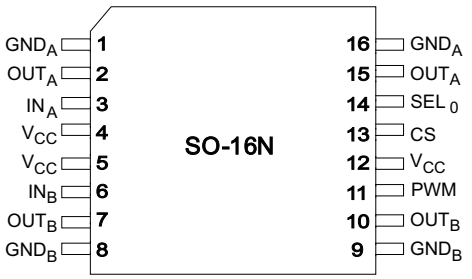
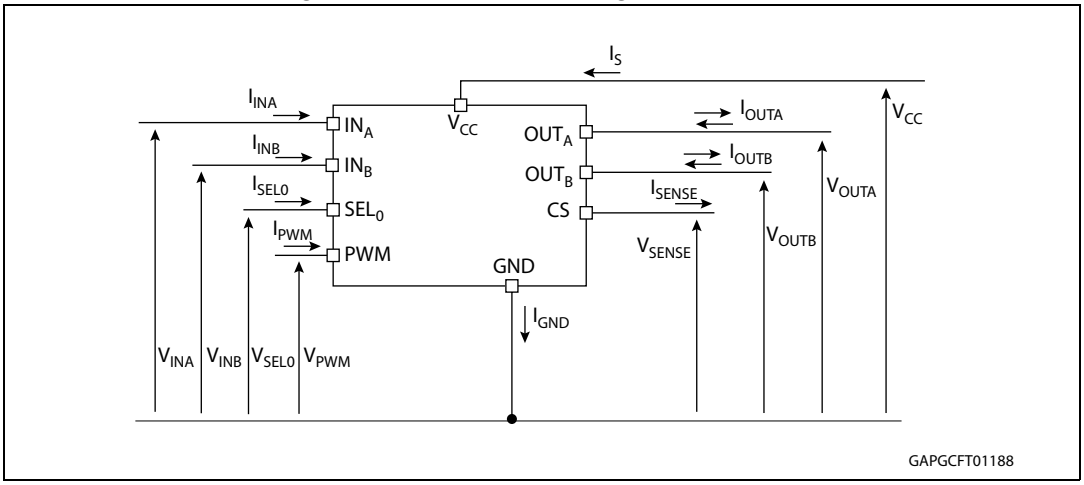



**Table 3. Pin definitions and functions**

| Pin N° | Symbol | Function |
|---|---|---|
| 1, 16 | $GND_A$ | Source of low-side switch A |
| 2, 15 | $OUT_A$ | Source of high-side switch A / drain of low-side switch A |
| 3 | $IN_A$ | Clockwise input |
| 4, 5, 12 | $V_{CC}$ | Power supply voltage |
| 6 | $IN_B$ | Counter clockwise input |
| 7, 10 | $OUT_B$ | Source of high-side switch B / drain of low-side switch B |
| 8, 9 | $GND_B$ | Source of low-side switch B |
| 11 | PWM | Voltage controlled input pin with hysteresis, CMOS compatible. Gates of low-side FETS get modulated by the PWM signal during their on phase allowing speed control of the motor. Active high. |
| 13 | CS | Multiplexed analog sense output pin; it delivers a current proportional to the motor current. |
| 14 | $SEL_0$ | Active high compatible with 3 V and 5 V CMOS outputs pin; in combination with $IN_A$, $IN_B$, it addresses the CurrentSense information delivered to the micro according to the operative truth table. |

# 2 Electrical specifications

**Figure 3. Current and voltage conventions**




## 2.1 Absolute maximum ratings

Stressing the device above the rating listed in *Table 4: Absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

**Table 4. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | Supply voltage | 38 | V |
| $-V_{CC}$ | Reverse DC Supply Voltage | 0.3 | V |
| $I_{max}$ | Maximum output current (continuous) | Internally limited | A |
| $I_R$ | Reverse output current (continuous) | -15 | A |
| $V_{CCPK}$ | Maximum transient supply voltage (ISO 16750-2:2010 Test B clamped to 40 V; $R_L$ = 4 Ω) | 40 | V |
| $V_{CCJS}$ | Maximum jump start voltage for single pulse short circuit protection | 28 | V |
| $I_{IN}$ | Input current ($IN_A$ and $IN_B$ pins) | -1 to 10 | mA |
| $I_{SEL0}$ | $SEL_0$ DC input current | -1 to 10 | mA |
| $I_{PWM}$ | PWM input current | -1 to 10 | mA |
| $I_{SENSE}$ | CS pin DC output current ($V_{GND}$ = $V_{CC}$ and $V_{SENSE}$ < 0 V) | 10 | mA |
| | CS pin DC output current in reverse ($V_{CC}$ < 0 V) | -20 | |

**Table 4. Absolute maximum ratings (continued)**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{ESD}$ | Electrostatic discharge<br>(Human body model: R = 1.5 kΩ; C = 100 pF)<br>– $IN_A$,$IN_B$, PWM<br>– $SEL_0$<br>– CS<br>– $V_{CC}$<br>– Output | <br><br>2<br>2<br>2<br>4<br>4 | kV |
| $V_{ESD}$ | Charge device model (CDM-AEC-Q100-011) | 750 | V |
| $T_c$ | Junction operating temperature | -40 to 150 | °C |
| $T_{STG}$ | Storage temperature | -55 to 150 | °C |

## 2.2 Thermal data

**Table 5. Thermal data**

| Symbol | Parameter | | Max. value | Unit |
|---|---|---|---|---|
| $R_{thj\text{-}pin}$ | Thermal resistance junction-pin | HSD | 32 | °C/W |
| | | LSD | 45 | °C/W |
| $R_{thj\text{-}amb}$ | Thermal resistance junction-ambient (JEDEC JESD 51-2)(1) | | See *Figure 24* | °C/W |
| $R_{thj\text{-}amb}$ | Thermal resistance junction-ambient (JEDEC JESD 51-2)(2) | HSD | 40.7 | °C/W |
| | | LSD | 55.4 | °C/W |

1. Device mounted on two-layers 2s0p PCB.
2. Device mounted on four-layers 2s2p PCB.

## 2.3 Electrical characteristics

Values specified in this section are for $V_{CC}$ = 7 V up to 28 V; -40°C < $T_j$ < 150°C, unless otherwise specified.

**Table 6. Power section**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Operating supply voltage | | 4 | | 28 | V |
| $I_S$ | Supply current | Off-state (standby)<br>$IN_A$ = $IN_B$ = 0; $SEL_0$ = 0;<br>PWM = 0; $T_j$ = 25 °C; $V_{CC}$ = 13 V; | | | 1 | µA |
| | | Off-state (standby)<br>$IN_A$ = $IN_B$ = 0; $SEL_0$ = 0;<br>PWM = 0; $V_{CC}$ = 13 V; $T_j$ = 85°C | | | 1 | µA |
| | | Off-state (standby)<br>$IN_A$ = $IN_B$ = 0; $SEL_0$ = 0;<br>PWM = 0; $V_{CC}$ = 13 V; $T_j$ = 125 °C | | | 3 | µA |
| | | Off-state (no standby)<br>$IN_A$ = $IN_B$ = 0; $SEL_0$ = 5 V;<br>PWM= 0 | | 2 | 4 | mA |
| | | On-state: $IN_A$ or $IN_B$ = 5 V;<br>PWM = 0 or PWM = 5; $SEL_0$ = X | | 3.5 | 6 | mA |
| $t_{D\_STBY}$(1) | Standby mode blanking time | $V_{CC}$ = 13 V;<br>$IN_A$ = $IN_B$ = PMW = 0 V;<br>$V_{SEL0}$ from 5 V to 0 V | 0.2 | 1 | 1.8 | ms |
| $R_{ONHS}$ | Static high-side resistance | $I_{OUT}$ = 2.5 A; $T_j$ = 25°C | | 60 | | mΩ |
| | | $I_{OUT}$ = 2.5 A; $T_j$ = -40 to 150°C | | | 120 | mΩ |
| $R_{ONLS}$ | Static low-side resistance | $I_{OUT}$ = 2.5 A; $T_j$ = 25°C | | 40 | | mΩ |
| | | $I_{OUT}$ = 2.5 A; $T_j$ = -40°C to 150°C | | | 80 | mΩ |
| $V_f$ | Free-wheeling diode forward voltage | $I_{OUT}$ = -2.5 A; $T_j$ = 150°C | | 0.7 | 0.9 | V |
| $I_{L(off)}$ | Off-state output current of one leg | $IN_A$ = $IN_B$ = 0; PWM = 0;<br>$V_{CC}$ = 13 V; $T_j$ = 25 °C | 0 | | 0.5 | µA |
| | | $IN_A$ = $IN_B$ = 0; PWM = 0;<br>$V_{CC}$ = 13 V; $T_j$ = 125 °C | 0 | | 3 | µA |
| $I_{L(off\_h)}$ | Off-state output current of one leg with other HSD on | $IN_A$ = 0; $IN_B$ = 5 V; PWM = 0;<br>$V_{CC}$ = 13 V | 20 | | 60 | µA |

1. To power on the device from the standby, it is recommended to:
   — toggle INA or INB from 0 to 1 first to come out from STBY mode
   — toggle PWM from 0 to 1 with a delay of 20 µs
   this avoids any over-stress on the device in case of existing short-to-battery.

**Table 7. Logic inputs ($IN_A$, $IN_B$, PWM) ($V_{CC}$ = 7 V up to 28 V; -40°C < $T_j$ < 150°C)**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input low level voltage | | | | 0.9 | V |
| $V_{IH}$ | Input high level voltage | | 2.1 | | | V |
| $V_{IHYST}$ | Input hysteresis voltage | | 0.2 | | | V |
| $V_{ICL}$ | Input clamp voltage | $I_{IN}$ = 1 mA | 5.3 | | 7.2 | V |
| | | $I_{IN}$ = -1 mA | | -0.7 | | V |
| $I_{INL}$ | Input current | $V_{IN}$ = 0.9 V | 1 | | | µA |
| $I_{INH}$ | Input current | $V_{IN}$ = 2.1 V | | | 10 | µA |
| **$SEL_0$ ($V_{CC}$ = 7 V up to 18 V; -40°C < $T_j$ < 150°C)** | | | | | | |
| $V_{SELL}$ | Input low level voltage | | | | 0.9 | V |
| $I_{SELL}$ | Low level input current | $V_{SEL}$ = 0.9 V | 1 | | | µA |
| $V_{SELH}$ | Input high level voltage | | 2.1 | | | V |
| $I_{SELH}$ | High level input current | $V_{SEL}$ = 2.1 V | | | 10 | µA |
| $V_{SEL(hyst)}$ | Input hysteresis voltage | | 0.2 | | | V |
| $V_{SELCL}$ | Input clamp voltage | $I_{SEL}$ = 1 mA | 5.3 | | 7.5 | V |
| | | $I_{SEL}$ = -1 mA | | -0.8 | | V |
| **PWM ($V_{CC}$= 7 V up to 28 V; -40°C < $T_j$ < 150°C)** | | | | | | |
| $V_{PWM}$ | Input low level voltage | | | | 0.9 | V |
| $I_{PWM}$ | Low level input current | $V_{PWM}$ = 0.9 V | 1 | | | µA |
| $V_{PWM}$ | Input high level voltage | | 2.1 | | | V |
| $I_{PWMH}$ | High level input current | $V_{PWM}$ = 2.1 V | | | 10 | µA |
| $V_{PWM(hyst)}$ | Input hysteresis voltage | | 0.2 | | | V |
| $V_{PMWCL}$ | Input clamp voltage | $I_{PWM}$ = 1 mA | 5.3 | | 7.2 | V |
| | | $I_{PWM}$ = -1 mA | | -0.7 | | V |

**Table 8. Switching ($V_{CC}$ = 13 V; $R_{LOAD}$ = 5.2 Ω)**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $f^{(1)}$ | PWM frequency | | 0 | | 20 | kHz |
| $t_{d(on)}$ | Turn-on delay time | Input rise time < 1µs (see *Figure 6*) | | 20 | | µs |
| $t_{d(off)}$ | Turn-off delay time | Input rise time < 1µs (see *Figure 6*) | | 13 | | µs |
| $t_r$ | Rise time | See *Figure 5* | | 1 | 2 | µs |
| $t_f$ | Fall time | See *Figure 5* | | 1 | 2 | µs |
| $t_{cross}$ | Low-side turn-on delay time | Input rise time < 1 µs (see *Figure 7*) | 40 | 150 | 350 | µs |

1. Parameter guaranteed by design and characterization; not subjected to production test.

**Table 9. Protections and diagnostics ($V_{CC}$ = 7 V up to 18 V; -40°C < $T_j$ < 150°C)**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{USD}$ | Undervoltage shutdown | | | | 4 | V |
| $V_{USDreset}$ | Undervoltage shutdown reset | | | | 5 | V |
| $V_{USDHyst}$ | Undervolatge shutdown Hysteresis | | | 0.4 | | V |
| $I_{LIM\_H}$ | High-side current limitation | | 12 | 18 | 24 | A |
| $I_{SD\_LS}$ | Shutdown LS current | | 14 | 22 | 30 | A |
| $t_{SD\_LS}$ | Time to shutdown for the low-side | $V_{INA}$ = $V_{INB}$ = 0 V; PWM = 5 V (see *Figure 8*) | | 5 | | µs |
| $V_{CL\_HSD}$ | High-side clamp voltage ($V_{CC}$ to $OUT_A$ = 0 or $OUT_B$ = 0) | $I_{OUT}$ = 100 mA; $t_{CLAMP}$ = 1 ms | 38 | 46 | | V |
| $V_{CL\_LSD}$ | Low-side clamp voltage ($OUT_A$ = $V_{CC}$ or $OUT_B$ = $V_{CC}$ to GND) | $I_{OUT}$ = 100 mA; $t_{CLAMP}$ = 1 ms | 38 | 46 | | V |
| $T_{TSD\_HS}$ | High-side thermal shutdown temperature | $IN_x$ = 2.1 V | 150 | 175 | 200 | °C |
| $T_{TR\_HS}$ | High-side thermal reset temperature | | 135 | | | °C |
| $T_{HYST\_HS}$ | High-side thermal hysteresis ($T_{SD\_HS}$ - $T_{R\_HS}$) | | | 7 | | °C |
| $T_{TSD\_LS}$ | Low-side thermal shutdown temperature | $IN_x$ = 0 V | 150 | 175 | 200 | °C |
| $V_{CL}$ | Total clamp voltage ($V_{CC}$ to GND) | $I_{OUT}$ = 100 mA; $t_{CLAMP}$ = 1 ms | 38 | 46 | 52 | V |
| $V_{OL}$ | OFF-state open-load voltage detection threshold | $IN_A$ = $IN_B$ = 0; PWM = 0; $V_{SEL0}$ = 5 V for CHA; $V_{SEL0}$ = 0 V and within $t_{D\_STBY}$ for CHB | 2 | 3 | 4 | V |
| $I_{L(off2)}$ | OFF-state output sink current | $IN_A$ = $IN_B$ = 0; $V_{OUTx}$ = $V_{OL}$; PWM = 0 V; $V_{SEL0}$ = 5 V for CHA; $V_{SEL0}$ = 0 V and within $t_{D\_STBY}$ for CHB | -100 | | -15 | µA |
| $t_{DSTKON}$ | OFF-state diagnostic delay time from falling edge of INPUT (see *Figure 4*) | $IN_A$ = 5 V to 0 V; $IN_B$ = 0 V; $V_{SEL0}$ = 5 V; $I_{OUT}$ = 0 A; $V_{OUTA}$ = 4 V; PWM = 0 V | 40 | 150 | 350 | µs |
| $t_{D\_VOL}$ (1) | OFF-state diagnostic delay time from rising edge of $V_{OUT}$ (see *Figure 11*) | $IN_A$ = $IN_B$ = 0 V; PWM = 0 V; $V_{OUTx}$ = 0 V to 4 V; $V_{SEL0}$ = 5 V for CHA; $V_{SEL0}$ = 0 V and within $t_{D\_STBY}$ for CHB | | 5 | 30 | µs |

**Table 9. Protections and diagnostics ($V_{CC}$ = 7 V up to 18 V; -40°C < $T_j$ < 150°C)**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{Latch\_RST\_HD}$(1) | Input reset time for high-side fault unlatch (see *Figure 9*) | $V_{INx}$ = 5 V to 0 V; HSDx faulting | 3 | 10 | 20 | µs |
| $t_{Latch\_RST\_LS}$(1) | Input reset time for low-side fault unlatch (see *Figure 10*) | $V_{INx}$ = 0 V to 5 V; LSDx faulting | 3 | 10 | 20 | µs |

1. Parameter guaranteed by design and characterization; not subjected to production test.

**Table 10. CS (7 V < $V_{CC}$ < 18 V; -40 °C < $T_j$ < 150 °C)**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{SENSE\_CL}$ | MultiSense clamp voltage | $V_{CC}$ = 18 V; $I_{SENSE}$ = -5 mA | | 11 | | V |
| | | $V_{CC}$ = 18 V; $I_{SENSE}$ = 5 mA | -13 | | -9 | V |
| $K_0$ | $I_{OUT}/I_{SENSE}$ | $I_{OUT}$ = 0.05 A; $V_{SENSE}$ = 0.5 V; $T_j$ = -40°C to 150°C | 420 | | | |
| $K_1$ | $I_{OUT}/I_{SENSE}$ | $I_{OUT}$ = 0.2 A; $V_{SENSE}$ = 0.5 V; $T_j$ = -40°C to 150°C | 710 | 1190 | 1670 | |
| $K_2$ | $I_{OUT}/I_{SENSE}$ | $I_{OUT}$ = 2.5 A; $V_{SENSE}$ = 4 V; $T_j$ = -40°C to 150°C | 980 | 1120 | 1247 | |
| $K_3$ | $I_{OUT}/I_{SENSE}$ | $I_{OUT}$ = 4 A; $V_{SENSE}$ = 4 V; $T_j$ = -40°C to 150°C | 990 | 1120 | 1235 | |
| $dK_0/K_0$(1)(2) | Analog sense current drift | $I_{OUT}$ = 0.05 A; $V_{SENSE}$ = 0.5 V; $T_j$ = -40°C to 150°C | -25 | | 25 | % |
| $dK_1/K_1$(1)(2) | Analog sense current drift | $I_{OUT}$ = 0.2 A; $V_{SENSE}$ = 0.5 V; $T_j$ = -40°C to 150°C | -21 | | 21 | % |
| $dK_2/K_2$(1)(2) | Analog sense current drift | $I_{OUT}$ = 2.5 A; $V_{SENSE}$ = 4 V; $T_j$ = -40°C to 150°C | -5 | | 5 | % |
| $dK_3/K_3$(1)(2) | Analog sense current drift | $I_{OUT}$ = 4 A; $V_{SENSE}$ = 4 V; $T_j$ = -40°C to 150°C | -4 | | 4 | % |
| $V_{SENSE\_SAT}$ | Max analog sense output voltage | $V_{CC}$ = 7 V; $R_{SENSE}$ = 10 kΩ; $V_{SEL0}$ = 5 V; $I_{OUTA}$ = 4 A; $V_{INA}$ = 5 V; PWM = 0; $T_j$ = 150 °C | 5 | | | V |
| $I_{SENSE0}$ | MultiSense leakage current | $I_{OUT}$ = 0 A; $V_{SENSE}$ = 0 V; $IN_x$ = 0 V; $SEL_0$ = 0; $T_j$ = -40°C to 150°C (standby) | 0 | | 0.5 | µA |
| | | $I_{OUT}$ = 0 A; $V_{SENSE}$ = 0 V; $IN_x$ = 0 V; $SEL_0$ = 5 V; $T_j$ = -40°C to 150°C (no standby) | 0 | | 0.5 | µA |
| | | $IN_x$ = 5 V; PWM = 5 V: $T_j$ = -40°C to 150°C; $I_{OUT}$ = 0 A | 0 | | 5 | µA |

**Table 10. CS (7 V < $V_{CC}$ < 18 V; -40 °C < $T_j$ < 150 °C) (continued)**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{SENSEH}$ | MultiSense output voltage in fault condition | $V_{CC}$ = 13 V; $R_{SENSE}$ = 1 kΩ<br>– E.g: $OUT_A$ in open-load<br>$IN_A$ = 0 V; $I_{OUTA}$ = 0 A;<br>$V_{OUTA}$ = 4 V; $V_{SEL0}$ = 5 V | 5 | | 7 | V |
| $V_{OUT\_MSD}$(2) | Output Voltage for MultiSense shutdown | $V_{INA}$ = 5 V; $V_{INB}$ = 0 V;<br>$V_{SEL0}$ = 5 V; $R_{SENSE}$ = 2.7 kΩ<br>$I_{OUT}$ = 2.5 A | | 5 | | V |
| $I_{SENSE\_SAT}$(2) | MultiSense saturation current | $V_{CC}$ = 13 V; $V_{SENSE}$ = 4 V;<br>$V_{INA}$ = 5 V; $V_{INB}$ = 0 V;<br>$V_{SEL0}$ = 5 V; $T_j$ = 150 °C | 5.8 | | | mA |
| $I_{OUT\_SAT}$(2) | Output saturation current | $V_{CC}$ = 13 V; $V_{SENSE}$ = 4 V;<br>$V_{INA}$ = 5 V; $V_{INB}$ = 0 V;<br>$V_{SEL0}$ = 5 V; $I_{OUT}$ = 7 A; $T_j$ = 150°C | 7 | | | A |
| $I_{SENSEH}$ | MultiSense output voltage in fault condition | $V_{CC}$ = 13 V; $V_{SENSE}$ = $V_{SENSEH}$ | 7 | 20 | 30 | mA |

1. Analog sense current drift is deviation of factor K for a given device over (-40 °C to 150 °C and 9 V < $V_{CC}$ < 18 V) with respect to its value measured at $T_j$ = 25 °C, $V_{CC}$ = 13 V.
2. Parameter guaranteed by design and characterization; not subjected to production test.

**Figure 4. $T_{DSTKON}$**

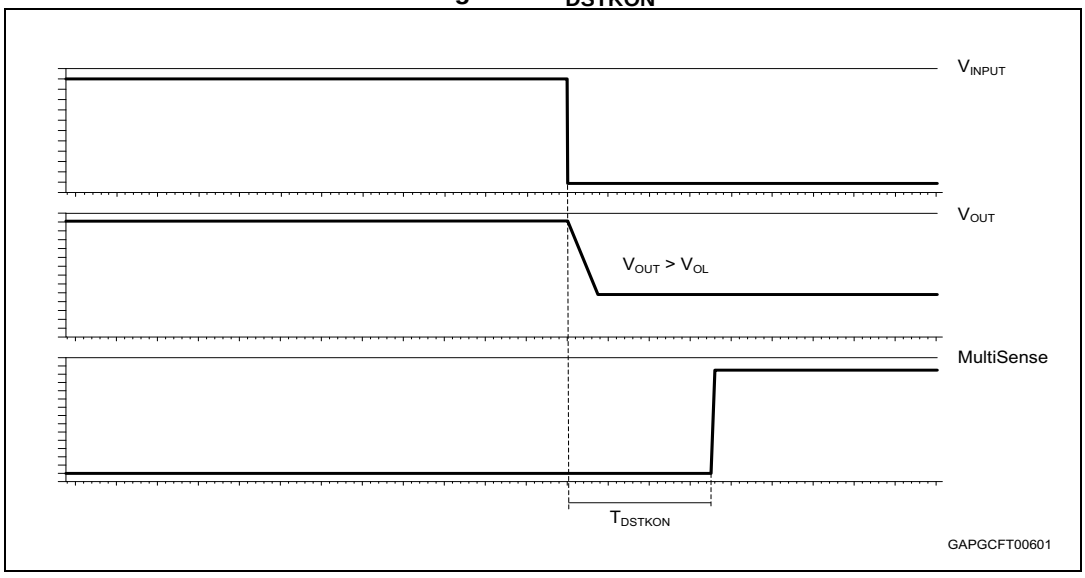


**Figure 5. Definition of the low-side switching times**

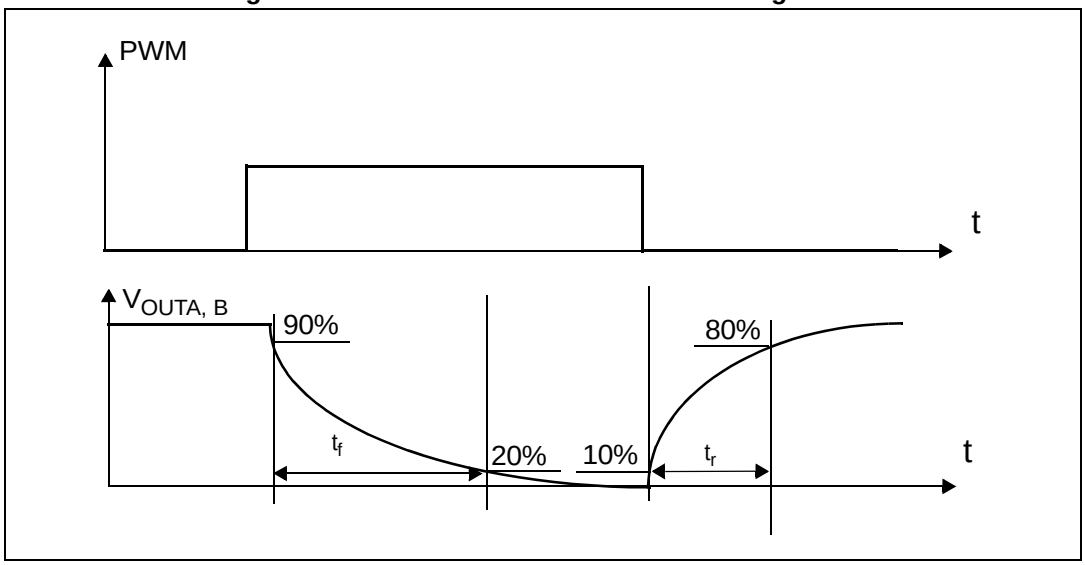



**Figure 6. Definition of the high-side switching times**

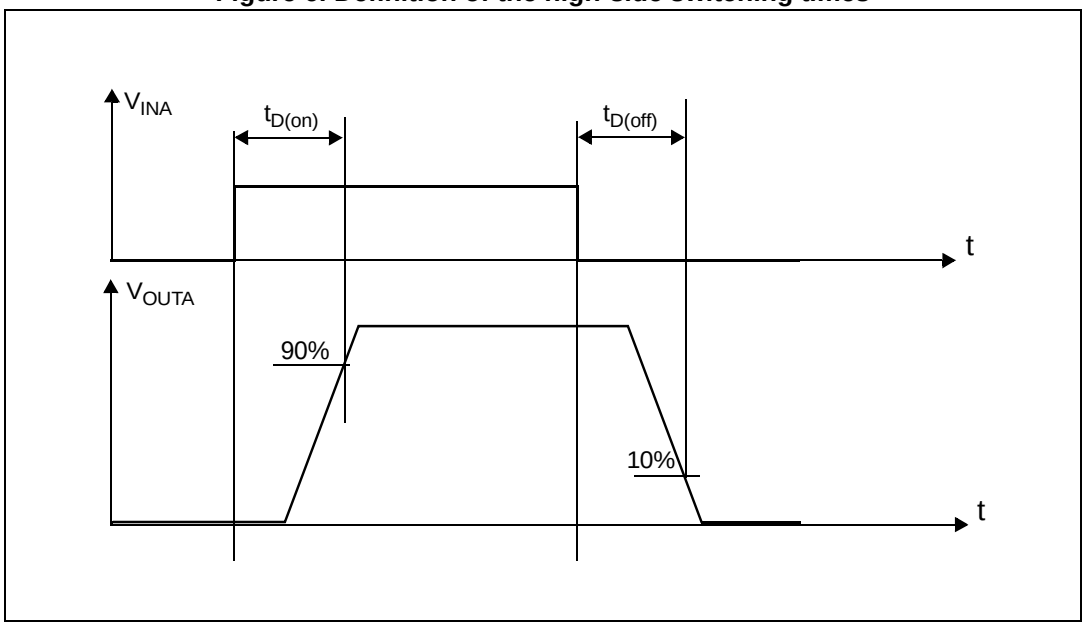


**Figure 7. Low-side turn-on delay time**

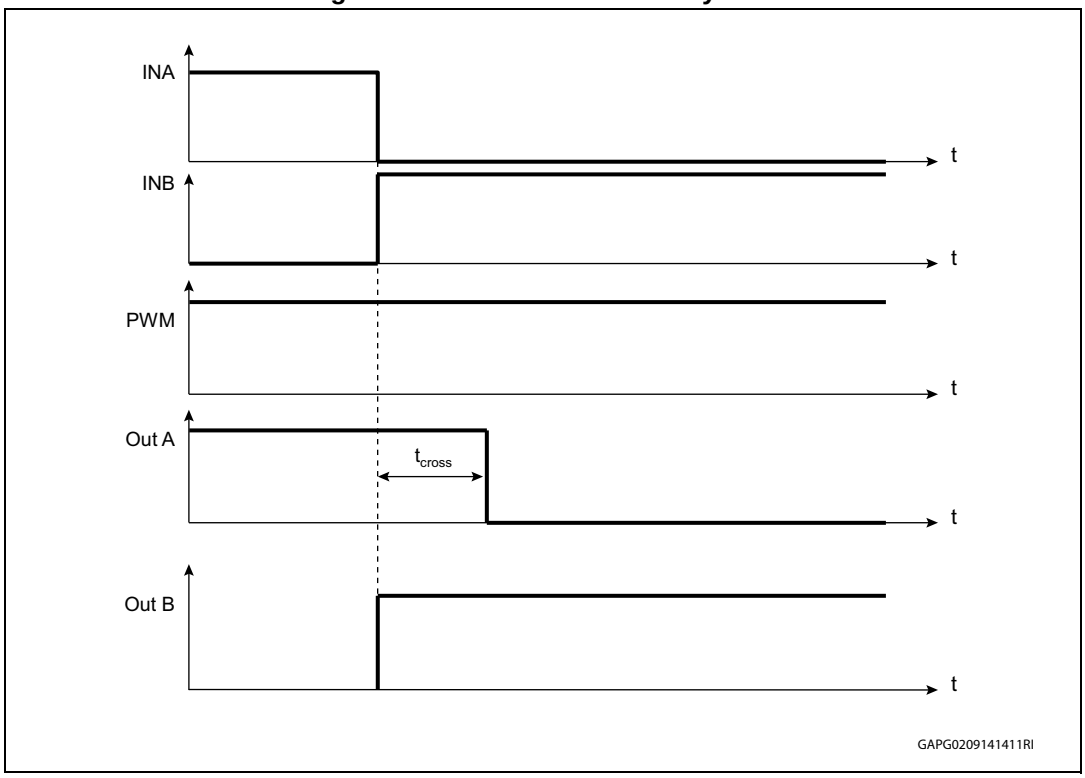



**Figure 8. Time to shutdown for the low-side driver**

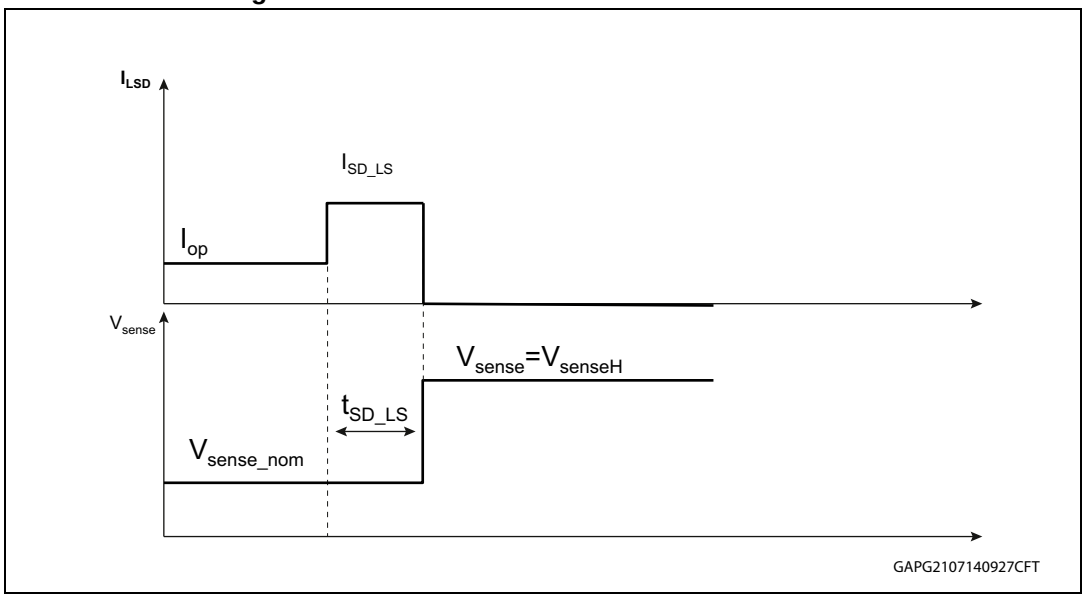


**Figure 9. Input reset time for HSD - fault unlatch**

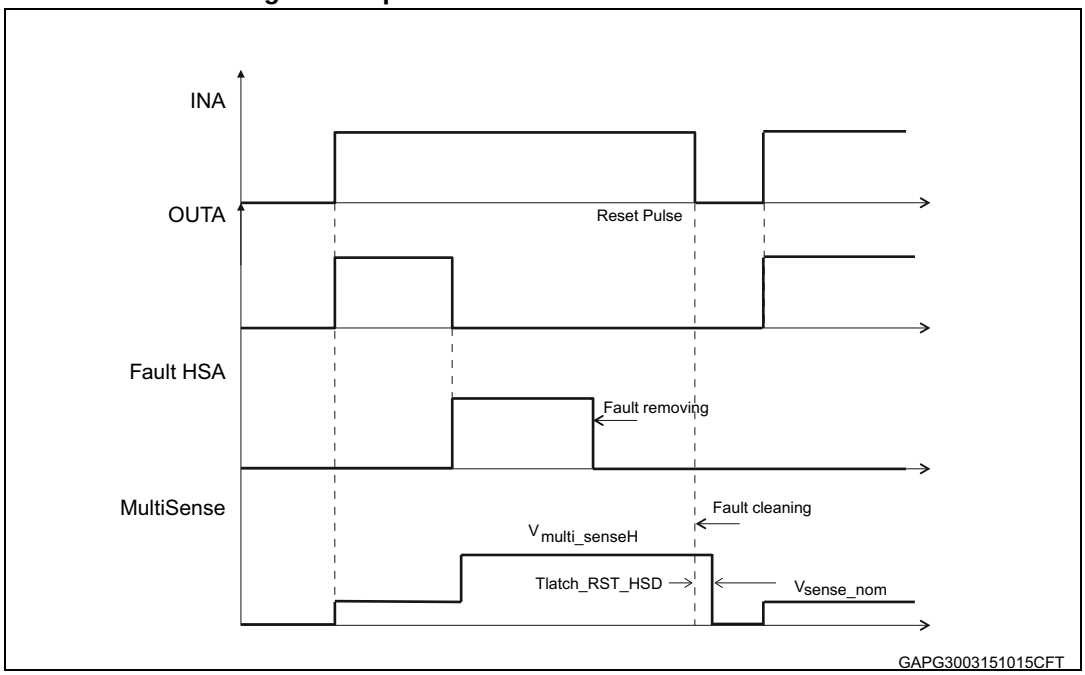



**Figure 10. Input reset time for LSD - fault unlatch**

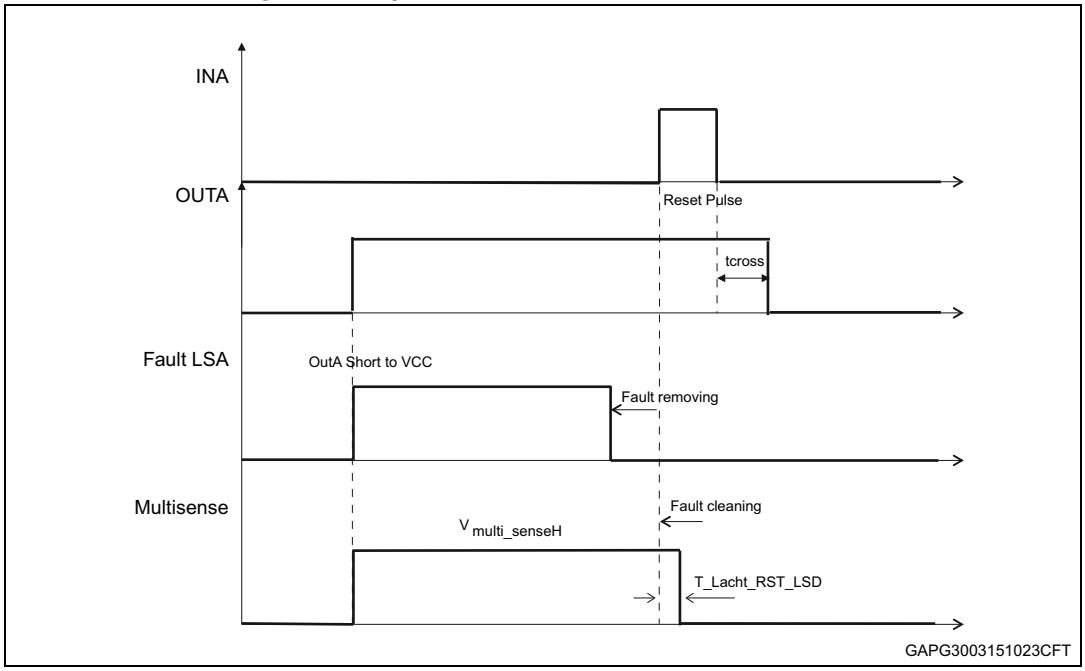


**Figure 11. OFF-state diagnostic delay time from rising edge of $V_{OUT}$ ($t_{D\_VOL}$)**

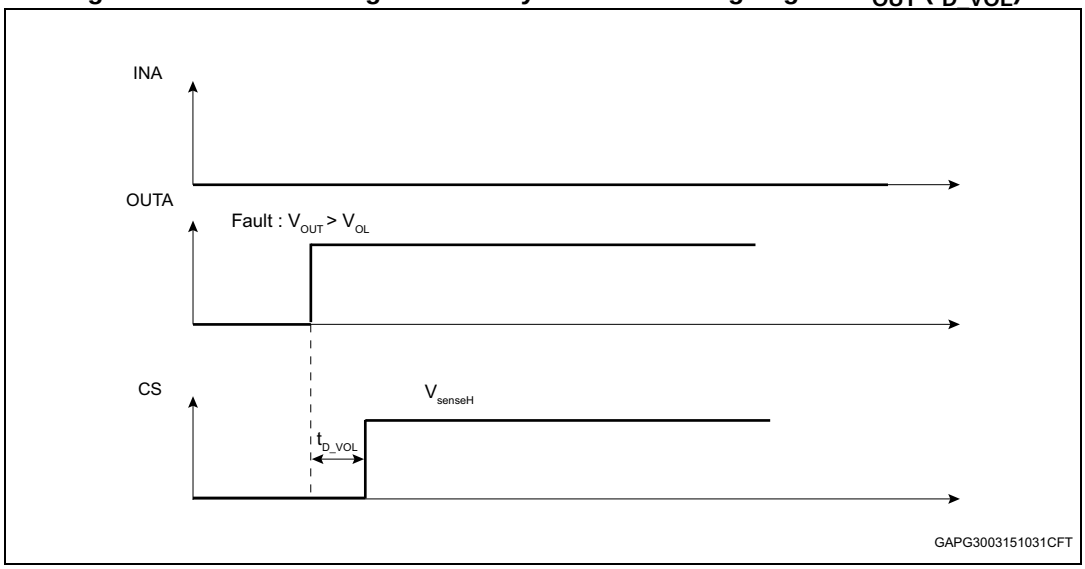


**Table 11. Operative condition - truth table**

| Pin status | | | | | HSDs and LDSs Status | | | |
|---|---|---|---|---|---|---|---|---|
| $IN_A$ | $IN_B$ | $SEL_0$ | PWM | CS | HSDA | LSDA | HSDB | LSDB |
| 1 | 1 | 1 | x | Current Monitoring HSDA | On | Off | On | Off |
| | | 0 | | Current Monitoring HSDB | | | | |
| 1 | 0 | 1 | 1 | Current Monitoring HSDA | On | Off | Off | On |
| | | | 0 | | On | Off | Off | Off |
| 1 | 0 | 0 | 1 | Hi-Z | On | Off | Off | On |
| | | | 0 | | On | Off | Off | Off |
| 0 | 1 | 1 | 1 | Hi-Z | Off | On | On | Off |
| | | | 0 | | Off | Off | On | Off |
| 0 | 1 | 0 | 1 | Current Monitoring HSDB | Off | On | On | Off |
| | | | 0 | | Off | Off | On | Off |
| 0 | 0 | 1 | 1 | Hi-Z | Off | On | Off | On |
| | | 0 | | | | | | |
| 0 | 0 | 1 | 0 | x(1) | Off | Off | Off | Off |
| | | 0(2) | | | Off | Off | Off | Off |

1. Refer to *Table 13: Off-state - truth table*
2. For $IN_A$ =$IN_B$=$SEL_0$ = PWM = 0, the device enters in standby after $t_{D\_STBY}$

**Table 12. On-state fault conditions - truth table**

| $IN_A$ | $IN_B$ | $SEL_0$ | PWM | $Out_A$ | $Out_B$ | CS | Fault description |
|---|---|---|---|---|---|---|---|
| On state diagnostic | | | | | | | |
| 0 | 0 | 0 | 1 | X | H | $V_{SENSEH}$ | Short to $V_{BATT}$ on Leg B |
| 0 | 0 | 1 | 1 | H | X | $V_{SENSEH}$ | Short to $V_{BATT}$ on Leg A |
| 0 | 1 | 0 | X | X | L | $V_{SENSEH}$ | Out B short to GND |
| 0 | 1 | 1 | 1 | H | H | $V_{SENSEH}$ | Out A short to $V_{CC}$ |
| 1 | 0 | 0 | 1 | H | H | $V_{SENSEH}$ | Out B short to $V_{CC}$ |
| 1 | 0 | 1 | X | L | L | $V_{SENSEH}$ | Out A short to GND |
| 1 | 1 | 0 | X | X | L | $V_{SENSEH}$ | Short to GND on Leg B |
| 1 | 1 | 1 | X | L | X | $V_{SENSEH}$ | Short to GND on Leg A |

**Table 13. Off-state - truth table**

| $IN_A$ | $IN_B$ | $SEL_0$ | PWM | $Out_A$ | $Out_B$ | CS | Description |
|---|---|---|---|---|---|---|---|
| Off-state diagnostic | | | | | | | |
| 0 | 0 | 1 | 0 | $V_{outA}>V_{OL}$ | x | $V_{SENSEH}$ | Case 1. $Out_A$ shorted to $V_{CC}$ if no pull-up is applied<br>Case 2. No open-load in full bridge configuration with an external pull-up on $Out_B$<br>Case 3. open-load in half bridge configuration with an external pull-up on $Out_A$(motor connected between $Out_A$ and Ground) |
| | | | | $V_{outA}<V_{OL}$ | x | Hi-Z | Case 1. Open-load in full Bridge configuration with an external pull-up on $Out_B$<br>Case 2. No open-load in half Bridge configuration with external pull-up on $Out_A$ (motor connected between $Out_A$ and Ground) |
| | | 0(1)(2) | | X | $V_{outB}>V_{OL}$ | $V_{SENSEH}$ | Case 1. $Out_B$ shorted to $V_{CC}$ if no pull-up is applied<br>Case 2. No open-load in full bridge configuration with external pull-up on $Out_A$<br>Case 3. Open-load in half bridge configuration with external pull-up on $Out_B$ (motor connected between $Out_B$ and Ground) |
| | | | | X | $V_{outB}<V_{OL}$ | Hi-Z | Case1. Open-load in full Bridge configuration with an external pull-up on $Out_A$<br>Case 2. No open-load in half Bridge configuration with external pull-up on $Out_B$ (motor connected between $Out_B$ and Ground) |

1. The device enters standby mode after $t_{D\_STBY}$
2. To power on the device from the standby, it is recommended to toggle $IN_A$ or $IN_B$ from 0 to 1 first and then PWM from 0 to 1 to avoid any over-stress on the device in case of short-to-battery.

## 2.4 Waveforms

**Figure 12. Normal operative conditions**

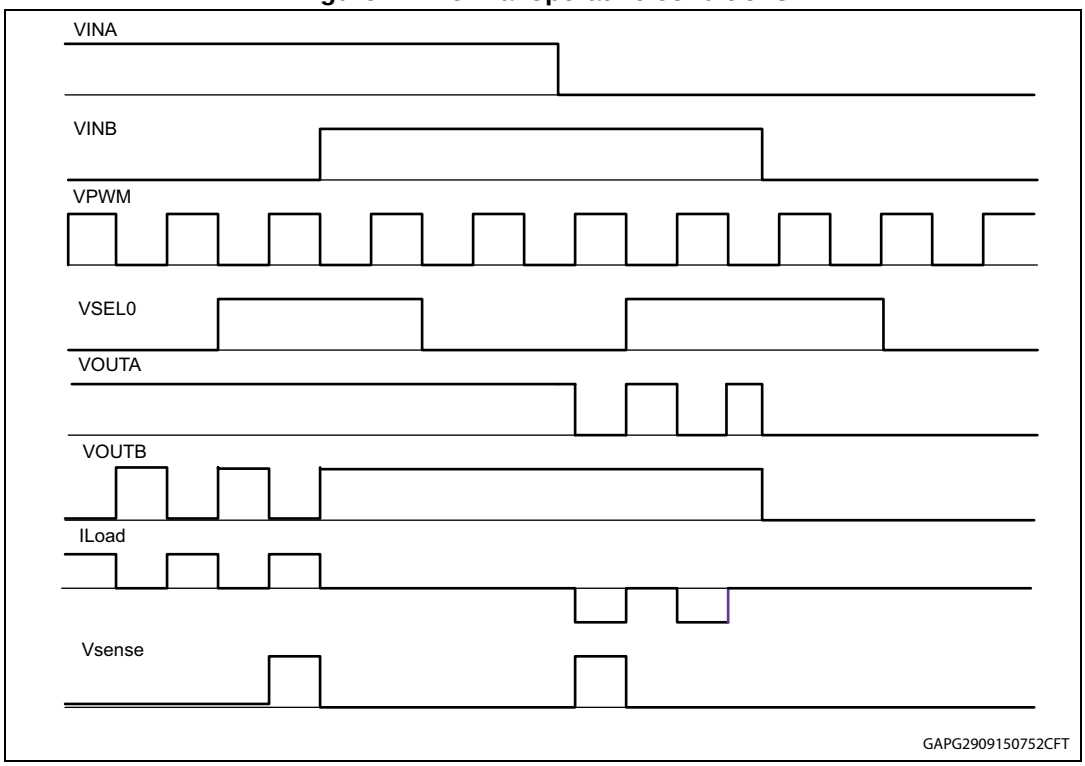



**Figure 13. OUT shorted to ground and short clearing**

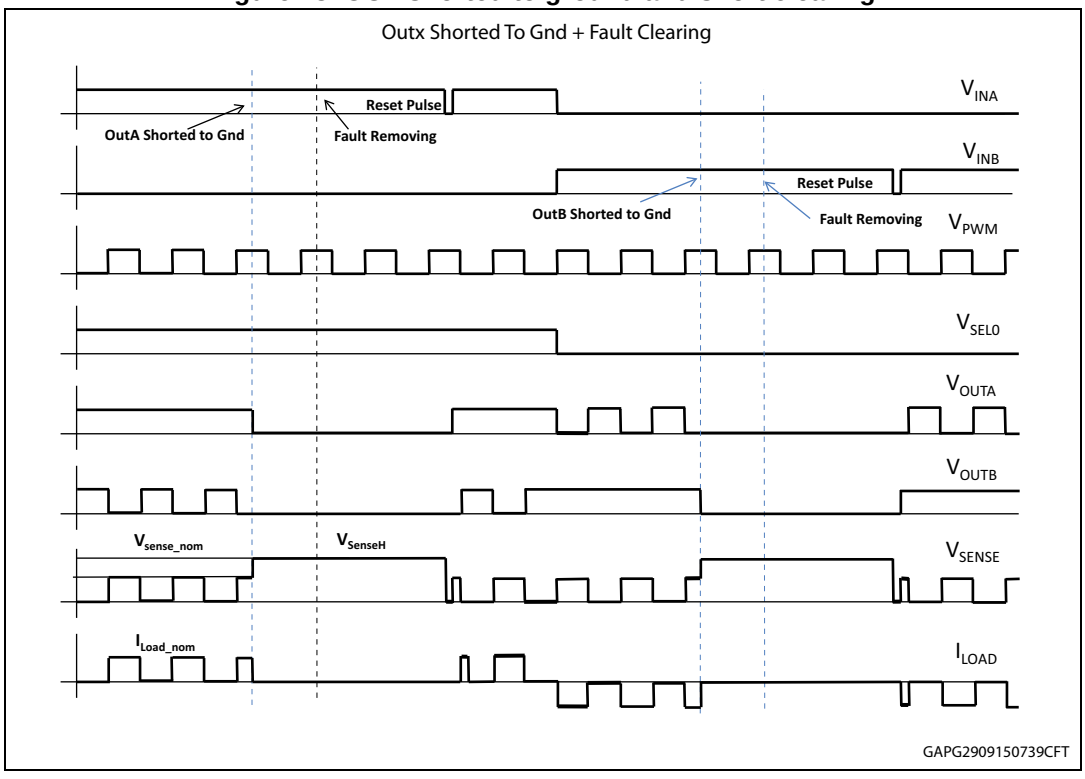
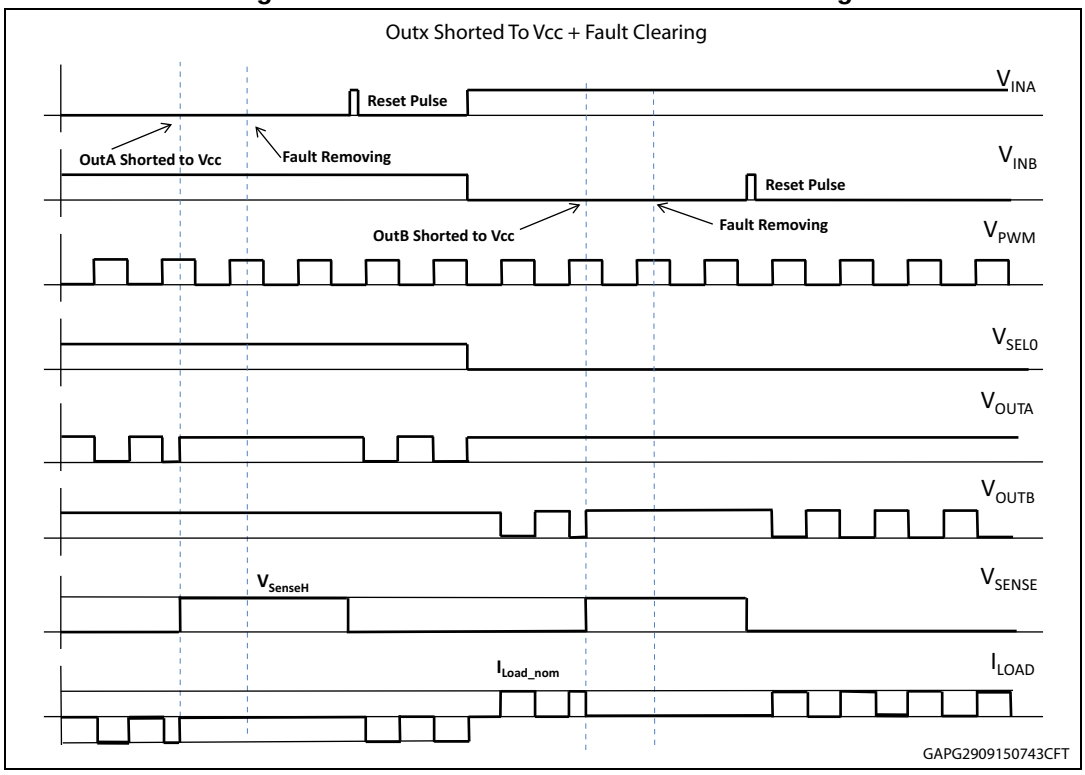


**Figure 14. OUT shorted to Vcc and short clearing**



# 3 Application information

Here following there is the typical application schematic suggested for a proper operation of the device in DC or PWM conditions.

**Figure 15. Application schematic with reverse battery protection connected to Vbatt**

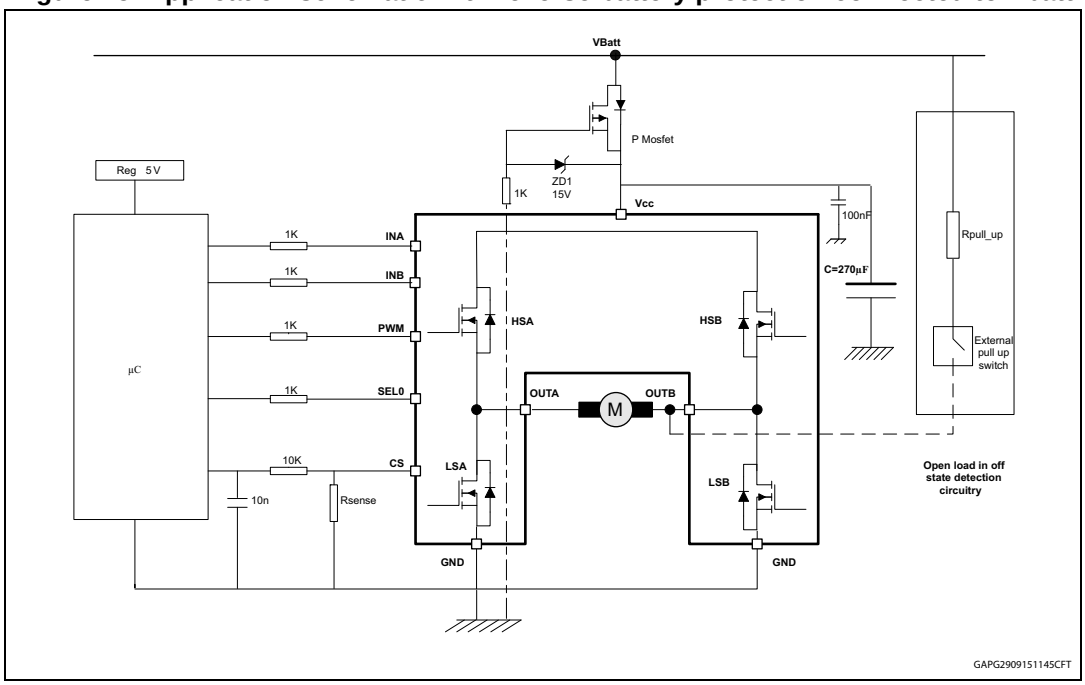



**Figure 16. Application schematic with reverse battery protection connected to GND**

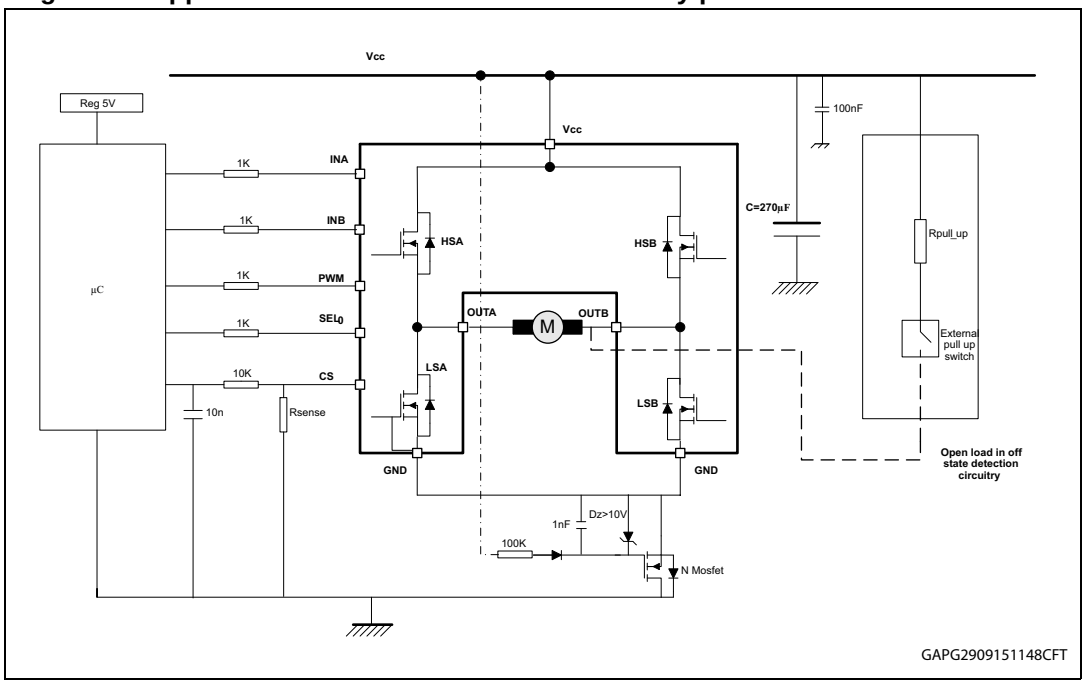
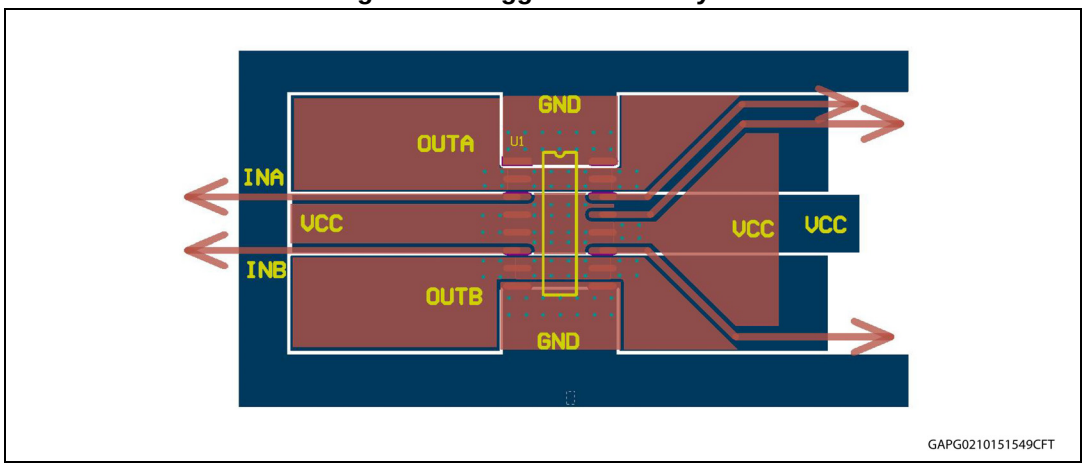


**Figure 17. Suggested PCB layout**




*Note: PCB layout recommendation:*
*Optimized connection (short) between Drain LSD and Source HSD*
*Optimized GNDa and GNDb connection (symmetric connection)*

## 3.1 Reverse battery protection

Three possible solutions can be considered:

- A Schottky diode D connected to $V_{CC}$ pin
- An N-channel MOSFET connected to the GND pin
- A P-channel MOSFET connected to the $V_{CC}$ pin

In case the reverse battery protection is not present, the device sustains no more than -15 A because of the two Body diodes of the Power MOSFETs. Additionally, in reverse battery condition the I/Os of the device is pulled down to the $V_{CC}$ line (approximately -1.5 V).

Series resistor must be inserted to limit the current sunk from the microcontroller I/Os. If $I_{Rmax}$ is the maximum target reverse current through microcontroller I/Os, series resistor is:

$$R = \frac{V_{IOs} - V_{CC}}{I_{Rmax}}$$

## 3.2 OFF-state open-load detection – External circuitry dimensioning

The detection of an open-load in off state requires an external circuitry to be connected between Output and $V_{BATT}$.

For the detection it is necessary to put one network on each leg in case of Half Bridge operation or one network on one of the output in case of full bridge (see *Table 13: Off-state - truth table*).

The external circuitry is made up by an external pull-up resistor $R_{pull\_up}$ connecting the output to a positive supply voltage $V_{PU}$ ($V_{Batt}$).

It is preferable to switch-off $V_{PU}$ by using an external pull_up switch to reduce the overall standby current during he module standby mode.

$R_{pull\_up}$ must be dimensioned to ensure that in normal operative conditions $V_{OUT} > V_{OLmax}$.

To satisfy this condition the $R_{pull\_up}$ must be selected according to:

- if the device is used in half bridge configuration, the equation is:

$$R_{pull\_up} < \frac{V_{BATTmin} - V_{OLmax}}{I_{L(off2)min[@VOLmax]}}$$

- if the device is used in H-bridge configuration, the equation is:

$$R_{pull\_up} < \frac{V_{BATTmin} - V_{OLmax}}{2 \times I_{L(off2)min[@VOLmax]}}$$

## 3.3 Immunity against transient electrical disturbances

The immunity of the device against transient electrical emissions, conducted along the supply lines and injected into the $V_{CC}$ pin, is tested in accordance with ISO7637-2:2011 (E) and ISO 16750-2:2010.

The related function performance status classification is shown in *Table 14*.

Test pulses are applied directly to DUT (Device Under Test) both in ON and OFF-state and in accordance to ISO 7637-2:2011(E), chapter 4. The DUT is intended as the present device only, without components and accessed through $V_{CC}$ and GND terminals.

Status II is defined in ISO 7637-1 Function Performance Status Classification (FPSC) as follows: “The function does not perform as designed during the test but returns automatically to normal operation after the test”.

**Table 14. ISO 7637-2 - electrical transient conduction along supply line**

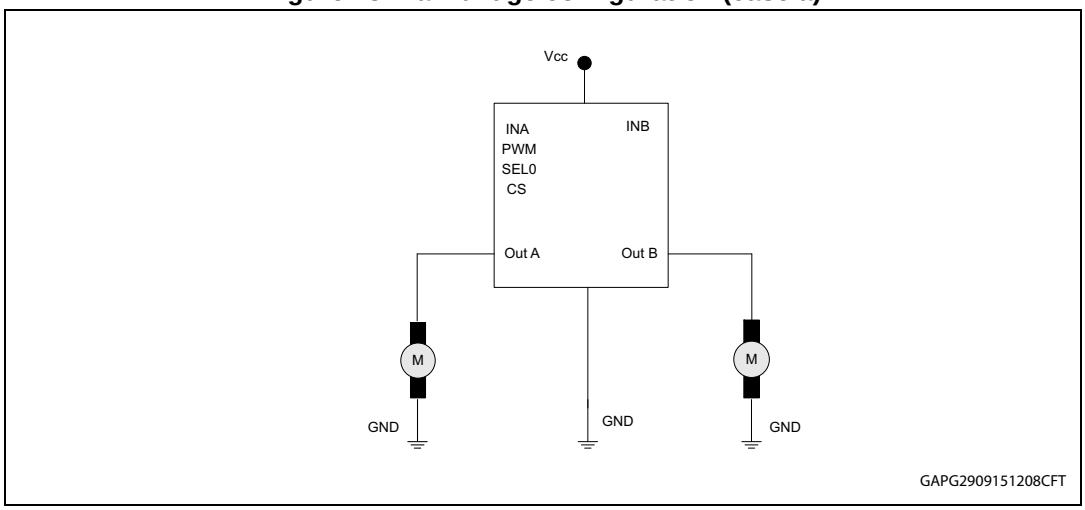
| Test Pulse 2011(E) | Test pulse severity level with Status II functional performance status | | Minimum number of pulses or test time | Burst cycle / pulse repetition time | | Pulse duration and pulse generator internal impedance |
|---|---|---|---|---|---|---|
| | Level | $U_S$(1) | | min | max | |
| 1 | III | -112 V | 500 pulses | 0,5 s | | 2ms, 10 Ω |
| 2a | III | +55 V | 500 pulses | 0,2 s | 5 s | 50µs, 2 Ω |
| 3a | IV | -220 V | 1h | 90 ms | 100 ms | 0.1µs, 50 Ω |
| 3b | IV | +150 V | 1h | 90 ms | 100 ms | 0.1µs, 50 Ω |
| 4(2) | IV | -7 V | 1 pulse | | | 100ms, 0.0 1Ω |
| **Load dump according to ISO 16750-2:2010** | | | | | | |
| Test B(3) | | 40 V | 5 pulse | 1 min | | 400 ms, 2 Ω |

1. $U_S$ is the peak amplitude as defined for each test pulse in ISO 7637-2:2011(E), chapter 5.6.

2. Test pulse from ISO 7637-2:2004(E).
3. With 40 V external suppressor referred to ground (-40°C < $T_j$ < 150°C).

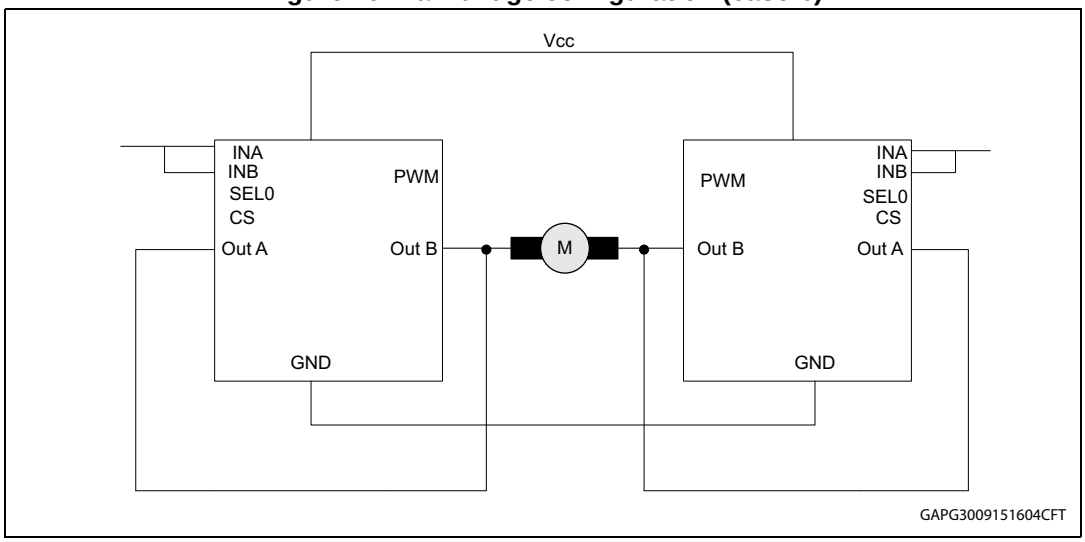
## 3.4 Device configurations

**Figure 18. Half-bridge configuration (case a)**



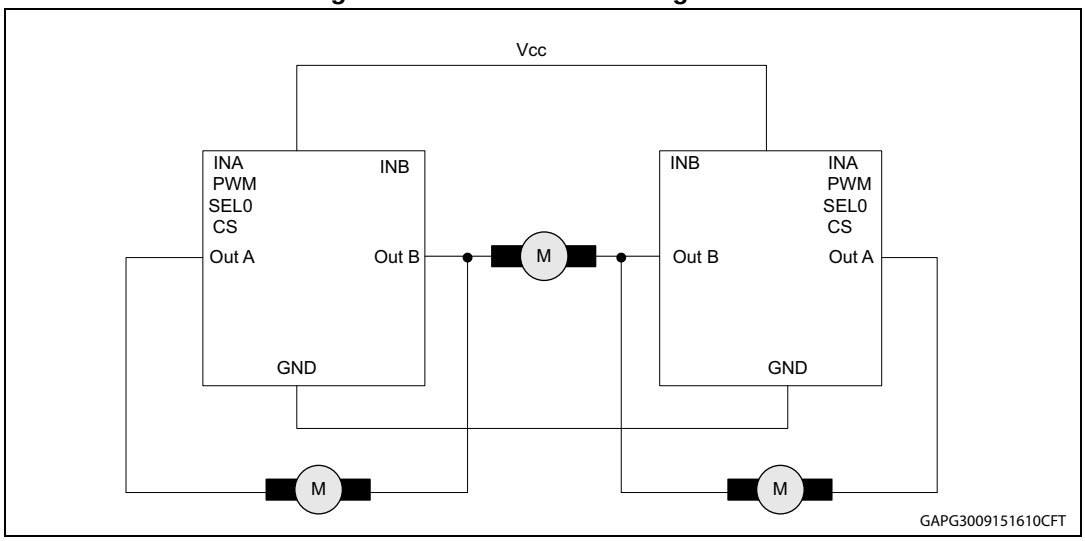

*Note: The VNH7100AS can be used in half bridge configuration as the two legs can be independently driven. The SEL0 pin can be used to address the diagnostic on the CS according to the operative truth table.*

**Figure 19. Half-bridge configuration (case b)**




*Note: The VNH7100AS can be used in applications where an half-bridge with a resistance of 50 mΩ per leg is needed.*

**Figure 20. Multi-motors configuration**




*Note: The VNH7100AS can easily be designed in multi motor driving configuration in the applications where only one motor at a time must be activated. The SEL0 pin can be used to read the diagnostic on the CS according to the operative truth table.*

# 4 Package and PCB thermal data

## 4.1 SO16-N thermal data

**Figure 21. PCB layout (top and bottom): footprint, 2+2+2 cm$^2$, 8+8+8 cm$^2$**

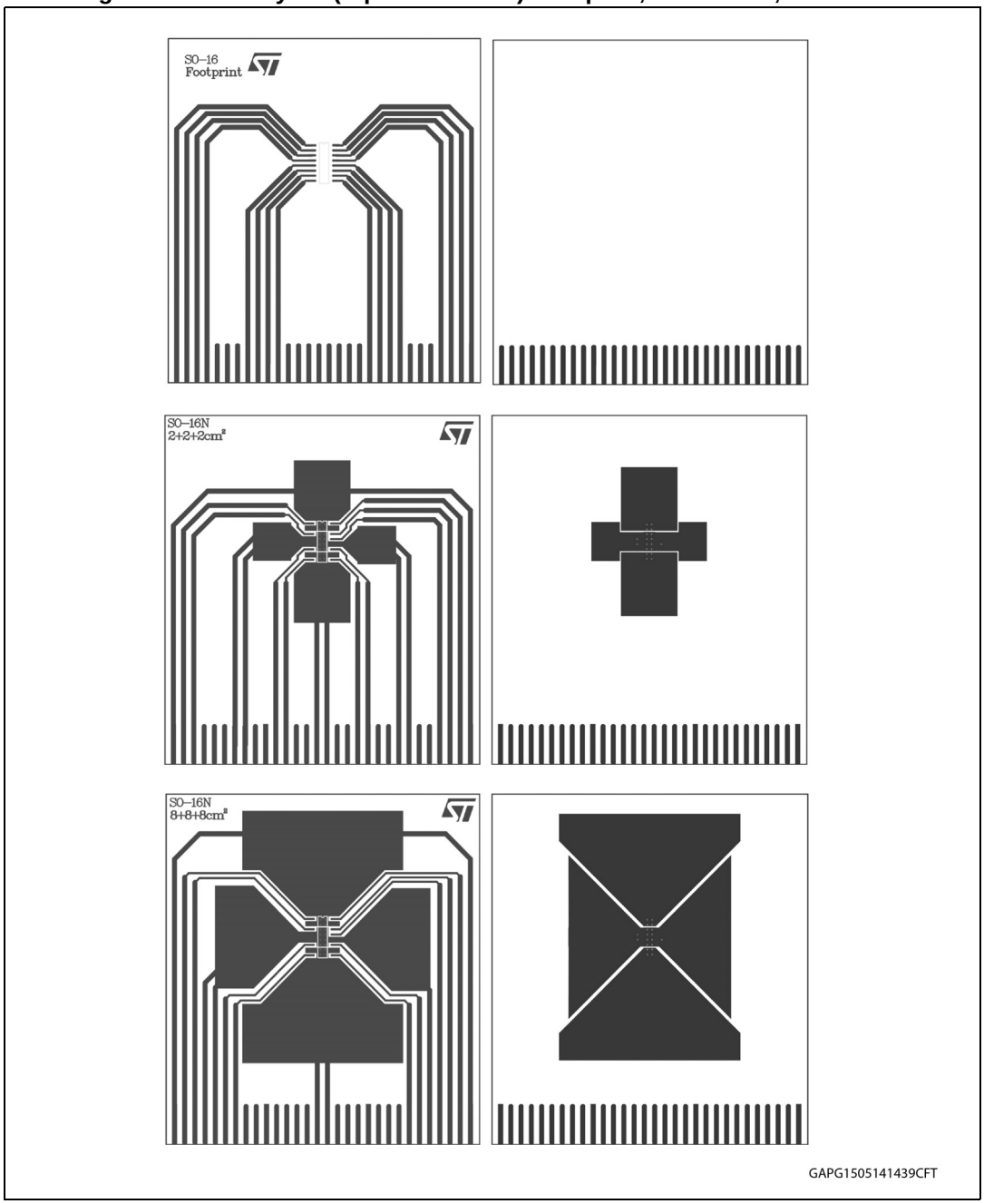
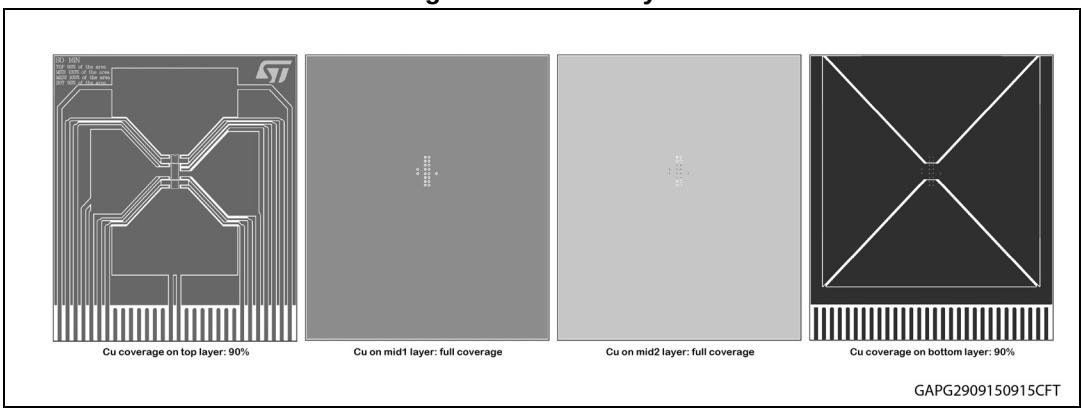


**Figure 22. PCB 4 layer**




*Note: Board finish thickness 1.6 mm +/- 10%; Board double layer and four layers; Board dimension 77x86 mm; Board Material FR4; Cu thickness 0.070mm (outer layers); Cu thickness 0.035mm (inner layers); Thermal vias separation 1.2 mm; Thermal via diameter 0.3 mm +/- 0.08 mm; Cu thickness on vias 0.025 mm.*

## 4.2 Package thermal data

### 4.2.1 Thermal characterization in steady state conditions

**Figure 23. Chipset configuration configuration in steady state conditions**

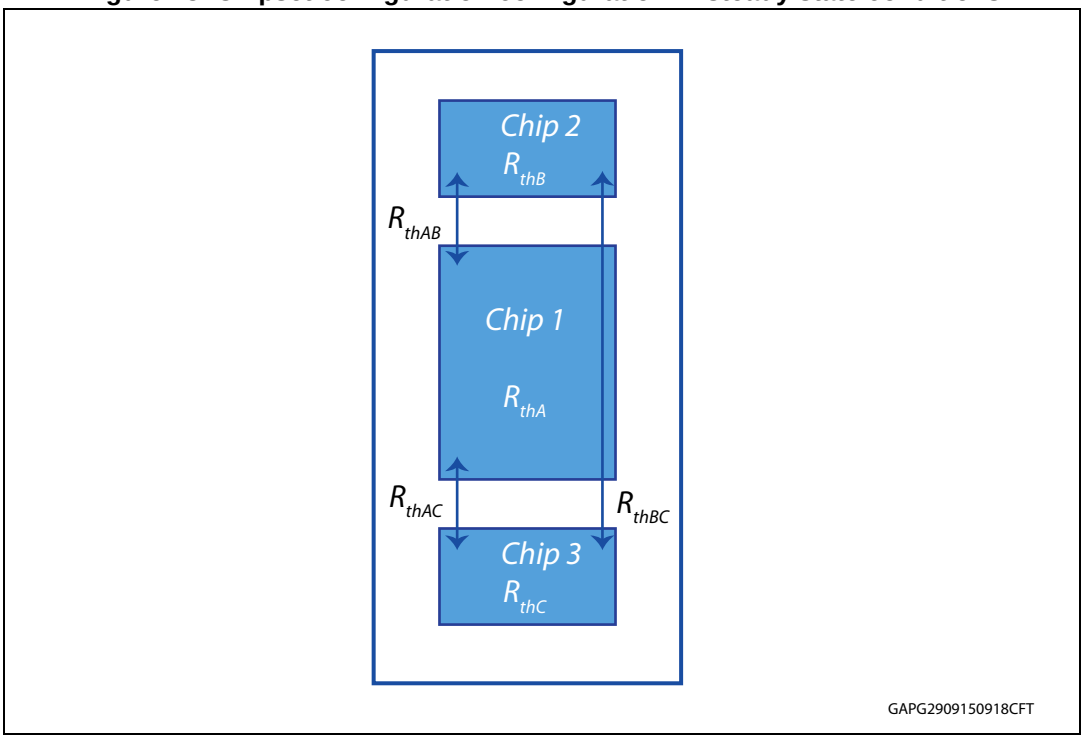


**Figure 24. Auto and mutual $R_{thj\text{-}amb}$ vs. PCB heat-sink area in open box free air condition**

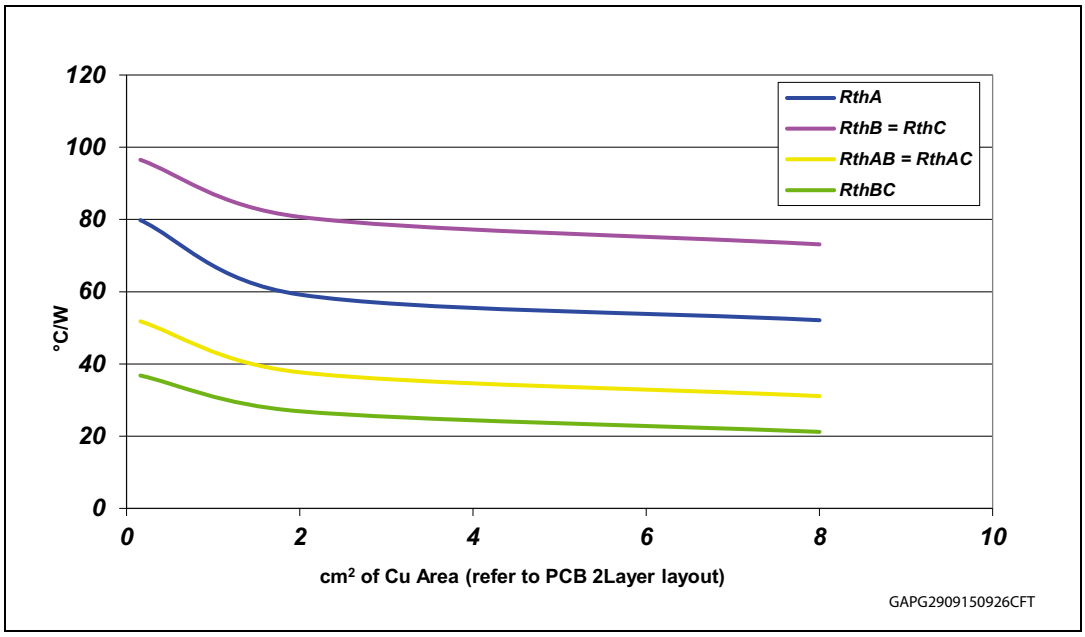



**Table 15. Thermal model for junction temperature calculation in steady-state conditions**

| Chip 1 | Chip 2 | Chip 3 | Tjchip1 | Tjchip2 | Tjchip3 |
|---|---|---|---|---|---|
| ON | OFF | ON | $P_{dchip1} \cdot R_{thA} + P_{dchip3} \cdot R_{thAC} + T_{amb}$ | $P_{dchip1} \cdot R_{thAB} + P_{dchip3} \cdot R_{thBC} + T_{amb}$ | $P_{dchip1} \cdot R_{thAC} + P_{dchip3} \cdot R_{thC} + T_{amb}$ |
| ON | ON | OFF | $P_{dchip1} \cdot R_{thA} + P_{dchip2} \cdot R_{thAB} + T_{amb}$ | $P_{dchip1} \cdot R_{thAB} + P_{dchip2} \cdot R_{thB} + T_{amb}$ | $P_{dchip1} \cdot R_{thAC} + P_{dchip2} \cdot R_{thBC} + T_{amb}$ |
| ON | OFF | OFF | $P_{dchip1} \cdot R_{thA} + T_{amb}$ | $P_{dchip1} \cdot R_{thAB} + T_{amb}$ | $P_{dchip1} \cdot R_{thAC} + T_{amb}$ |
| ON | ON | ON | $P_{dchip1} \cdot R_{thA} + (P_{dchip2} + P_{dchip3}) \cdot R_{thAB} + T_{amb}$ | $P_{dchip2} \cdot R_{thB} + P_{dchip1} \cdot R_{thAB} + P_{dchip3} \cdot R_{thBC} + T_{amb}$ | $P_{dchip1} \cdot R_{thAB} + P_{dchip2} \cdot R_{thBC} + P_{dchip3} \cdot R_{thC} + T_{amb}$ |

### 4.2.2 Thermal characterization during transients

$T_{hs} = Pd_{hs} \cdot Z_{hs} + Z_{hsls} \cdot (Pd_{lsA} + Pd_{lsB}) + T_{amb}$

$T_{lsA} = Pd_{lsA} \cdot Z_{ls} + Pd_{hs} \cdot Z_{hsls} + Pd_{lsB} \cdot Z_{lsls} + T_{amb}$

$T_{lsB} = Pd_{lsB} \cdot Z_{ls} + Pd_{hs} \cdot Z_{hsls} + Pd_{lsA} \cdot Z_{lsls} + T_{amb}$

**Figure 25. HSD thermal impedance junction ambient single pulse**

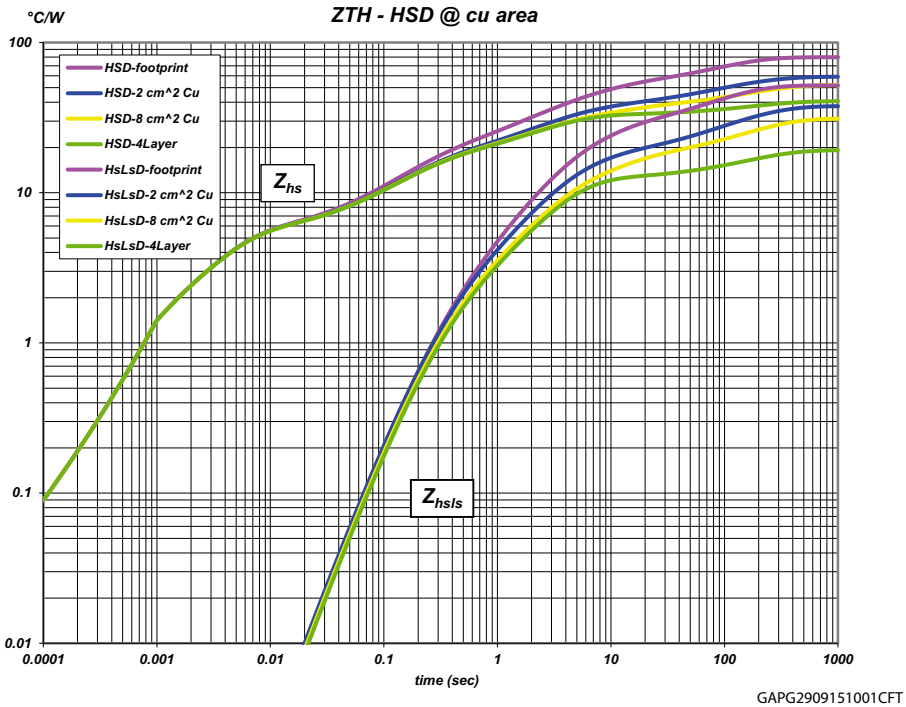



**Figure 26. LSD thermal impedance junction ambient single pulse**

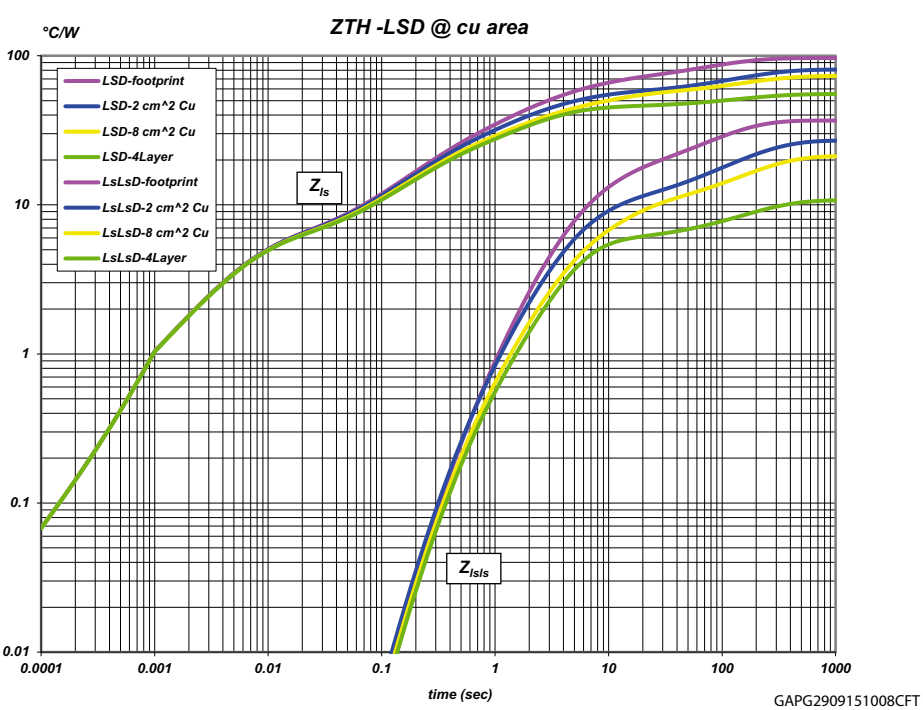


**Figure 27. Electrical equivalent model**

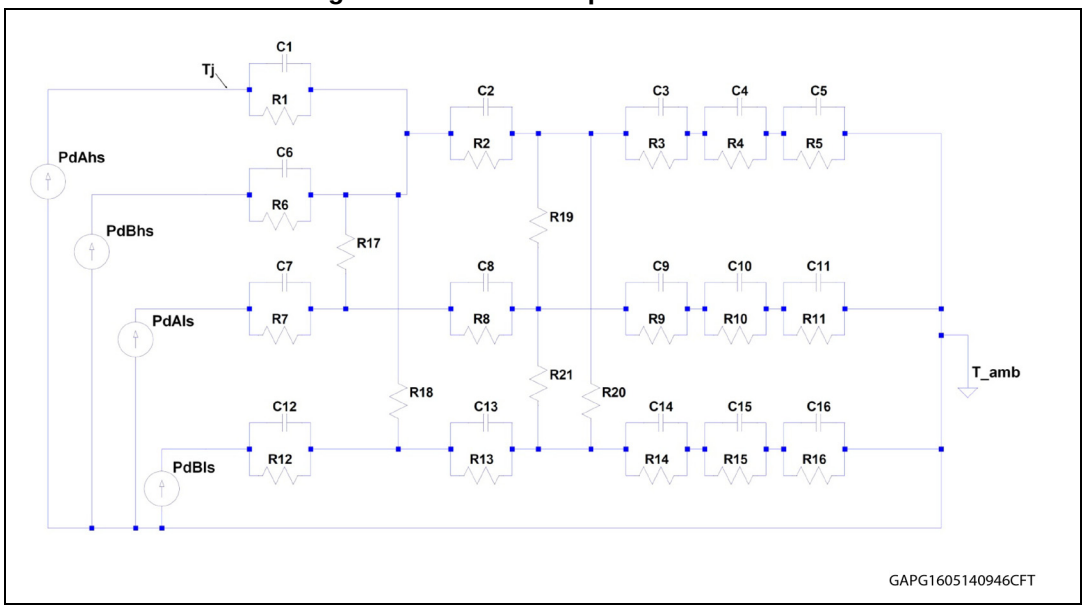



**Table 16. Thermal parameters**

| Area/island ($cm^2$) | FP | 2 | 8 | 4L |
|---|---|---|---|---|
| R1 (°C/W) | 5.3 | 5.3 | 5.3 | 5.3 |
| R2 (°C/W) | 12 | 12 | 12 | 12 |
| R3 (°C/W) | 30 | 25 | 25 | 30 |
| R4 (°C/W) | 42 | 12 | 12 | 2 |
| R5 (°C/W) | 85 | 45 | 30 | 17 |
| R6 (°C/W) | 5.3 | 5.3 | 5.3 | 5.3 |
| R7 (°C/W) | 5.1 | 5.1 | 5.1 | 5.1 |
| R8 (°C/W) | 12 | 12 | 12 | 12 |
| R9 (°C/W) | 30 | 30 | 30 | 42 |
| R10 (°C/W) | 68 | 52 | 48 | 10 |
| R11 (°C/W) | 75 | 80 | 60 | 26 |
| R12 (°C/W) | 5.1 | 5.1 | 5.1 | 5.1 |
| R13 (°C/W) | 12 | 12 | 12 | 12 |
| R14 (°C/W) | 30 | 30 | 30 | 42 |
| R15 (°C/W) | 68 | 52 | 48 | 10 |
| R16 (°C/W) | 75 | 80 | 60 | 26 |
| R17 (°C/W) | 120 | 100 | 100 | 100 |
| R18 (°C/W) | 120 | 100 | 100 | 100 |
| R19 (°C/W) | 180 | 170 | 170 | 170 |
| R20 (°C/W) | 180 | 170 | 170 | 170 |

Table 16. Thermal parameters (continued)

| Area/island ($cm^2$) | FP | 2 | 8 | 4L |
|---|---|---|---|---|
| C1 (W·s/°C) | 0.00065 | 0.00065 | 0.00065 | 0.00065 |
| C2 (W·s/°C) | 0.018 | 0.018 | 0.018 | 0.018 |
| C3 (W·s/°C) | 0.08 | 0.1 | 0.1 | 0.1 |
| C4 (W·s/°C) | 0.2 | 0.5 | 1 | 2 |
| C5 (W·s/°C) | 1.5 | 2 | 6 | 12 |
| C6 (W·s/°C) | 0.00065 | 0.00065 | 0.00065 | 0.00065 |
| C7 (W·s/°C) | 0.001 | 0.001 | 0.001 | 0.001 |
| C8 (W·s/°C) | 0.02 | 0.02 | 0.02 | 0.02 |
| C9 (W·s/°C) | 0.06 | 0.06 | 0.06 | 0.06 |
| C10 (W·s/°C) | 0.08 | 0.1 | 0.2 | 0.5 |
| C11 (W·s/°C) | 1 | 2.5 | 3 | 6 |
| C12 (W·s/°C) | 0.00065 | 0.00065 | 0.00065 | 0.00065 |
| C13 (W·s/°C) | 0.02 | 0.02 | 0.02 | 0.02 |
| C14 (W·s/°C) | 0.06 | 0.06 | 0.06 | 0.06 |
| C15 (W·s/°C) | 0.08 | 0.1 | 0.2 | 0.5 |
| C16 (W·s/°C) | 1 | 2.5 | 3 | 6 |

# 5 Package and packing information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

## 5.1 SO-16N mechanical data

**Figure 28. SO-16N package dimensions**

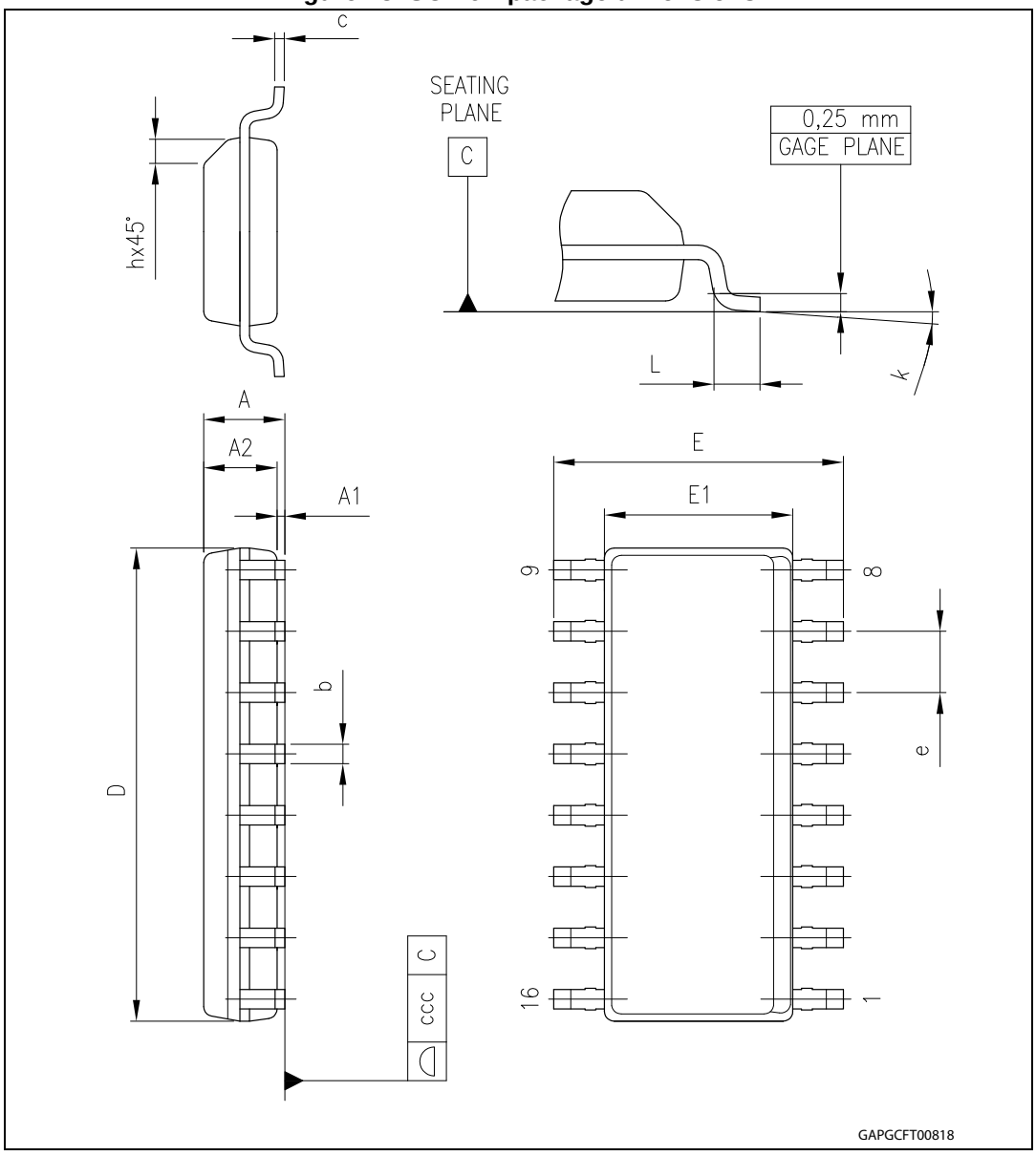


Table 17. SO-16N mechanical data

| Symbol | Millimeters | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | | | 1.75 |
| A1 | 0.10 | | 0.25 |
| A2 | 1.25 | | |
| b | 0.31 | | 0.51 |
| c | 0.17 | | 0.25 |
| D | 9.80 | 9.90 | 10.00 |
| E | 5.80 | 6.00 | 6.20 |
| E1 | 3.80 | 3.90 | 4.00 |
| e | | 1.27 | |
| h | 0.25 | | 0.50 |
| L | 0.40 | | 1.27 |
| k | 0 | | 8 |
| ccc | | | 0.10 |

## 5.2 SO-16N packing information

Figure 29. SO-16N reel 13”

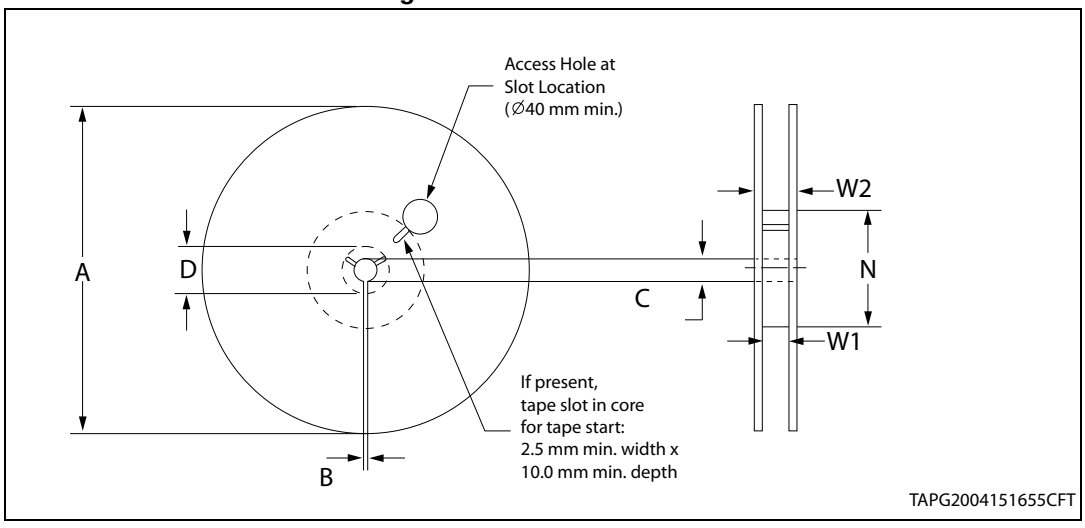


**Table 18. Reel dimensions**

| Description | Value(1) |
|---|---|
| Base quantity | 2500 |
| Bulk quantity | 2500 |
| A (max) | 330 |
| B (min) | 1.5 |
| C (+0.5, -0.2) | 13 |
| D (min) | 20.2 |
| N | 100 |
| W1 (+2 /-0) | 16.4 |
| W2 (max) | 22.4 |

1. All dimensions are in mm.

**Figure 30. SO-16N carrier tape**

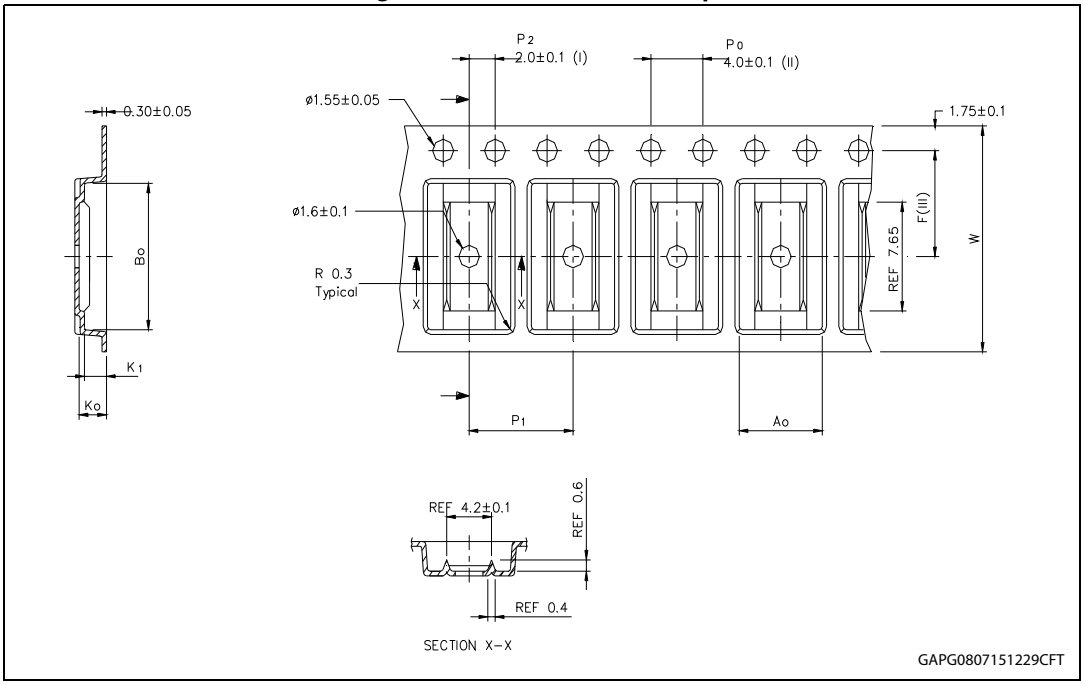


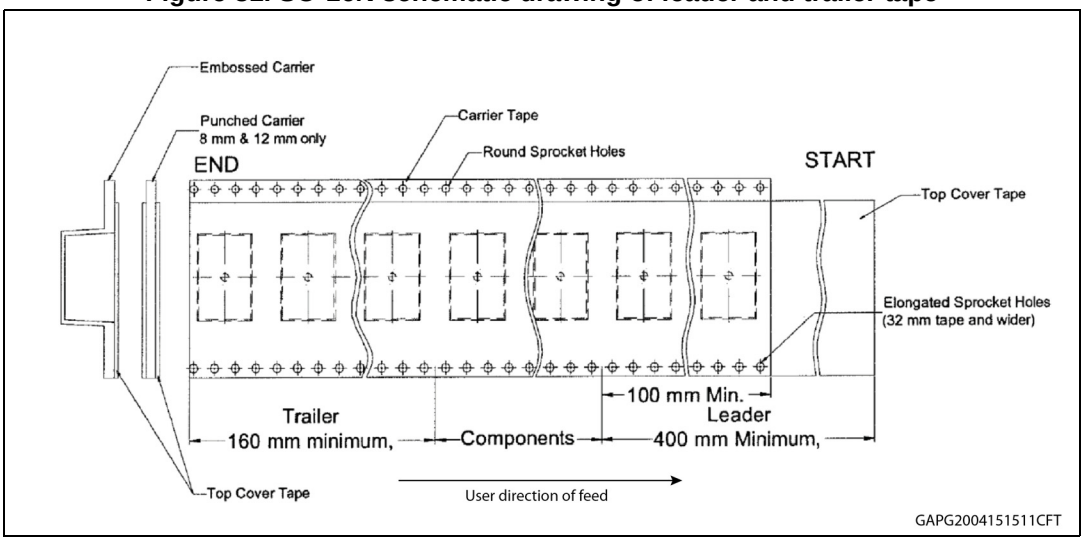

**Table 19. SO-16N carrier tape dimensions**

| Description | Value |
|---|---|
| $A_0$ | 6.55 ± 0.1 |
| $B_0$ | 10.38 ± 0.1 |
| $K_0$ | 2.10 ± 0.1 |
| $K_1$ | 1.80 ± 0.1 |
| F | 7.50 ± 0.1 |

**Table 19. SO-16N carrier tape dimensions (continued)**

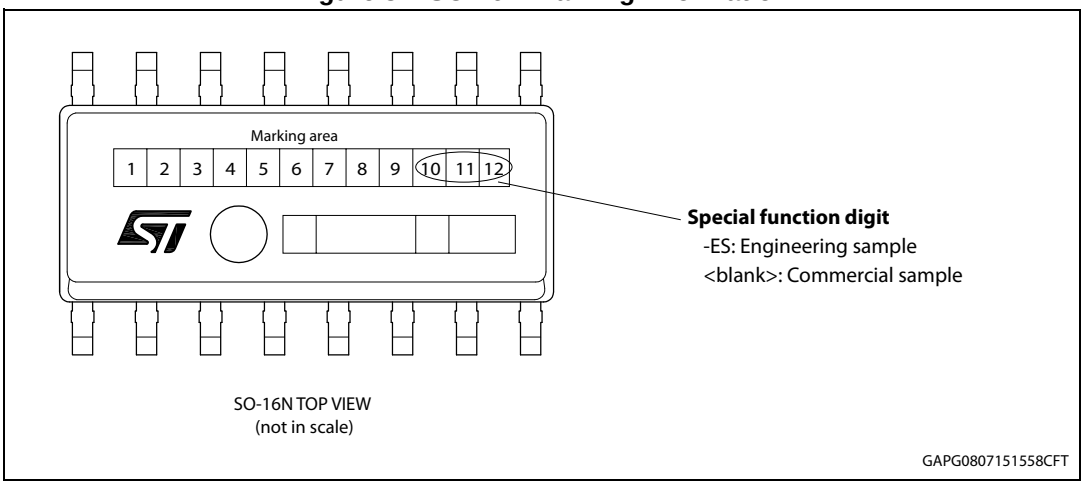
| Description | Value |
|---|---|
| $P_1$ | 8.00 ± 0.1 |
| W | 16.00 ± 0.3 |

**Figure 31. SO-16N schematic drawing of leader and trailer tape**




## 5.3 SO-16N marking information

**Figure 32. SO-16N marking information**




*Note: Engineering Samples: these samples can be clearly identified by a dedicated special symbol in the marking of each unit. These samples are intended to be used for electrical compatibility evaluation only; usage for any other purpose may be agreed only upon written authorization by ST. ST is not liable for any customer usage in production and/or in reliability qualification trials.*

*Commercial Samples: fully qualified parts from ST standard production with no usage restrictions.*

# 6 Revision history

**Table 20. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 16-Jul-2015 | 1 | Initial release. |
| 01-Sep-2015 | 2 | *Table 8: Switching (VCC = 13 V; RLOAD = 5.2 Ω)*:<br>– $t_{cross}$: updated values<br>*Table 9: Protections and diagnostics (VCC = 7 V up to 18 V; -40°C < Tj < 150°C)*:<br>– $I_{SD\_LS}$, $t_{DSTKON}$: updated values<br>*Table 10: CS (7 V < VCC < 18 V; -40 °C < Tj < 150 °C)*:<br>– $K_2$, $K_3$, $I_{SENSE\_SAT}$: updated values |
| 04-Sep-2015 | 3 | *Table 4: Absolute maximum ratings*:<br>– $I_R$: updated value |
| 07-Oct-2015 | 4 | *Table 4: Absolute maximum ratings*:<br>– $-I_{GND}$: removed row<br>Updated *Table 5: Thermal data*<br>*Table 6: Power section*:<br>– $V_f$: updated parameter<br>Updated *Figure 9: Input reset time for HSD - fault unlatch* and *Figure 10: Input reset time for LSD - fault unlatch*<br>Added *Section 2.4: Waveforms* and *Chapter 4: Package and PCB thermal data*<br>Updated *Chapter 3: Application information* |