# VNI8200XP

## Octal high side smart power solid state relay with serial/parallel selectable interface on chip

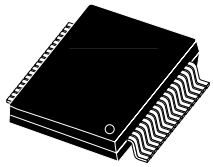
**Preliminary data**

## Features

| Type | $V_{demag}$ (1) | $R_{DS(on)}$ (1) | $I_{out}$ (1) | $V_{CC}$ |
|---|---|---|---|---|
| VNI8200XP | $V_{CC}$-45 V | 0.11 Ω | 0.7 A | 45 V |

1. Per channel

- Output current: 0.7 A per channel
- Serial/parallel selectable interface
- Short-circuit protection
- 8-bit and 16-bit SPI Interface for IC command and control diagnostic
- Channel over-temperature detection and protection
- Thermal independence of separate channels
- Drivers for all type of loads (resistive, capacitive, inductive load)
- Loss of GND protection
- Power Good diagnostic
- Undervoltage shutdown with hysteresis
- Overvoltage protection ($V_{CC}$ clamping)
- Very low supply current
- Common fault open drain output
- IC pre-warning temperature detection
- Channels output disable
- 100 mA high efficiency step-down switching regulator with integrated boot diode
- Adjustable regulator output
- Feed-back disconnection protection
- Switching regulator disable
- 5 V and 3.3 V compatible I/Os
- Channel outputs status LED driving 4 x 4 multiplexed array
- Fast demagnetization of inductive loads
- ESD protection
- Compliant with IEC 61131-2



**PowerSSO-36**

## Applications

- Programmable logic control
- Industrial PC peripheral input/output
- Numerical control machines

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# 1 Device description

The VNI8200XP is a monolithic 8 channel driver featuring a very low supply current, with integrated SPI interface and high efficiency 100 mA micro-power step-down switching regulator burst hysteresis control. The IC, realized in STMicroelectronics VIPower technology, is intended for driving any kind of load with one side connected to ground.

Active channel current limitation combined with thermal shutdown, independent for each channel, and automatic restart, protect the device against overload.

Additional embedded functions are: Loss of GND protection that automatically turns OFF the IC in case of ground pin disconnection, under voltage shutdown with hysteresis, Power Good diagnostic for valid supply voltage range recognition, output enable function for immediate power outputs shutdown and programmable watchdog function for micro controller safe operation; case over temperature protection to control the IC case temperature.

The device embedded a four wires SPI serial peripheral with selectable 8 or 16 bits operations; through a select pin the device can operate with parallel interface as well.

Both the 8 bits and 16 bits SPI operations are compatible with daisy chain connection.

The SPI Interface allows commanding the output driver by enabling or disabling each channel featuring in 16 bits format a parity check control for communication robustness. It also allows monitoring the status of the IC signaling Power Good, loss of ground, over-temperature condition for each channel, IC pre-warning temperature detection.

Built-in thermal shutdown protects the chip from over temperature and short circuit. In overload condition, channel turns OFF and back ON automatically after the IC temperatures decreased below a threshold fixed by a temperature hysteresis so that junction temperature is controlled. If this condition makes case temperature reaching case temperature limit, $T_{CSD}$ overloaded channels are turned OFF and will restart, non simultaneously, only when case temperature decreased down to $T_{CSD}$. Non overloaded channels continue to operate normally. Case temperature above $T_{CSD}$ is signalized through $\overline{TWARN}$ open drain pin.

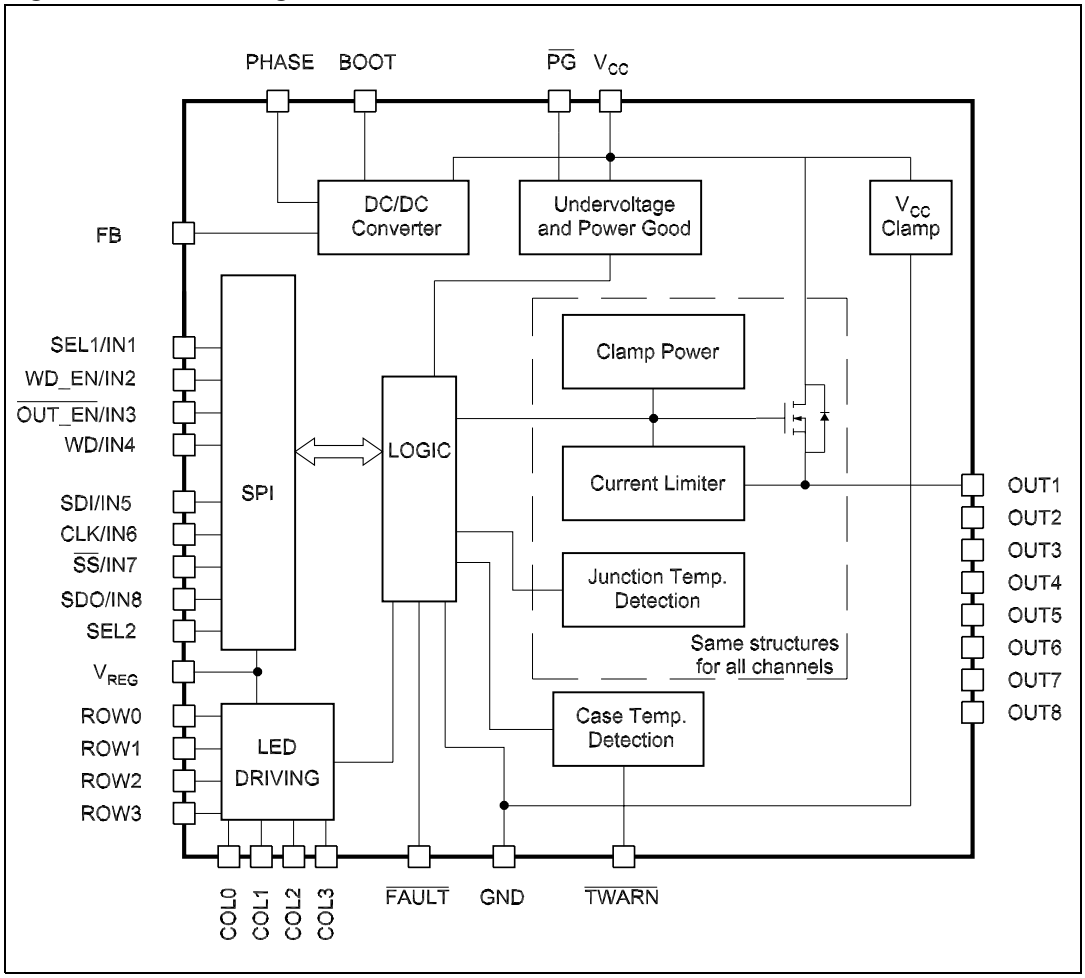
An internal circuit provides a not latched common $\overline{FAULT}$ indicator signaling if one of the following events occurs: channel OVT (over temperature) and parity check fail. While the Power Good diagnostic, $\overline{PG}$, warns the controller that the supply voltage is below a fixed threshold

The watch-dog function is used to detect the occurrence of a software fault of the host controller. The watchdog circuitry generates an internal reset on expiry of the internal Watch-dog timer. The watchdog timer reset can be achieved applying a negative pulse on WD pin. Watch-dog function can be disabled by WD_EN dedicated pin. This pin also allows programming a wide range of watch-dog timings.

An internal LED matrix block (4 rows, 4 columns) allows to detect status of the single outputs, and junction over temperature fault notification for each channel. An integrated step-down voltage regulator provides supply voltage to the internal LED driving outputs and logic output circuit and to the external optocoupler if the application requires isolation. The regulator is protected against short circuit or overload condition. Pulse by pulse current limit with burst hysteretic control offers an effective constant current limiting.

# 2 Block diagram

**Figure 1. Block diagram**



# 3 Pin connection

**Figure 2. Pin connection (top view)**

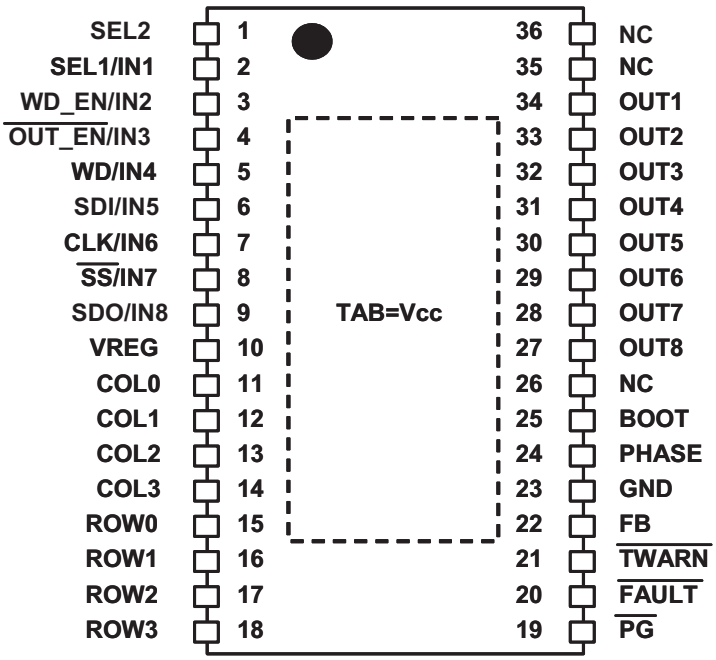



**Table 2. Pin description**

| Pin | Name | Type | Description |
|---|---|---|---|
| 1 | SEL2 | Logic/analog input | SPI/parallel selection mode |
| 2 | SEL1/IN1 | Logic/analog input | 8/16 bits SPI selection mode/channel 1 input |
| 3 | WD_EN/ IN2 | Analog input | Watch-dog enable_setting/channel 2 input |
| 4 | $\overline{\text{OUT\_EN}}$ /IN3 | Logic/analog input | Output enable_disable/channel 3 input, disable is active low. |
| 5 | WD/IN4 | Logic/analog input | Watchdog input. The internal watchdog counter cleared on the falling edges/channel 4 input |
| 6 | SDI/IN5 | Logic/analog input | Serial data input/channel 5 input |
| 7 | CLK/IN6 | Logic/analog input | Serial clock/channel 6 input |
| 8 | $\overline{\text{SS}}$/IN7 | Logic/analog input | Slave select/channel 7 input |
| 9 | SDO/IN8 | Logic/analog input | Serial data output/channel 8 input |
| 10 | VREG | Power supply | Stepdown regulated voltage |
| 11 | COL0 | Open source output | LED source output |
| 12 | COL1 | Open source output | LED source output |
| 13 | COL2 | Open source output | LED source output |
| 14 | COL3 | Open source output | LED source output |

Table 2. Pin description (continued)

| Pin | Name | Type | Description |
|---|---|---|---|
| 15 | ROW0 | Open drain output | Row LED 0-3 |
| 16 | ROW1 | Open drain output | Row LED 4-7 |
| 17 | ROW2 | Open drain output | Row LED 8-11 |
| 18 | ROW3 | Open drain output | Row LED 12-15 |
| 19 | $\overline{PG}$ | Open drain output | Power Good diagnostic -active low |
| 20 | $\overline{FAULT}$ | Open drain output | Fault indication - active low |
| 21 | $\overline{TWARN}$ | Open drain output | IC pre-warning temperature detection - active low |
| 22 | FB | Analog input | Step-down feedback input. Connecting the output voltage directly to this pin results in an output voltage of 3.3 V. An external resistor divider is required for higher output voltages (the typical value for the resistor connected between this pin and ground is 47 kΩ). |
| 23 | GND | | Ground |
| 24 | PHASE | Power output | Stepdown output |
| 25 | BOOT | Power output | Stepdown bootstrap voltage. Used to provide a drive voltage, higher than the supply voltage, to power the switch of the step-down regulator |
| 26 | NC | | Not connected |
| 27 | OUT8 | Power output | Channel 8 power output |
| 28 | OUT7 | Power output | Channel 7 power output |
| 29 | OUT6 | Power output | Channel 6 power output |
| 30 | OUT5 | Power output | Channel 5 power output |
| 31 | OUT4 | Power output | Channel 4 power output |
| 32 | OUT3 | Power output | Channel 3 power output |
| 33 | OUT2 | Power output | Channel 2 power output |
| 34 | OUT1 | Power output | Channel 1 power output |
| 35 | NC | | Not connected |
| 36 | NC | | Not connected |
| TAB | TAB | Power supply | Exposed tab internally connected to $V_{CC}$ |

## 3.1 Maximum ratings

**Table 3. Absolute maximum rating**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | Power supply voltage | 45 | V |
| $-V_{CC}$ | Reverse supply voltage | -0.3 | V |
| $I_{GND}$ | DC ground reverse current | -250 | mA |
| $I_{OUT}$ | Output current (continuous) | Internally limited | A |
| $I_R$ | Reverse output current (per channel) | -5 | A |
| $V_{REG}$ | Logic supply voltage | -0.3 to +6 | V |
| $-I_{REG}$ | Reverse input current | -10 | mA |
| $V_{FAULT}$ $V_{TWARN}$ $V_{PG}$ | Voltage range at pins $\overline{TWARN}$, $\overline{FAULT}$, $\overline{PG}$ | -0.3 to +6 | V |
| $I_{FAULT}$ $I_{TWARN,}$ $I_{PG}$ | Current range at pins $\overline{TWARN}$, $\overline{FAULT}$, $\overline{PG}$ | ± 10 | mA |
| $V_{BOOT}$ | Bootstrap peak voltage $V_{PHASE}$ = Vcc | $V_{CC}$+10 | V |
| $V_{ROW}$ | Voltage range at $ROW_i$ pins | -0.3 to +6 | V |
| $V_{COL}$ | Voltage range at $COL_i$ pins | -0.3 to +6 | V |
| $I_{ROW}$ | Current range at $ROW_i$ pins | ±40 | mA |
| $I_{COL}$ | Current range at $COL_i$ pins | ±10 | mA |
| $V_{ESD}$ | Electrostatic discharge (R = 1.5 kΩ; C = 100 pF) | 2000 | V |
| $V_{dig}$ | Voltage level range at logic inputs pins | -0.3 to +6 | V |
| $E_{AS}$ | Single pulse avalanche energy per channel not simultaneously | 300 | mJ |
| $P_{TOT}$ | Power dissipation at $T_c$ = 25 °C | Internally limited | W |
| $T_J$ | Junction operating temperature | Internally limited | °C |
| $T_{STG}$ | Storage temperature | -55 to 150 | °C |

## 3.2 Thermal data

**Table 4. Thermal data**

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $R_{th(JC)}$ | Thermal resistance junction-case (1) | Max | 2 | °C/W |
| $R_{th(JA)}$ | Thermal resistance junction-ambient (2) | Max | 52 | °C/W |

1. Per channel
2. When mounted using minimum recommended pad size on FR-4 board (for details refer to *Chapter 10 on page 22*)

# 4 Electrical characteristics

10.5 V < $V_{CC}$ < 36 V; -40 °C < $T_J$ < 125 °C; unless otherwise specified.

**Table 5. Power section**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Vcc | Supply voltage | | 10.5 | | 36 | V |
| $R_{DS(ON)}$ | On state resistance | $I_{OUT}$ = 0.5 A at $T_J$ = 25 °C<br>$I_{OUT}$ = 0.5 A | | | 0.110<br>0.200 | Ω<br>Ω |
| $I_S$ | Supply current | All channel in OFF state, SPI OFF. (1)<br>ON state and SPI ON (2) ($T_J$ = 125 °C) | | 250<br>4.8 | <br>TBD | µA<br>mA |
| $I_{LGND}$ | Output current at turn-off | $V_{CC}$ = $V_{STAT}$ = $V_{IN}$ = $V_{GND}$ = 24 V, $V_{OUT}$ = 0 V | | | 1 | mA |
| $V_{OUT(OFF)}$ | OFF state output voltage | $V_{IN}$ = 0 V, and $I_{OUT}$ = 0 A | | | 3 | V |
| $I_{OUT(OFF)}$ | OFF state output current | $V_{IN}$ = $V_{OUT}$ = 0 V | 0 | | 5 | µA |
| $F_{CP}$ | Charge pump frequency | Channel in ON state (3) | | 1.45 | | MHz |

1. $\overline{SS}$ signal high, NO communication
2. $\overline{SS}$ signal low, communication ON
3. To cover EN55022 class A and class B normative

**Table 6. SPI characteristics**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $f_{CLK}$ | SPI clock frequency | | | - | 5 | MHz |
| $t_r$(CLK), $t_f$(CLK) | SPI clock rise/fall time | | | - | 20 | ns |
| $t_{su}(\overline{SS})$ | $\overline{SS}$ setup time | | 120 | - | | ns |
| $t_h(\overline{SS})$ | $\overline{SS}$ hold time | | 120 | - | | ns |
| $t_w$(CLK) | CLK high time | | 80 | - | | ns |
| $t_{su}$(SDI) | Data input setup time | | 100 | - | | ns |
| $t_h$(SDI) | Data input hold time | | 100 | - | | ns |
| $t_a$(SDO) | Data output access time | | | - | 100 | ns |
| $t_{dis}$(SDO) | Data output disable time | | | - | 200 | ns |
| $t_v$(SDO) | Data output valid time | | | - | 100 | ns |
| $t_h$(SDO) | Data output hold time | | 0 | - | | ns |
| $V_{SDO}$ | Voltage on serial data output | $I_{SDO}$ = 15 mA | | - | Vreg-0.8 | V |
| | | $I_{SDO}$ = -2 mA | | - | 0.8 | V |

$V_{CC}$ = 24 V; -40 °C < $T_J$ < 125 °C

**Table 7. Switching**

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(ON)}$ | Turn ON delay time of output current | $I_{OUT}$ = 0.5 A, resistive load, input rise time < 0.1 µs | - | 50 | - | µs |
| $t_r$ | Rise time of output Current | $I_{OUT}$ = 0.5 A, resistive load, input rise time < 0.1 µs | - | 50 | - | µs |
| $t_{d(OFF)}$ | Turn OFF delay time of output current | $I_{OUT}$ = 0.5 A, resistive load, input rise time < 0.1 µs | - | 34 | - | µs |
| $t_f$ | Fall time of output current | $I_{OUT}$ = 0.5 A, resistive load, input rise time < 0.1 µs | - | 8 | - | µs |
| $dV/dt_{(ON)}$ | Turn ON voltage slope | $I_{OUT}$ = 0.5 A, resistive load, input rise time < 0.1 µs | - | 0.7 | - | V/µs |
| dV/dt(off) | Turn OFF voltage slope | $I_{OUT}$ = 0.5 A, resistive load, input rise time < 0.1 µs | - | 1.5 | - | V/µs |

**Table 8. Logical input**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input low level voltage | | | | 0.8 | V |
| $V_{IH}$ | Input high level voltage | | 2.20 | | | V |
| $V_{I(HYST)}$ | Input hysteresis voltage | | | 0.15 | | V |
| $I_{IN}$ | Input current | $V_{IN}$ = 5 V | 10 | | | µA |

**Table 9. Protection and diagnostic**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{FAULT}$ | $\overline{FAULT}$ pin open drain voltage output low | $I_{FAULT}$ = 1.6 mA (fault condition) | | | 0.6 | V |
| $V_{TWARN}$ | $\overline{TWARN}$ pin open drain voltage output low | $I_{TWARN}$ = 1.6 mA (active condition) | | | 0.6 | V |
| $V_{PG}$ | $\overline{PG}$ pin open drain voltage output low | $I_{PG}$ = 1.6 mA (active condition) | | | 0.6 | V |
| $I_{LFAULT}$ | $\overline{FAULT}$ leakage current | $V_{pin}$ = 5 V | | 2 | | µA |
| $I_{TWARN}$ | $\overline{TWARN}$ leakage current | | | | | |
| $I_{PG}$ | $\overline{PG}$ leakage current | | | | | |
| $V_{pgH1}$ | Power Good diagnostic ON threshold | -40 °C < $T_J$ < 125 °C | 16.6 | 17.5 | 18.4 | V |
| $V_{pgH2}$ | Power Good diagnostic OFF threshold | | 15.6 | 16.5 | 17.4 | |
| $V_{pgHYS}$ | Power Good diagnostic hysteresis | | TBD | | | |
| $V_{USD}$ | Undervoltage protection | | | 9.5 | 10.5 | V |
| $V_{USDHYS}$ | Undervoltage hysteresis | | 0.4 | 0.5 | | V |
| $T_{TSD}$ | Junction shutdown temperature | | 150 | 170 | 190 | °C |
| $T_R$ | Junction reset temperature | | 135 | | | °C |
| $T_{HIST}$ | Junction thermal hysteresis | | 7 | 15 | | °C |
| $I_{PEAK}$ | Maximum DC output current(1) | | | 1.4 | | A |
| $I_{LIM}$ | Short circuit current limitation per channel | $R_{LOAD}$ = 0 | 0.7 | 1.1 | 1.7 | A |
| Hyst | $I_{LIM}$ tracking limits | $R_{LOAD}$ = 0 | | 0.3 | | A |
| $T_{CSD}$ | Case shutdown temperature | | 115 | 130 | 145 | °C |
| $T_{CR}$ | Case reset temperature | | | 110 | | °C |
| $T_{CHYST}$ | Case thermal hysteresis | | | 20 | | °C |
| $V_{demag}$ | Output voltage at turn-OFF | $I_{OUT}$ = 0.5 A; $L_{LOAD} \geq$ 1 mH | $V_{CC}$-45 | $V_{CC}$-50 | $V_{CC}$-52 | V |
| $t_{WD}$ | Watchdog hold time | See *Figure 16* | 50 | | | ns |
| $t_{WM}$ | Watchdog time | See *Table 13* and *Figure 16* | | | | |
| $t_{WO}$ | Watchdog time-out(2) | | | | $t_{WM}$ + $t_{d(off)}$ | ms |

**Table 9. Protection and diagnostic (continued)**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{OUT\_EN}$ | $\overline{OUT\_EN}$ pin propagation delay(3) | | | | $t_{d(off)}$ | ms |
| $t_{res}$ | $\overline{OUT\_EN}$ hold time | | 50 | | | ns |

1. Current level from open load to short circuit until thermal protection intervention
2. The time from $t_{WM}$ elapsed to power out disable
3. Time from reset active low and power out disable

10.5 V < Vcc < 36 V; -40 °C < $T_J$ < 125 °C; unless otherwise specified

**Table 10. Step-down switching regulator**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{REG}$ | Regulated output voltage | Ireg from 0 to 100 mA<br>Vreg 3.3 V, *Figure 7.* | 3.135 | 3.3 | 3.465 | V |
| | | Ireg from 0 to 100 mA<br>Vreg 5 V, *Figure 8.* | | 5 | | |
| $I_{REG}$ | Regulator output current | | | | 100 | mA |
| $R_{DSON}$ | MOSFET on resistance | | | 1.5 | | Ω |
| $I_{PEAK}$ | Maximum peak current | | | 1 | | A |
| $f_s$ | Switching frequency | | | 100 | | kHz |
| $D_{max}$ | Maximum duty cycle | | | TBD | | % |
| $D_{min}$ | Minimum duty cycle | | | TBD | | % |
| $V_{FB}$ | Voltage feedback | | 3.135 | 3.3 | 3.465 | V |
| $I_{FB}$ | Feedback current | $V_{FB}$ = 3.3 V | | 10 | | µA |
| $I_{qop}$ | Total operating quiescent current | | | 1 | | mA |
| $I_{qst\text{-}by}$ | Total stand-by quiescent current | Regulator stand-by | | TBD | | µA |
| $I_{BOOTleak}$ | Bootstrap reverse leakage current | | | | 2 | µA |

10.5 V < Vcc < 36 V; -40 °C < $T_J$ < 125 °C; unless otherwise specified

**Table 11. LED driving array**

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{COL}$ | Output source voltage at COL pins output peak current ranging from 0 to 7 mA | Vreg-0.3 | Vreg-0.2 | | V |
| Vrow | Open drain voltage at row pins output peak current ranging from 0 to 30 mA | | 0.2 | 0.3 | V |
| Fsw | Switching frequency | | 1 | | kHz |

# 5 Functional pin description

## 5.1 SPI/parallel selection mode (SEL2)

This pin allows selecting the IC interfacing mode. SPI interface is selected if SEL2 = H while Parallel interface is selected if SEL2 = L according to the following table:

**Table 12. Pin description**

| Pin | Function | | | |
|---|---|---|---|---|
| | if SEL2 = H SPI operation | | SEL2 = L Parallel operation | |
| SDO/IN8 | SDO | Serial data output | IN8 | Input to channel 8 |
| $\overline{SS}$/IN7 | $\overline{SS}$ | Slave select | IN7 | Input to channel 7 |
| CLK/IN6 | CLK | Serial clock | IN6 | Input to channel 6 |
| SDI/IN5 | SDI | Serial data input | IN5 | Input to channel 5 |
| WD/IN4 | WD | Watchdog input | IN4 | Input to channel 4 |
| $\overline{OUT\_EN}$/IN3 | $\overline{OUT\_EN}$ | IC OUTPUT enable / disable | IN3 | Input to channel 3 |
| WD_EN/IN2 | WD_EN | Watch-dog enable / disable and timing preset | IN2 | Input to channel 2 |
| SEL1/IN1 | SEL1 | 8/16 bits SPI selection mode | IN1 | Input to channel 1 |

## 5.2 Serial data in (SDI)

If SEL2 = H this pin is the input of the serial command frame. SDI is read on CLK rising edges and, thus, microcontroller must change SDI state during the CLK falling edges.

## 5.3 Serial data out (SDO)

If SEL2 = H this pin is the output of the serial fault frame. SDO is updated on CLK falling edges and, thus, microcontroller must read SDO state during the CLK rising edges.

SDO pin is tri-stated when $\overline{SS}$ signal is high.

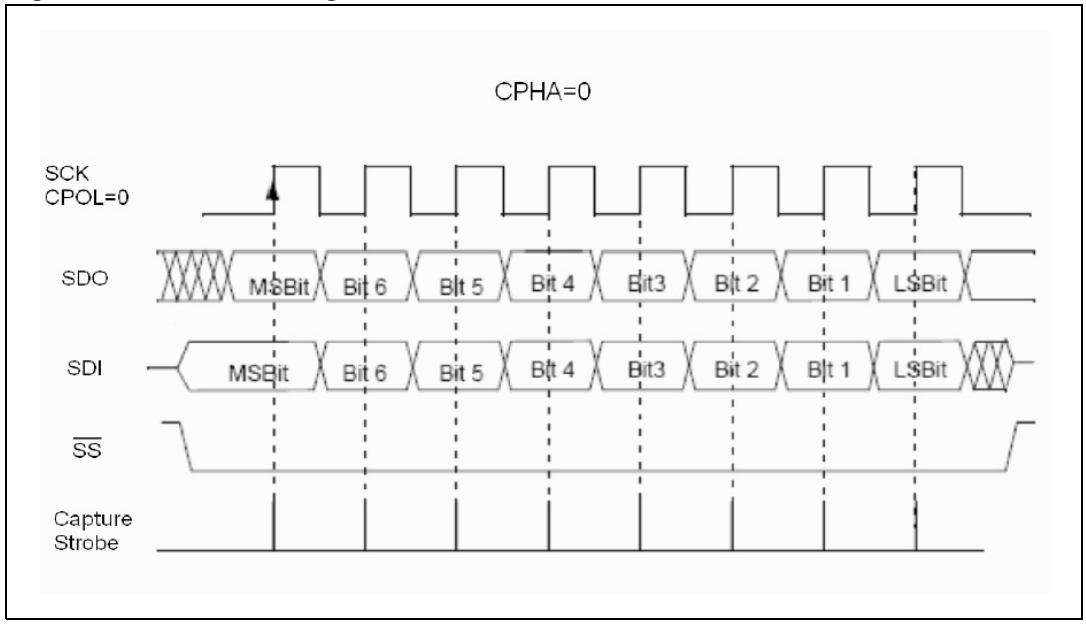
## 5.4 Serial data clock (CLK)

If SEL2 = H the CLK line is the input clock for serial data sampling. SDO is updated on CLK falling edges, and then it must be sampled on the rising edge, and the SDI line is sampled on CLK rising edges. When the $\overline{SS}$ signal is high, slave not selected, the micro controller should drive the CLK low (settings for MCU SPI port are CPHA = 0 and CPOL = 0).

## 5.5 Slave select ($\overline{SS}$)

If SEL2 = H slave select ($\overline{SS}$) signal is used to enable the VNI8200XP serial communication shift register, data is flushed in through the SDI pin and out from SDO pin only when $\overline{SS}$ pin is low. On the $\overline{SS}$ pin falling edge the shift register (containing switch fault conditions) is frizzed, so any change on the switch status will be latched until the next $\overline{SS}$ falling edge event. On the $\overline{SS}$ pin rising edge event the 8/16 bits present on the SPI shift register are evaluated and the outputs are driven accordingly to this frame. If more than 8/16 bits (depending on the SPI settings) are flushed into the switch only last 8/16 are evaluated, the others are flushed out from the SDO pin after fault condition bits; in this way a proper communication is granted also in a daisy chain configuration.

**Figure 3. SPI mode diagram**




## 5.6 8/16 bits selection (SEL1)

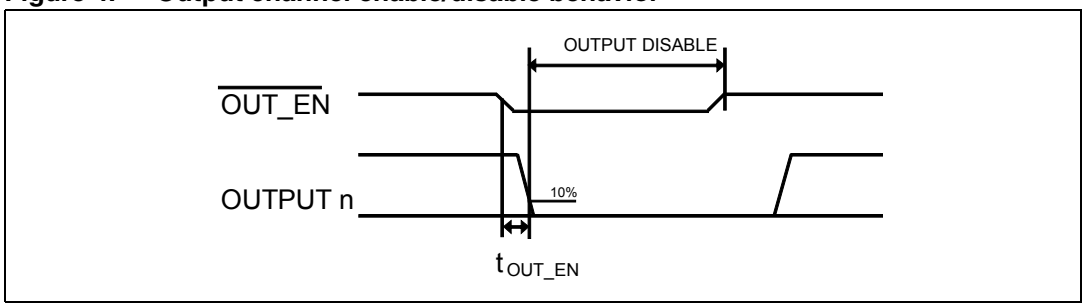
If SEL2 = H SEL1 is used to select among two possible SPI configurations: the 8 bit SPI mode (SEL1 = L) and the 16 bit SPI node (SEL1 = H). 8/16 bit SPI operation is described below.

## 5.7 Output enable / disable ($\overline{OUT\_EN}$)

If SEL2 = H this pin provides a fast way to disable all the outputs simultaneously, useful in case of a fault condition. When the $\overline{OUT\_EN}$ pin is driven low for at least $T_{RES}$ the outputs are disabled while fault conditions in the SPI register are latched. To enable the outputs is then necessary to raise the $\overline{OUT\_EN}$ pin and re-program the IC through the SPI interface. Since fault conditions are latched inside the IC and SPI interface is working also while $\overline{OUT\_EN}$ pin is driven low, it's possible to use SPI to detect which fault condition occurred before the reset event. This timing execution is compatible with an external reset push from operator, safety requirement, and permits a microcontroller, or generic government unit, polling all internal information during a reset procedure.

The device is ready to normally operate after a $T_{SU}$ period. The $\overline{OUT\_EN}$ pin is the fastest way to disable all the output when a fault occurs.

**Figure 4. Output channel enable/disable behavior**




## 5.8 IC pre-warning temperature detection ($\overline{TWARN}$)

The $\overline{TWARN}$ pin is an active low open drain output. This pin is activated if the IC case temperature exceeds $T_{CSD}$. According to the PCB thermal design and $R_{thJC}$ value, this function allows to warn about a PCB overheating condition.

$\overline{TWARN}$ bit is also available through SPI. This bit is not latched: $\overline{TWARN}$ pin is low only when the case over temperature is active ($T_C > T_{CSD}$) and it's released when this condition has been removed ($T_C < T_{CR}$).

## 5.9 Fault indication ($\overline{FAULT}$)

The $\overline{FAULT}$ pin is an open drain active low fault indication pin. This pin is activated by one or more of the following conditions:

- **Channel over-temperature (OVT)**

  This pin is activated when at least one of the channels is in junction over temperature.

  Unlike the SPI fault detection bits this signal is not latched: the $\overline{FAULT}$ pin is low only when the fault condition is active and it's released after this condition has been removed, which happens if the channel temperature decreases below the intervention level and the case temperature has not exceeded TCSD or is below TCR.

  This means that the $\overline{FAULT}$ pin is low only when the junction over temperature is active ($T_J > T_{TSD}$) and it's released after this condition has been removed ($T_J < T_R$ and $T_C < T_{CR}$).

- **Parity check fail**

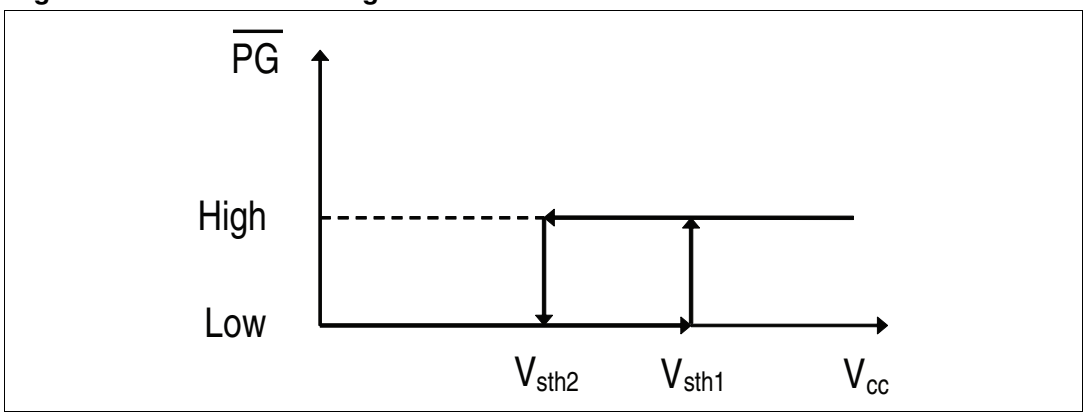
  When SPI mode is used (SEL2 = H), if a Parity check fault of the incoming SPI frame is detected or counted CLK rising edges are different than a multiple of 8 the $\overline{FAULT}$ pin is kept low. When counted CLK rising edges are multiple of 8 and parity check is valid the $\overline{FAULT}$ pin is kept high.

## 5.10 Power Good ($\overline{PG}$)

The $\overline{PG}$ terminal is an open drain, active low output that indicates the status of supply voltage. When $V_{CC}$ supply voltage reaches Vsth1 threshold. $\overline{PG}$ will go to a high-impedance state. It will go to a low-impedance state when $V_{CC}$ falls below Vsth2 threshold.

In 16 bit SPI mode a $\overline{PG}$ bit is also provided. This bit is set to one when the Power Good diagnostic is active, cleared otherwise.

**Figure 5. Power Good diagnostic**



## 5.11 Programmable watchdog counter reset (WD)

If SEL2 = H the VNI8200XP embeds a watchdog counter that must be erased, with a negative pulse on the WD pin, before it expires. If the WD counter elapses the VNI8200XP goes into an internal RESET state where all the output are disabled; to restart the normal operation a negative pulse must be applied at the WD pin.

The watchdog enable/disable pin should be connected through an external divider to Vreg. The watchdog time is fixed following the table below:

**Table 13. Programmable watchdog time**

| $V_{WD\_EN}$ | $t_{WM}$ |
|---|---|
| 0.25 Vreg > $V_{WD\_EN}$ | Disable |
| 0.25 Vreg ≤ $V_{WD\_EN}$ < 0.5 Vreg | 42 ± 10 % ms |
| 0.5 Vreg ≤ $V_{WD\_EN}$ < 0.75 Vreg | 84 ± 10 % ms |
| 0.75 Vreg ≤ $V_{WD\_EN}$ = Vreg | 170 ± 10 % ms |

# 6 SPI operation (SEL2 = H)

## 6.1 8 bit SPI mode (SEL1 = L)

If SEL2 = H the 8 bit SPI mode is based on a 8 bit command frame sent from the microcontroller to the IC; each bit directly drives the corresponding output where LSB drives output 0 and MSB drives output 7. Each bit set to ‘1’ activates (closes) the corresponding output.

At the same time the IC transfers the channel fault conditions (OVT) to the microcontroller. These fault conditions are latched at the occurrence and cleared after each communication (each time the $\overline{SS}$ signal has a positive transition). Each bit set to ‘1’ indicates an OVT condition for the corresponding channel.

Command 8 bit frame (master to slave):

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| IN7 | IN6 | IN5 | IN4 | IN3 | IN2 | IN1 | IN0 |

Fault 8 bit frame (slave to master):

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| S7 | S6 | S5 | S4 | S3 | S2 | S1 | S0 |

## 6.2 16 bit SPI mode (SEL1 = H)

The 16 bit SPI mode is based on a 16 bit command frame sent from the microcontroller to the IC; the first 8 bits directly drive the output channels (each bit set to '1' activates the corresponding output), the other 8 bits contain a 4 bit parity check code where the last bit (the inversion of the previous one) is used to detect a communication error condition (providing at least a transition in each frame):

P0 = IN0 ⊕ IN1 ⊕ IN2 ⊕ IN3 ⊕ IN4 ⊕ IN5 ⊕ IN6 ⊕ IN7

P1 = IN1 ⊕ IN3 ⊕ IN5 ⊕ IN7

P2 = IN0 ⊕ IN2 ⊕ IN4 ⊕ IN6

nP0 = NOT P0

Command 16 bit frame (master to slave):

| MSB | | | | | | | | | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| IN7 | IN6 | IN5 | IN4 | IN3 | IN2 | IN1 | IN0 | - | - | - | - | P2 | P1 | P0 | nP0 |

At the same time the IC transfers to the microcontroller a 16 bit fault frame where the first 8 bits indicate a channel fault (OVT) condition (each bit set to '1' indicates an OVT event), the following 4 bits provide general fault condition information: REG_OK (if the Step-down regulated voltage is OK this bit is '1'), $\overline{\text{TWARN}}$ (IC pre-warning temperature, see *Section 5.8*), $\overline{\text{PC}}$ (Parity check fail, the pin set to '1' indicates an $\overline{\text{PC}}$ fail or the length is not a multiple of 8 bit frame) and $\overline{\text{PG}}$ (Power Good, see *Section 5.10*), while the last 4 bits are used as parity check bits and communication error condition (see command 16 bit frame):

P0 = S0 ⊕ S1 ⊕ S2 ⊕ S3 ⊕ S4 ⊕ S5 ⊕ S6 ⊕ S7

P1 = $\overline{\text{PC}}$ ⊕ REG_OK ⊕ S1 ⊕ S3 ⊕ S5 ⊕ S7

P2 = $\overline{\text{PG}}$ ⊕ $\overline{\text{TWARN}}$ ⊕ S0 ⊕ S2 ⊕ S4 ⊕ S6

nP0 = NOT P0

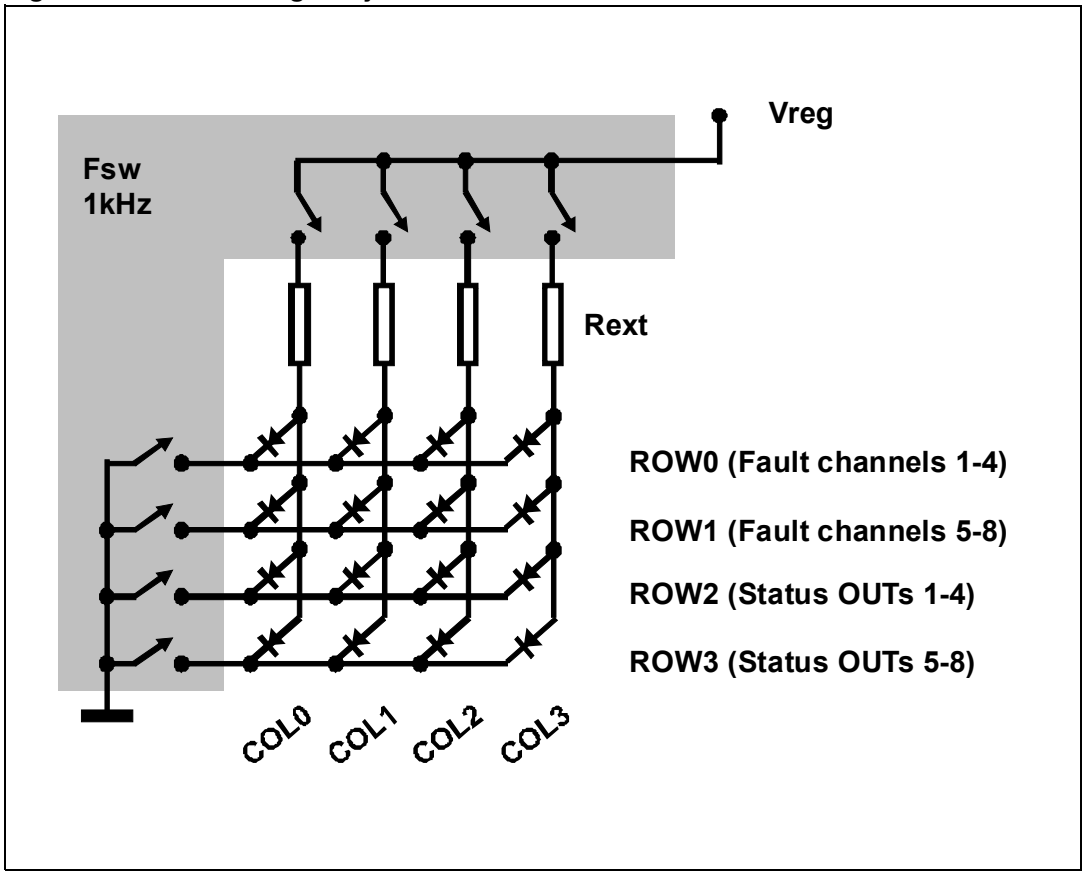
Fault 16 bit frame (master to slave):

| MSB | | | | | | | | | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| S7 | S6 | S5 | S4 | S3 | S2 | S1 | S0 | REG_ OK | $\overline{\text{TWARN}}$ | $\overline{\text{PC}}$ | $\overline{\text{PG}}$ | P2 | P1 | P0 | nP0 |

Channels indication are latched and cleared only after a communication.

# 7 LED driving array

**Figure 6. LED driving array**




The following is an indication on how to dimension the $R_{ext}$ resistors.

$$Rext = \frac{(V_{COL}\,min) - (V_{ROW}\,max) - V_{F(LED)}}{I_{F(LED)}}$$

*Note:* $I_{F(LED)} \leq 7\ mA$

Where ($V_{COL}$ min) and ($V_{ROW}$ max) can be found in the *Table 11* and $V_{F(LED)}$ and $I_{F(LED)}$ depend on the electrical characteristics of the LED.

# 8 Step-down switching regulator

The IC embeds a high efficiency 100 mA micro-power step-down switching regulator with burst hysteretic control. The regulator is protected against short circuit or overload conditions. Pulse by pulse current limit with burst hysteretic control and the regulation is obtained, in normal operation, trough a current loop control that limits the current always at the same value, about 1.4 A. A low ESR output capacitor connected on Vreg helps to limit the regulated voltage ripple; a low ESR (less than 10 mΩ) capacitor is preferable. The regulator is designed to properly work in discontinuous mode. The control loop pin FB allows to regulate 3.3 V connecting it directly to Vreg (see *Figure 8*), or 5 V connecting it trough a voltage divider R1/R2 (see *Figure 9*). It is possible to exclude the DC/DC converter block disconnecting the feedback pin; in this case an internal pull up will make the voltage on it to rise enough turning off the regulator. In some applications it is possible to supply a 5 V or 3.3 V voltage externally or, in the case of two or more VNI8200XP inside the same board, it's possible to configure the DC/DC converter on only one and supply also the other ICs. The following table shows typical values for the inductor and the capacitor.

**Table 14. Step-down switching regulator**

| | 18 V | | 24 V | | 36 V | |
|---|---|---|---|---|---|---|
| **Out voltage** | **Inductor** | **Capacitor** | **Inductor** | **Capacitor** | **Inductor** | **Capacitor** |
| 3.3V | 10 µH | 100 µF | 15 µH | 100 µF | 15 µH | 100 µF |
| 5V | 15 µH | 47µF | 22 µH | 47 µF | 22 µH | 47µF |

# 9 Conventions

**Figure 7. Supply voltage and power output conventions with Vreg = 3.3 V**

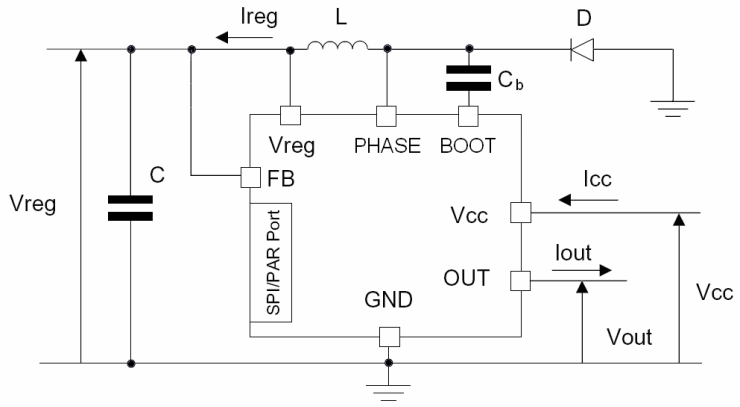



**Figure 8. Schematic with Vreg = 5 V ± 5 % using ideal resistors**

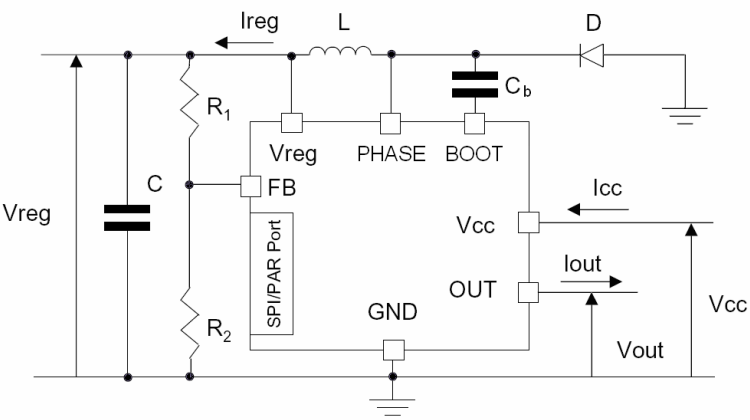
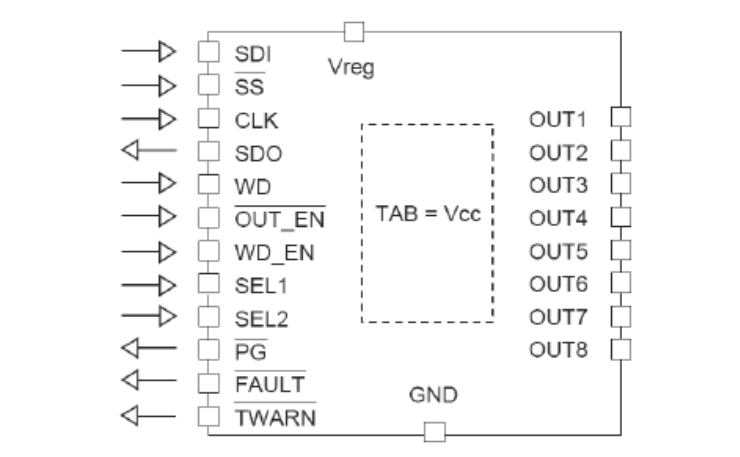


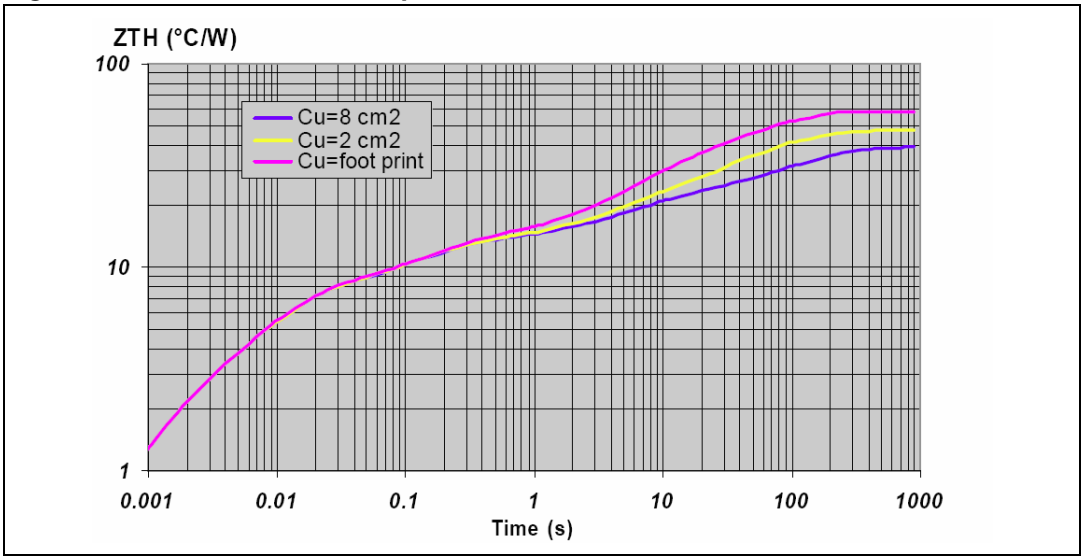

**Figure 9. SPI directional logic convention**



# 10 Thermal management

The power dissipation in the IC is the main factor that sets the safe operating condition of the device in the application. Therefore, it has to be taken into account very carefully. Besides the available space on the PCB should be chosen considering the power dissipation. Heat sinking can be achieved using copper on the PCB with proper area and thickness. The following picture (*Figure 10*) shows the junction to-ambient thermal Impedance values for the PSSO36 package.

**Figure 10. PSSO36 thermal impedance versus time**

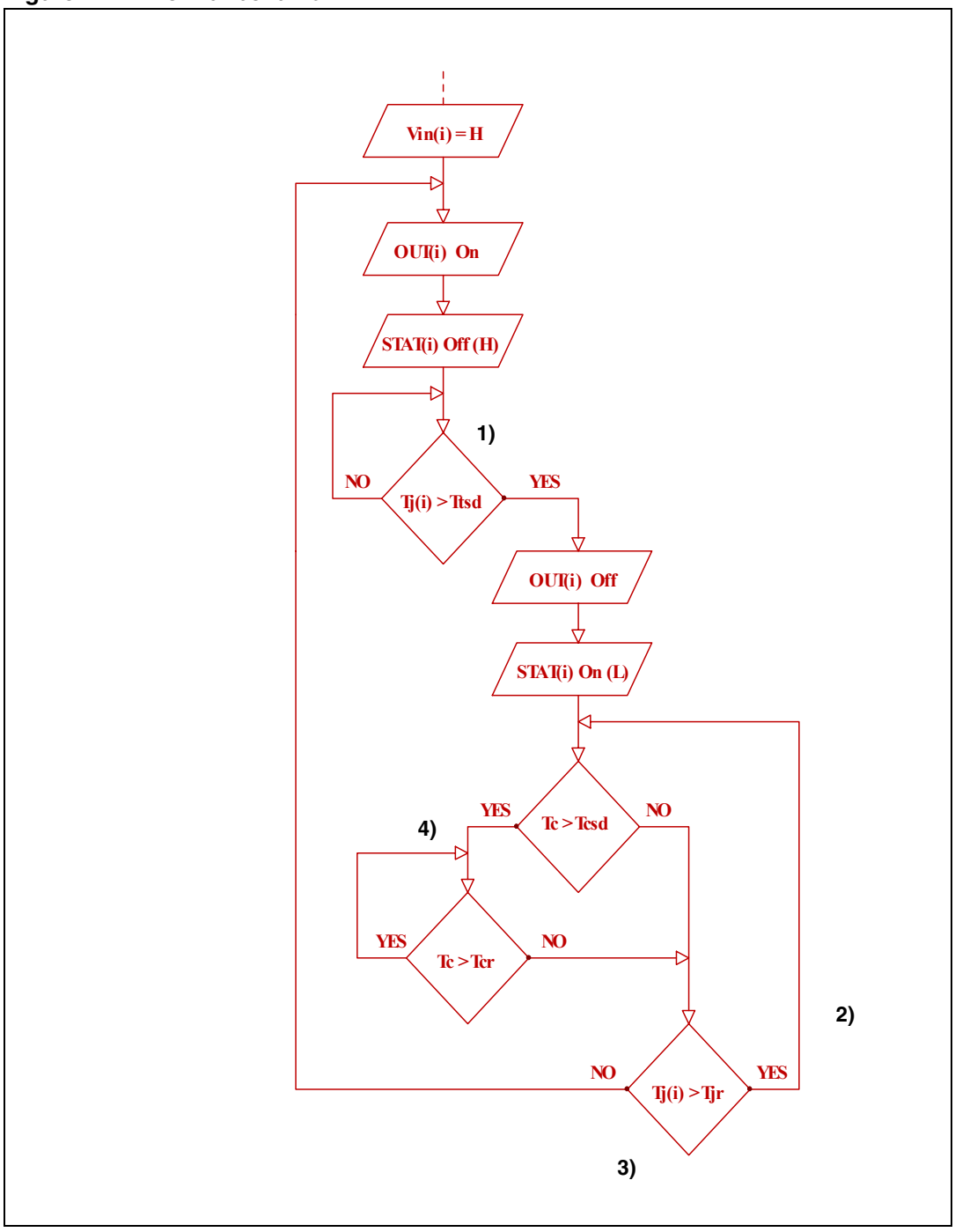



For instance, three cases have been considered using a PSSO36 packaged with copper slug soldered on a 1.6 mm thickness FR4 board with dissipating footprint (copper thickness of 70 µm):

- single layer PCB with just IC footprint dissipating area
- double layer PCB with footprint dissipating area on the top side and a 2 $cm^2$ dissipating layer on the bottom side through 15 via holes.
- double layer PCB with footprint dissipating area on the top side and a 8 $cm^2$ dissipating layer on the bottom side through 15 via holes.

## 10.1 Thermal behavior

**Figure 11. Thermal behavior**

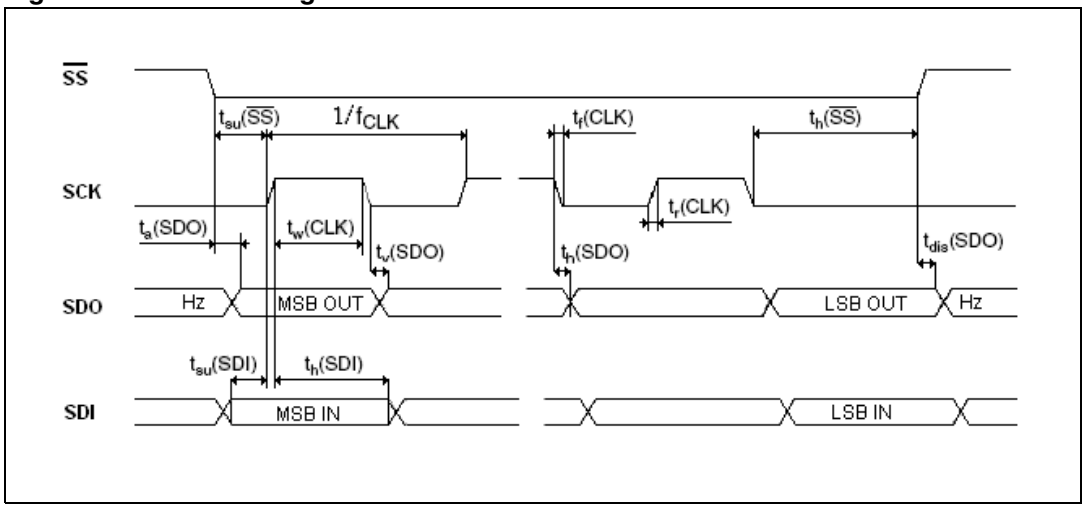



*Note: 1 Thermal shutdown intervention*
*2 Junction hysteresis*
*3 Restore to idle condition*
*4 Case hysteresis*

# 11 Interface timing diagram

## 11.1 SPI timing diagram

**Figure 12. Serial timing**



# 12 Switching parameters test condition

**Figure 13. $t_{ON}$ and $t_{OFF}$ time diagram test condition**

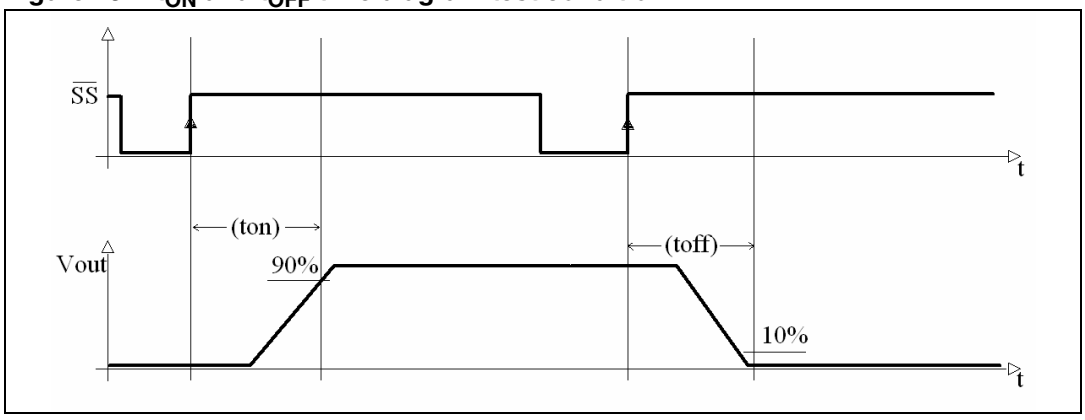



**Figure 14. $dV_{OUT}/dt_{ON}$ and $dV_{OUT}/dt_{OFF}$ time diagram test condition**

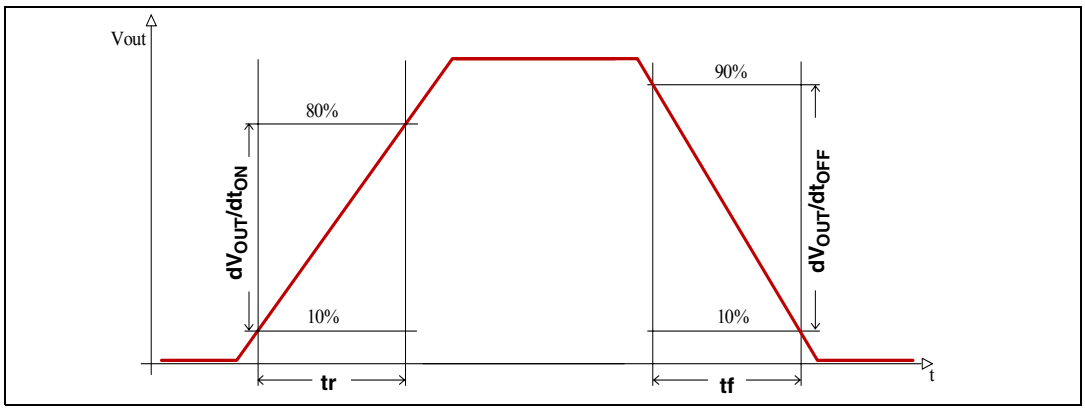



**Figure 15. $td_{ON}$ and $td_{OFF}$ time diagram test condition**

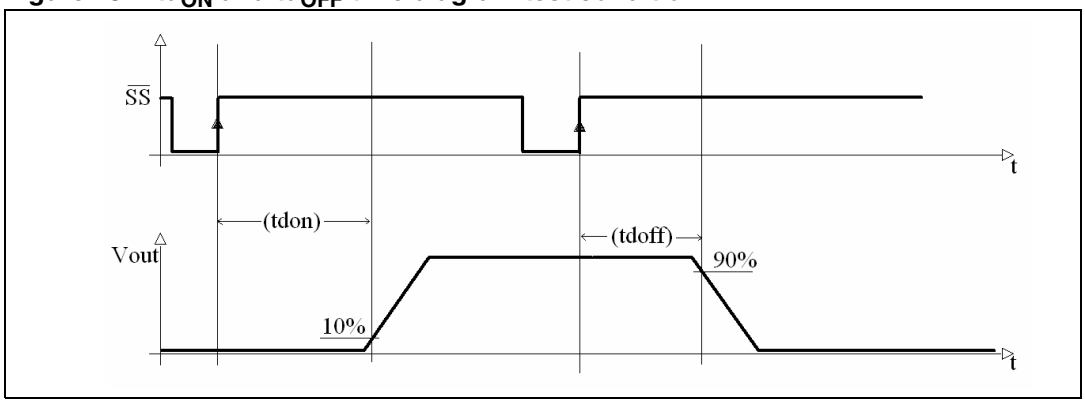
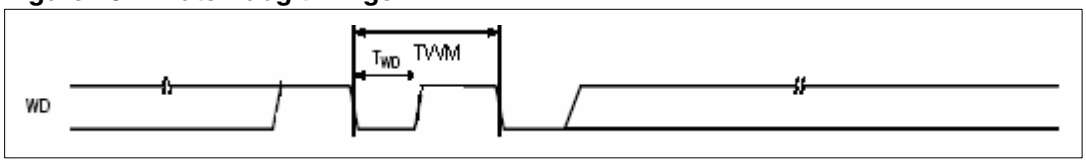



**Figure 16. Watch-dog timings**



# 13 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 15. PowerSSO-36™ mechanical data

| Symbol | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 2.15 | | 2.47 |
| A2 | 2.15 | | 2.40 |
| a1 | 0 | | 0.075 |
| b | 0.18 | | 0.36 |
| c | 0.23 | | 0.32 |
| D | 10.10 | | 10.50 |
| E | 7.4 | | 7.6 |
| e | | 0.5 | |
| e3 | | 8.5 | |
| F | | 2.3 | |
| G | | | 0.075 |
| G1 | | | 0.06 |
| H | 10.1 | | 10.5 |
| h | | | 0.4 |
| L | 0.55 | | 0.85 |
| M | | 4.3 | |
| N | | | 10deg |
| O | | 1.2 | |
| Q | | 0.8 | |
| S | | 2.9 | |
| T | | 3.65 | |
| U | | 1.0 | |
| X | 4.1 | | 4.7 |
| Y | 4.9 | | 5.5 |

**Figure 17. PowerSSO-36™ package dimensions**

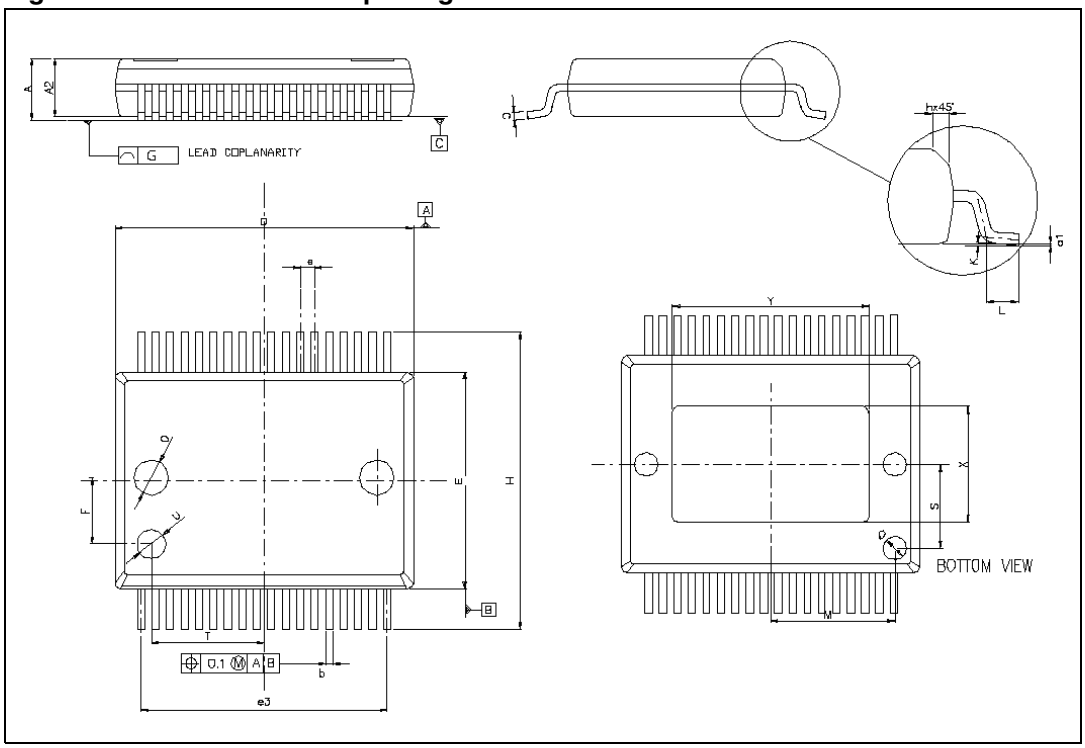



**Figure 18. PowerSSO-36™ tube shipment (no suffix)**

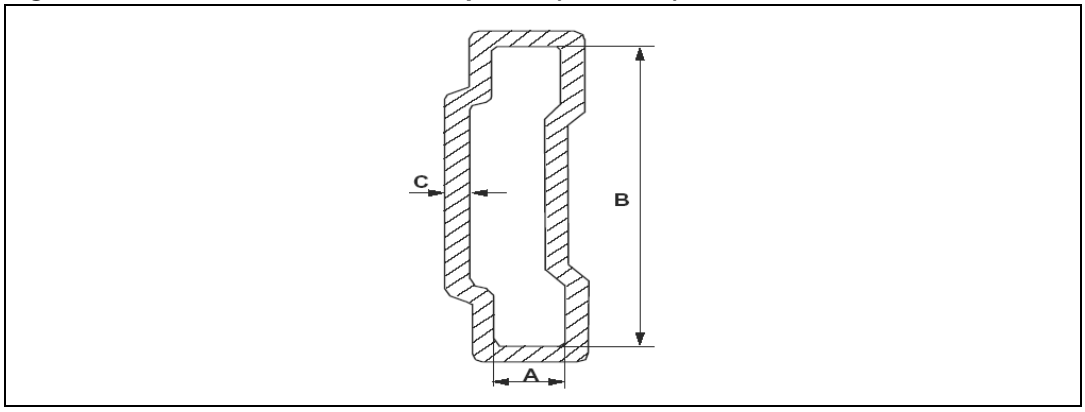



**Table 16. PowerSSO-36™ tube shipment**

| | |
|---|---|
| **Base Q.ty** | 49 |
| **Bulk Q.ty** | 1225 |
| **Tube length (± 0.5)** | 532 |
| **A** | 3.5 |
| **B** | 13.8 |
| **C (± 0.1)** | 0.6 |

*Note: All dimensions are in mm.*

**Figure 19. PowerSSO-36™ reel shipment (suffix “TR”)**

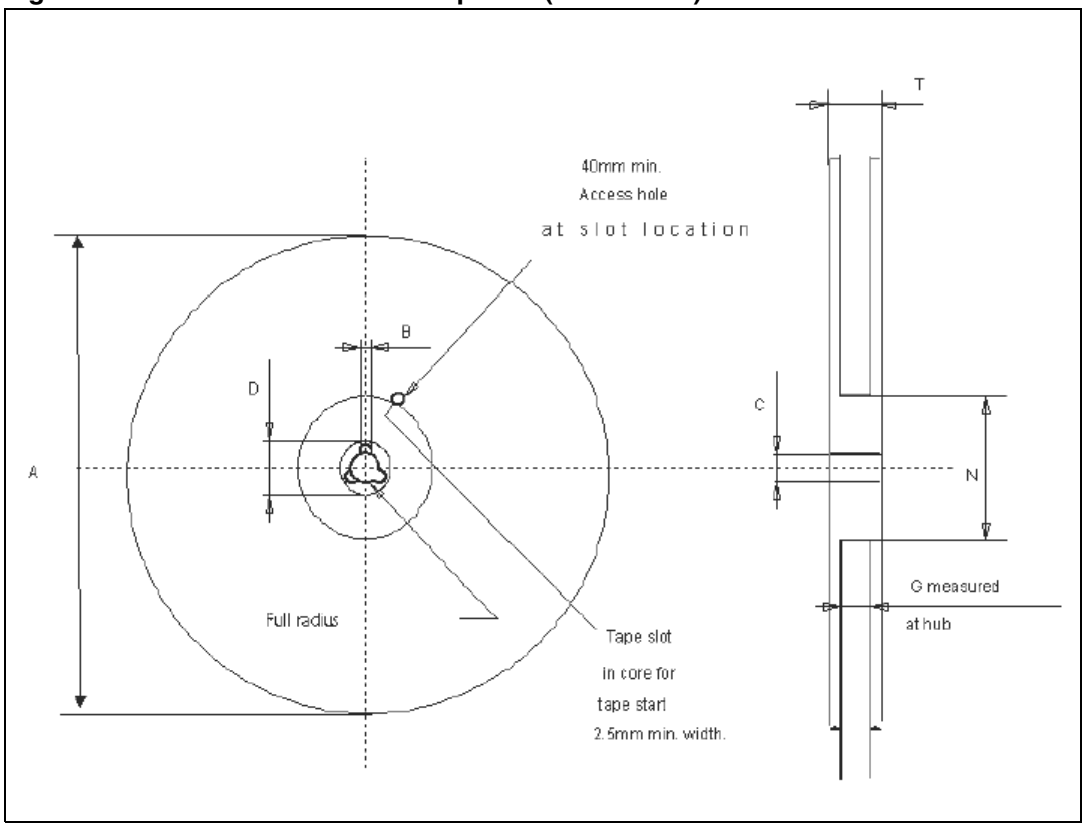



**Table 17. PowerSSO-36™ reel dimensions**

| | |
|---|---|
| **Base Q.ty** | 1000 |
| **Bulk Q.ty** | 1000 |
| **A (max)** | 330 |
| **B (min)** | 1.5 |
| **C (± 0.2)** | 13 |
| **F** | 20.2 |
| **G (2 ± 0)** | 24.4 |
| **N (min)** | 100 |
| **T (max)** | 30.4 |

**Figure 20. PowerSSO-36™ tape dimensions**

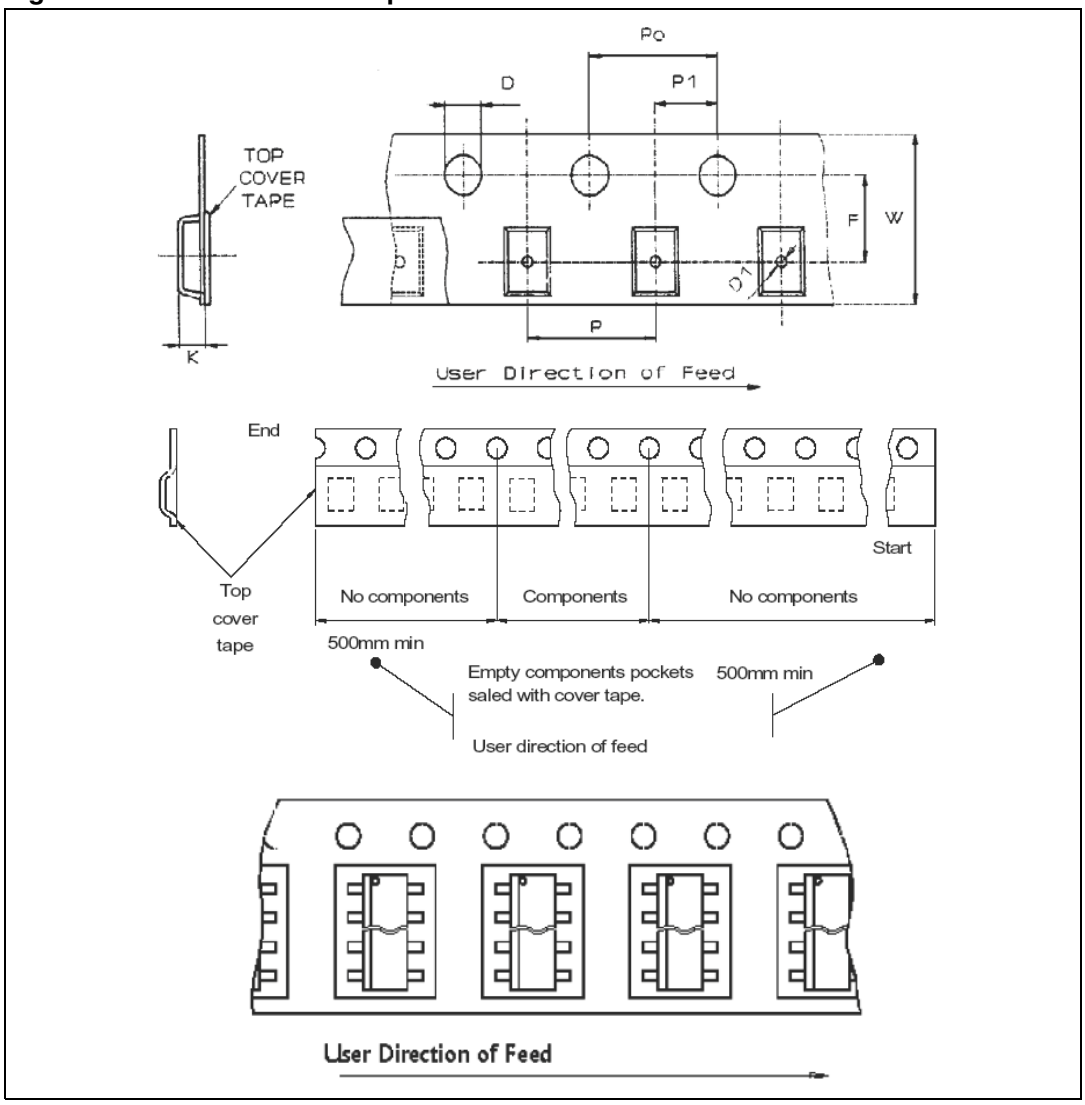



**Table 18. PowerSSO-36™ tape dimensions**

| | | |
|---|---|---|
| **Tape width** | W | 24 |
| **Tape hole spacing** | P0 (± 0.1) | 4 |
| **Component spacing** | P | 12 |
| **Hole diameter** | D (± 0.05) | 1.55 |
| **Hole diameter** | D1 (min) | 1.5 |
| **Hole position** | F (± 0.1) | 11.5 |
| **Compartment depth** | K (max) | 2.85 |
| **Hole spacing** | P1 (± 0.1) | 2 |

*Note: According to electronic industries association (EIA) standard 481 rev. A, Feb 1986*

# 14 Revision history

Table 19. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 04-Dec-2008 | 1 | Initial release |
| 29-Apr-2009 | 2 | Updated *Table 5 on page 9* |

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