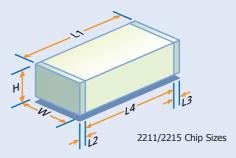
# Surface Mount Chip Capaciton Chip Safety Certified Surge Protection Chip

COG/X7R

Syfer Technology's Surge Protection (SP) range of ceramic chip capacitors are Class Y2/X1 compliant and designed for use in equipment certified to IEC 60950 (2000 Edition) where overvoltage surges can occur - i.e. a lightning strike.

This range of multilayer chip capacitors is approved and certified by TÜV. They meet the electrical requirements of IEC 60384-14: 1993 and EN 132400: 1994.

Also approved by UL for use in equipment certified to UL 60950 (previously UL 1950).



Case size	Nominal Cap value	Class	Dielectric	Tolerance	Approvals
2211	4.7pF	Y2, X1	C0G/NP0	±0.25pF, ±0.5pF	UL/TÜV
2211	5.6pF	Y2, X1	C0G/NP0	±0.25pF, ±0.5pF	UL/TÜV
2211	6.8pF	Y2, X1	C0G/NP0	±0.25pF, ±0.5pF	UL/TÜV
2211	8.2pF	Y2, X1	C0G/NP0	±0.25pF, ±0.5pF	UL/TÜV
2211	10pF	Y2, X1	COG/NP0	±1%, ±2%, ±5%, ±10%	UL/TÜV
2211	12pF	Y2, X1	COG/NP0	±1%, ±2%, ±5%, ±10%	UL/TÜV
2211	15pF	Y2, X1	COG/NP0	±1%, ±2%, ±5%, ±10%	
2211	18pF	Y2, X1	COG/NP0	±1%, ±2%, ±5%, ±10%	UL/TÜV
2211	22pF	Y2, X1	C0G/NP0	±1%, ±2%, ±5%, ±10%	UL/TÜV
2211	27pF	Y2, X1	C0G/NP0	±1%, ±2%, ±5%, ±10%	UL/TÜV
2211	33pF	Y2, X1	C0G/NP0	±1%, ±2%, ±5%, ±10%	UL/TÜV
2211	39pF	Y2, X1	COG/NPO COG/NPO	±1%, ±2%, ±5%, ±10% ±1%, ±2%, ±5%, ±10%	UL/TÜV
2211	47pF	Y2, X1	COG/NPO	±1%, ±2%, ±5%, ±10% ±1%, ±2%, ±5%, ±10%	UL/TÜV
2211	56pF	Y2, X1	COG/NPO COG/NPO	±1%, ±2%, ±5%, ±10% ±1%, ±2%, ±5%, ±10%	UL/TÜV
2211		Y2, X1			UL/TÜV
	68pF		COG/NP0	±1%, ±2%, ±5%, ±10%	UL/TÜV UL/TÜV
2211	82pF	Y2, X1	C0G/NP0	±1%, ±2%, ±5%, ±10%	
2211	100pF	Y2, X1	C0G/NP0	±1%, ±2%, ±5%, ±10%	UL/TÜV
2211	120pF	Y2, X1	C0G/NP0	±1%, ±2%, ±5%, ±10%	UL/TÜV
2211	150pF	Y2, X1	COG/NP0	±1%, ±2%, ±5%, ±10%	UL/TÜV
2211	180pF	Y2, X1	COG/NP0	±1%, ±2%, ±5%, ±10%	UL/TÜV
2211	220pF	Y2, X1	C0G/NP0	±1%, ±2%, ±5%, ±10%	UL/TÜV
2211	270pF	Y2, X1	C0G/NP0	±1%, ±2%, ±5%, ±10%	UL/TÜV
2211	330pF	Y2, X1	C0G/NP0	±1%, ±2%, ±5%, ±10%	UL/TÜV
2211	390pF	Y2, X1	C0G/NP0	±1%, ±2%, ±5%, ±10%	UL/TÜV
2211	470pF	Y2, X1	C0G/NP0	±1%, ±2%, ±5%, ±10%	UL/TÜV
2211	560pF	Y2, X1	C0G/NP0	±1%, ±2%, ±5%, ±10%	UL/TÜV
2211	680pF	Y2, X1	C0G/NP0	±1%, ±2%, ±5%, ±10%	UL/TÜV
2215	820pF	Y2, X1	C0G/NP0	±1%, ±2%, ±5%, ±10%	UL/TÜV
2215	1nF	Y2, X1	C0G/NP0	±1%, ±2%, ±5%, ±10%	UL/TÜV
2211	100pF	Y2, X1	X7R	±5%, ±10%, ±20%	UL/TÜV
2211	120pF	Y2, X1	X7R	±5%, ±10%, ±20%	UL/TÜV
2211	150pF	Y2, X1	X7R	±5%, ±10%, ±20%	UL/TÜV
2211	180pF	Y2, X1	X7R	±5%, ±10%, ±20%	UL/TÜV
2211	220pF	Y2, X1	X7R	±5%, ±10%, ±20%	UL/TÜV
2211					UL/TÜV
	270pF	Y2, X1	X7R X7R	±5%, ±10%, ±20%	
2211	330pF	Y2, X1		±5%, ±10%, ±20%	UL/TÜV
2211	390pF	Y2, X1	X7R	±5%, ±10%, ±20%	UL/TÜV
2211	470pF	Y2, X1	X7R	±5%, ±10%, ±20%	UL/TÜV
2211	560pF	Y2, X1	X7R	±5%, ±10%, ±20%	UL/TÜV
2211	680pF	Y2, X1	X7R	±5%, ±10%, ±20%	UL/TÜV
2211	820pF	Y2, X1	X7R	±5%, ±10%, ±20%	UL/TÜV
2211	1nF	Y2, X1	X7R	±5%, ±10%, ±20%	UL/TÜV

## **Electrical Specification**

**Operating Temperature Temperature Coefficient** 

 $COG/NPO = 0 \pm 30 \text{ ppm/}^{\circ}C$ , Ultra

(EIA Class II)

Insulation resistance at +25°C Insulation resistance at +125°C  $>10G\Omega$ 

**Dielectric Strength (DWV)** Rated voltage

**Climatic Category (IEC)** 

**Ageing rate** 

Test parameters for capacitance COG/NP0 = 1Vrms @ 1MHz @ 20°C

**Test parameters for DF** 

-55°C to +125°C

Stable Class 1 Ceramic (EIA Class 1)  $X7R = \pm 15\%$ , Stable Class II Ceramic

>100G $\Omega$ 

1500VAC/3000VDC

250VAC 55/125/56 C0G/NP0 = zero

X7R = 1% per decade of time

X7R = 1Vrms @ 1KHz @ 20°C C0G/NP0 = 1Vrms @ 1MHz @ 20°C X7R = 1Vrms @ 1KHz @ 20°C

#### **Mechanical Specification**

Length (L1) Width (W)

2211 size **2215 size** 

Thickness (H) **Termination Bands (L2, L3) Creepage Distance (L4) Termination Material Solderability** 

5.7mm  $\pm 0.4$ mm  $(0.225" \pm 0.016")$ 2.79mm  $\pm 0.3$ mm  $(0.110" \pm 0.012")$ 3.81mm  $\pm 0.35$ mm  $(0.150" \pm 0.014")$ 2.54 (0.1) Max.

0.25 - 0.80mm (0.01" - 0.03") 4.0mm (0.16") Min.

Nickel Barrier (Tin over Nickel) IFC 68-2-20



SS2211Y2.ver2

## Surface Mount Chip Capacitors Safety Certified Surge Protection Chip

COG/X7R

Specification		Details		
EN 132400: 1994 + A2: 1998 + A3: 1998 + A4: 1999		Meets the electrical requirements of these specifications for class Y2, X1 devices.		
IEC 60384-14 second + A1: 1995	d edition 1993			
UL 60950: third edition IEC 60950: 2000		Certified for use in equipment intending to be certified to these specifications.		
IEEE 802.3		Meets the 1500Vrms isolation requirements of section 12.10.1 of this specification.		

### **Approvals**

Marked parts can be released as certified by TÜV (C0G/NP0 and X7R). Unmarked parts can be supplied tested in accordance with, but not certified by TÜV.





TÜV Certificate Nos. R60001955 and R60003753

Reeled Quantities	178mm (7")	1000	
	330mm (13")	4000	

Ordering Information								
2211	J	A25	0102	J	X	T	SPU	
Chip Size 2211 2215	Termination J= Nickel Barrier Y= FlexiCap	Voltage A25=250VAC	Capacitance Expressed in picofarads (pF). First digit is 0. Second and third digits are significant figures of capacitance code. The fourth digit is number of zeros following. Example: 0102=1000pF. For values below 10pF insert a P for the decimal point. eg: 8P20=8.2pF	Tolerance <10pF C = ±0.25pF D = ±0.5pF ≥10pF F = ±1% G = ±2% J = ±5% K = ±10% M = ±20%	Dielectric C=COG/NPO X=X7R	Packaging T = 178mm (7") reel R = 330mm (13") reel B = Bulk	SPU=Unmarked SP=Marked	

