

# TDC1046

## Monolithic Video A/D Converter

### 6-Bit, 25 Msps

#### Features

- 6-bit resolution
- 1/4 LSB linearity
- Sample-and-hold circuit not required
- TTL compatible
- 25 Msps conversion rate
- Selectable output format
- Available in an 18-pin Cerdip
- Low cost
- Low analog input capacitance
- Available per Standard Military Drawing

#### Applications

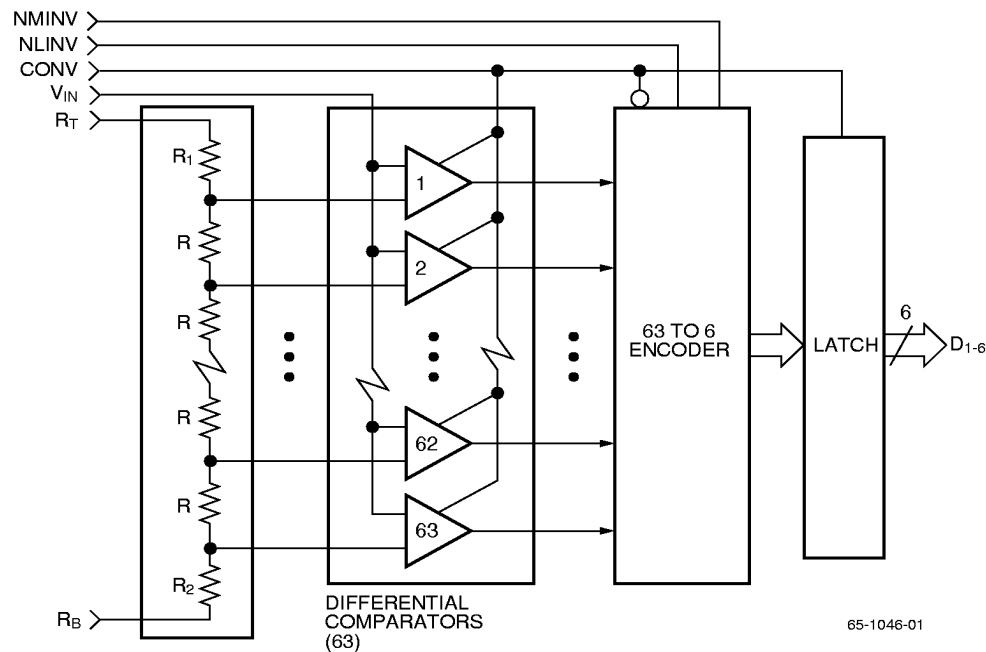
- Low-cost video digitizing
- Medical imaging
- Data acquisition
- TV special effects
- Video simulators
- Radar data conversion

#### Description

The TDC1046 is a 25 Msps (Megasample per second) full-parallel (flash) analog-to-digital converter, capable of converting an analog signal with full-power frequency components up to 12.5 MHz into 6-bit digital words. Use of a sample-and-hold circuit is not necessary for operation of the TDC1046. All digital inputs and outputs are TTL compatible.

The TDC1046 consists of 63 clocked latching comparators, encoding logic, and an output buffer register. A single convert signal controls the conversion operation. The unit can be connected to give either true or inverted outputs in binary or offset two's complement coding.

#### Block Diagram



Rev. 1.0.0

## Functional Description

### General Information

The TDC1046 has three functional sections: a comparator array, encoding logic, and output latches. The comparator array compares the input signal with 63 reference voltages to produce an N-of-63 code (sometimes referred to as a “thermometer” code, as all the comparators referred to voltages more positive than the input signal will be off, and those referred to voltages more negative than the input signal will be on). The encoding logic converts the N-of-63 code into binary or offset two’s complement coding, and can invert either output code. This coding function is controlled by DC signals on pins NMINV and NLINV. The output latch holds the output constant between updates.

### Power

The TDC1046 operates from two supply voltages, +5.0V and -5.2V. The return for ICC, the current drawn from the +5.0V supply, is DGND. The return for IEE, the current drawn from the -5.2V supply, is AGND. All power and ground pins must be connected.

### Reference

The TDC1046 converts analog signals in the range  $V_{RB} \leq V_{IN} \leq V_{RT}$  into digital form.  $V_{RB}$  (the voltage applied to  $R_B$  at the bottom of the reference resistor chain) and  $V_{RT}$  (the voltage applied to  $R_T$  at the top of the reference resistor chain) should be between +0.1V and -1.1V.  $V_{RT}$  should be more positive than  $V_{RB}$  within that range. The voltage applied across the reference resistor chain ( $V_{RT} - V_{RB}$ ) must be between 0.8V and 1.2V. The nominal voltages are  $V_{RT} = 0.00V$  and  $V_{RG} = -1.00V$ . These voltages may be varied dynamically up to 12.5MHz. Due to variation in the reference currents with clock and input signals,  $R_T$  and  $R_B$  should be low-impedance-to-ground points. For circuits in which the reference is not varied, a bypass capacitor to ground is recommended. If the reference inputs are exercised dynamically (as in an Automatic Gain Control circuit), a low-impedance reference source is required.

### Controls

Two function control pins, NMINV and NLINV are provided. These controls are for DC (i.e., steady states use. They permit the output coding to be either straight binary or offset two’s complement, in either true or inverted sense, according to the Output Coding Table. These pins are active LOW as signified by the prefix “N” in the signal name. They may be tied to VCC for a logic “1” and DGND for a logic “0.”

### Convert

The TDC1046 requires a CONVerT (CONV) signal. A sample is taken (the comparators are latched) within 5ns after a rising edge on the CONV pin. This time is  $t_{STO}$ . Sampling Time Offset. The 63 to 6 encoding is performed on the falling edge of the CONV signal. The coded result is transferred to the output latches on the next rising edge. The outputs hold the previous data a minimum time ( $t_{HO}$ ) after the rising edge of the CONV signal.

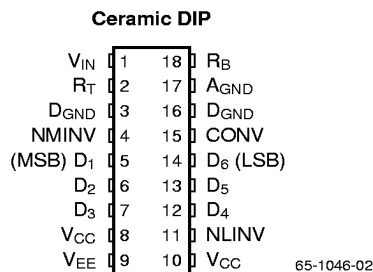
### Analog Input

The TDC1046 uses strobed latching comparators which cause the input impedance to vary with the signal level, as comparator input transistors are cut-off or become active. For optimal performance, the source impedance of the driving circuit must be less than 50  $\Omega$ . The input signal will not damage the TDC1046 if it remains within the range of  $V_{EE}$  to +0.5V. If the input signal is at a voltage between  $V_{RT}$  and  $V_{RB}$ , the output will be a binary number between 0 and 63 inclusive. A signal outside this range will indicate either full-scale positive or full-scale negative, depending on whether the signal is off-scale in the positive or negative direction.

### Outputs

The outputs of the TDC1046 are TTL compatible, and capable of driving four low-power Schottky TTL (54/74 LS) unit loads or the equivalent. The outputs hold the previous data a minimum time ( $t_{HO}$ ) after the rising edge of the CONV signal. Data is guaranteed to be valid after a maximum delay time ( $t_D$ ) after the rising edge of CONV. For optimum performance, 2.2 K $\Omega$  pull-up resistors are recommended.

## Pin Assignments



## Pin Descriptions

Pin Name	Pin Number	Value	Pin Function Description
<b>Power</b>			
VCC	8, 10	+5.0V	Positive Supply Voltage
VEE	9	-5.2V	Negative Supply Voltage
DGND	3, 16	0.0V	Digital Ground
AGND	17	0.0V	Analog Ground
<b>Reference</b>			
VRT	2	0.0V	Reference Resistor (Top)
VRB	18	-1.0V	Reference Resistor (Bottom)
<b>Controls</b>			
NMINV	4	TTL	Not Most Significant Bit INVert
NLINV	11	TTL	Not Least Significant Bit INVert
<b>Convert</b>			
CONV	15	TTL	Convert
<b>Analog Input</b>			
VIN	1	0V to -1V	Analog Signal Input
<b>Outputs</b>			
D1	5	TTL	MSB Output
D2	6	TTL	
D3	7	TTL	
D4	12	TTL	
D5	13	TTL	
D6	14	TTL	LSB Output

## Output Coding Table<sup>1</sup>

Range 15.8730mV Step	Binary		Two's Complement	
	True	Inverted	True	Inverted
	NMINV=1, NLINV=1	0, 0	0, 1	1, 0
0.0000V	000000	111111	100000	011111
-0.0159V	000001	111110	100001	011110
⋮	⋮	⋮	⋮	⋮
⋮	⋮	⋮	⋮	⋮
-0.4921V	011111	100000	111111	000000
-0.5079V	100000	011111	000000	111111
-0.5238V	100001	011110	000001	111110
⋮	⋮	⋮	⋮	⋮
⋮	⋮	⋮	⋮	⋮
-0.9841V	111110	000001	011110	100001
-1.0000V	111111	000000	011111	100000

**Note:**

1. Voltages are code midpoints when calibrated (see Calibration section).

## Absolute Maximum Ratings<sup>1</sup>

(beyond which the device will be damaged)

Parameter		Min.	Max.	Unit
<b>Supply Voltages</b>				
VCC (measured to DGND)		-0.5	+7.0	V
VEE (measured to AGND)		-7.0	+0.5	V
AGND (measured to DGND)		-0.5	+0.5	V
<b>Input Voltages</b>				
CONV, NMINV, NLINV (measured to DGND)		0.5	+5.5	V
VIN, VRT, VRB (measured to AGND)		+0.5	VEE	V
VRT (measured to VRB)		+1.2	-1.2	V
<b>Output</b>				
Applied voltage (measured to DGND) <sup>2</sup>		-0.5	5.5	V
Applied current, externally forced <sup>3, 4</sup>		-1.0	6.0	mA
Short circuit duration (single output in high state to ground)			1	sec
<b>Temperature</b>				
Operating	Case	-55	+125	°C
	Junction		+175	°C
Lead, soldering (10 seconds)			+300	°C
Storage		-65	+150	°C

### Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as positive when flowing into the device.

## Operating Conditions

Parameters		Temperature Range						Units
		Standard			Extended			
		Min.	Nom.	Max.	Min.	Nom.	Max.	
VCC	Positive Supply Voltage (measured to DGND)	4.75	5.0	5.25	4.5	5.0	5.5	V
VEE	Negative Supply Voltage (measured to AGND)	-4.9	-5.2	-5.5	-4.9	-5.2	-5.5	V
VAGND	Analog Ground Voltage (measured to DGND)	-0.1	0.0	0.1	-0.1	0.0	0.1	V
tPWL	CONV Pulse Width (LOW)	15			15			ns
tPWH	CONV Pulse Width (HIGH)	17			17			ns
VIL	Input Voltage, Logic LOW			0.8			0.8	V
VIH	Input Voltage, Logic HIGH	2.0			2.0			V
IOL	Output Current, Logic LOW			4.0			2.0	mA
IOH	Output Current, Logic HIGH			-0.4			-0.4	mA
VRT	Most Positive Reference Input <sup>1</sup>	-0.1	0.0	0.1	-0.1	0.0	0.1	V
VRB	Most Negative Reference Inputs <sup>1</sup>	-0.9	-1.0	-1.1	-0.9	-1.0	-1.1	V
VRT-VRB	Voltage Reference Differential	0.8		1.2	0.8		1.2	V
VIN	Input Voltage	VRB		VRT	VRB		VRT	V

## Operating Conditions (continued)

Parameters		Temperature Range						Units
		Standard			Extended			
		Min.	Nom.	Max.	Min.	Nom.	Max.	
TA	Ambient Temperature, Still Air	0		70				°C
TC	Case Temperature				-55		125	°C

**Note:**

1. V<sub>RT</sub> must be more positive than V<sub>RB</sub>, and voltage reference differential must be within specified range.

## DC Electrical Characteristics

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min.	Max.	Min.	Max.	
ICC	Positive Supply Current	VCC = MAX, static <sup>1</sup>		20		25	mA
IEE	Negative Supply Current	V <sub>EE</sub> = MAX, static <sup>1</sup>					
		T <sub>A</sub> = 0°C to 70°C		-95			mA
		T <sub>A</sub> = 70°C		-75			mA
		T <sub>C</sub> = -55°C to 125°C				-150	mA
		T <sub>C</sub> = 125°C				- 75	mA
IREF	Reference Current	V <sub>RT</sub> , V <sub>RB</sub> = NOM		10		15	mA
RREF	Total Reference Resistance	V <sub>RT</sub> – V <sub>RB</sub> = MAX	100		66		Ω
RIN	Input Equivalent Resistance	V <sub>RT</sub> , V <sub>RG</sub> = NOM, V <sub>IN</sub> = V <sub>RB</sub>	40		40		KΩ
CIN	Input Capacitance			30		30	pF
ICB	Input Constant Bias Current	V <sub>EE</sub> = MAX		105		180	mA
IIL	Input Current, Logic LOW	VCC = MAX, V <sub>I</sub> = 0.5V					
		CONV		-0.4		-0.6	mA
		NMINV, NLINV		-0.6		-0.8	mA
IIH	Input Current, Logic HIGH	VCC = MAX, V <sub>I</sub> = 2.4V		50		50	pA
II	Input Current, Max Input Voltage	VCC = MAX, V <sub>I</sub> = 5.5V		1.0		1.0	mA
VOL	Output Voltage, Logic LOW	VCC = MIN, I <sub>OL</sub> = 2 mA		0.5		0.5	V
VOH	Output Voltage, Logic HIGH	VCC = MIN, I <sub>OH</sub> = MAX	2.4		2.4		V
IOS	Short Circuit Output Current	VCC = MAX, One pin to ground, one second duration, output HIGH		-30		-30	mA
CI	Digital Input Capacitance	T <sub>A</sub> = 25°C, F = 1MHz		15		15	pF

**Note:**

1. Worst case, all digital inputs and outputs LOW.

## AC Electrical Characteristics

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
F <sub>S</sub>	Maximum Conversion Rate	V <sub>CC</sub> = MIN, V <sub>EE</sub> = MIN	25		25		Msp/s
t <sub>STO</sub>	Sampling Time Offset	V <sub>CC</sub> = MIN, V <sub>EE</sub> = MIN		5		10	ns
t <sub>D</sub>	Output Delay	V <sub>CC</sub> = MIN, V <sub>EE</sub> = MIN, Load 1		30		35	ns
t <sub>HO</sub>	Output Hold Time	V <sub>CC</sub> = MAX, V <sub>EE</sub> = MAX, Load 1	5		5		ns

## Timing Diagram

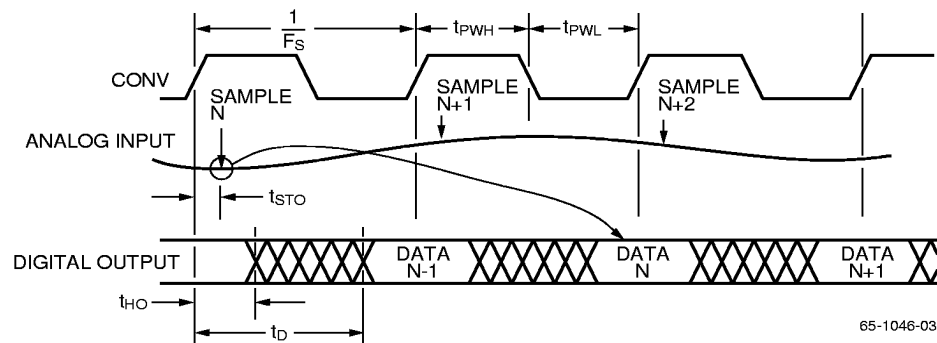
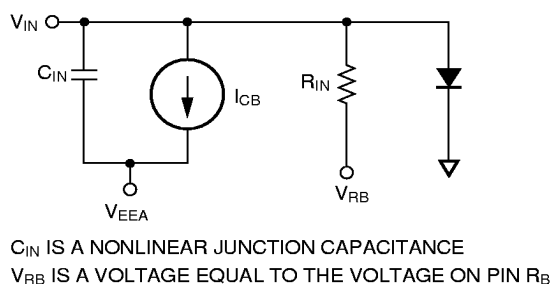
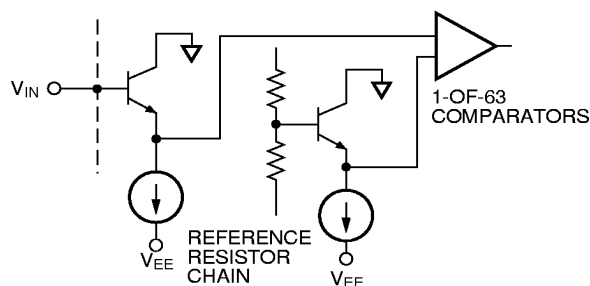


Figure 1. Timing Diagram

## System Performance Characteristics

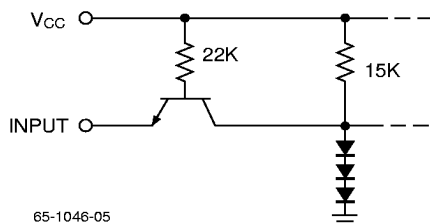
Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
ELI	Linearity Error Integral, Independent	V <sub>RT</sub> , V <sub>RB</sub> = Nom		0.4		0.4	%
ELD	Linearity Error Differential			0.4		0.4	%
CS	Code Size	V <sub>RT</sub> , V <sub>RB</sub> = Nom	50	150	50	150	% Nominal
EOT	Offset Error, Top	V <sub>IN</sub> = V <sub>RT</sub>		+50		+50	mV
EOB	Offset Error, Bottom	V <sub>IN</sub> = V <sub>RB</sub>		-30		-30	mV
T <sub>CO</sub>	Temperature Coefficient (Offset Voltage)			±20		±20	μV/°C
BW	Bandwidth, Full Power Input		12.5		12.5		MHz
t <sub>TR</sub>	Transient Response, Full-Scale			10		10	ns
SNR	Signal-to-Noise Ratio	12.5MHz Bandwidth, 25Mbps Conversion Rate					
	Peak Signal/RMS Noise	1 MHz Input	42		36		dB
		12.5 MHz Input	40		32		dB
	RMS Signal/RMS Noise	1 MHz Input	33		33		dB
		12.5 MHz Input	31		29		dB
EAP	Aperture Error			30		30	ps

## Equivalent Circuits



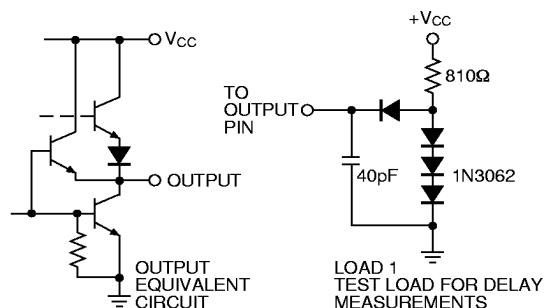
65-1046-04

Figure 2. Simplified Analog Input Equivalent Circuit



65-1046-05

Figure 3. Digital Input Equivalent Circuit



65-1046-06

Figure 4. Output Circuits

## Applications Discussion

### Calibration

To calibrate the TDC1046, adjust  $V_{RT}$  and  $V_{RB}$  to set the 1st and 63rd thresholds to the desired voltages. In the Block Diagram, note that  $R_1$  is greater than  $R$ , ensuring calibration with a positive voltage on  $R_T$ . Assuming a 0V to -1V desired range, continuously strobe the converter with -0.0079V on the analog input, and adjust  $V_{RT}$  for output toggling between codes 00 and 01. Then apply -0.9921V and adjust  $V_{RB}$  for toggling between codes 62 and 63. Instead of adjusting  $V_{RT}$ ,  $R_T$  can be connected to analog ground and the 0V end of the range calibrated with a buffer offset control.  $R_B$  is a convenient point for gain adjust that is not in the analog signal path. These techniques are employed in Figure 5.

### Typical Interface Circuit

The TDC1046 does not require a special input buffer amplifier to drive the analog input because of its low analog input capacitance. A terminated low-impedance transmission line ( $< 100 \Omega$ ) connected to the  $V_{IN}$  terminals of the TDC1046 is sufficient if the input voltage levels match those of the A/D converter.

However, many driver circuits lack sufficient offset control, drive current, or gain control. The Typical Interface Circuit

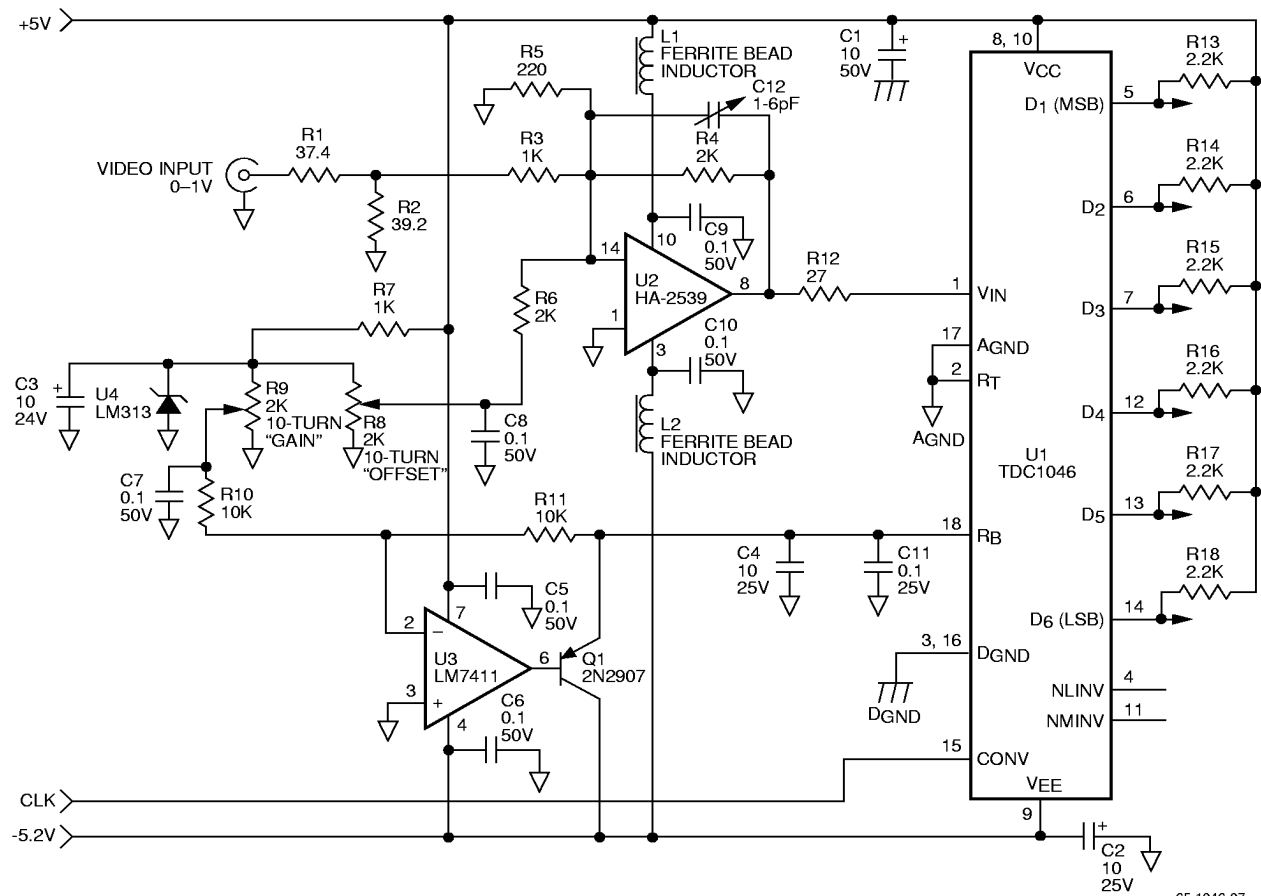
(Figure 5) shows a simple buffer amplifier and voltage reference circuit that may be used with the TDC1046. U2 is a wide-band operational amplifier with a gain factor of -2. A small value resistor,  $R_{12}$ , serves to help isolate the input capacitance of the A/D converter from the amplifier output and insure frequency stability. The pulse and frequency response of the buffer amplifier are optimized by variable capacitor  $C_{12}$ .

The reference voltage for the TDC1046 is generated by amplifier U3 and PNP transistor Q1 which supplies the reference current. System gain is adjusted by varying  $R_9$  which controls the reference voltage level to the A/D converter.

Input voltage range and input impedance for the circuit are determined by resistors  $R_1$  and  $R_2$ . Formulas for calculating values for these input resistors are:

$$R_1 = \frac{1}{\left(\frac{2VR}{Z_{IN}}\right) - \frac{1}{1000}} \quad \text{and} \quad R_2 = Z_{IN} - \left(\frac{1000 R_1}{1000 + R_1}\right)$$

where  $VR$  is the input voltage range of the circuit,  $Z_{IN}$  is the input impedance of the circuit, and the constant 1000 comes from the value of  $R_3$ . As shown, the circuit is set up for 1Vp-p  $75 \Omega$  video input.



**Figure 5. Typical Interface Circuit**

## Standard Military Drawing

These devices are also available as products manufactured, tested, and screened in compliance with Standard Military Drawings (SMDs). The nearest vendor equivalent product is shown below; however, the applicable SMD is the sole controlling document defining the SMD product.

Standard Military Drawing	Nearest Equivalent Fairchild Product No.	Package
5962-87786-01VA	TDC1046B8V	18 Pin CerDIP



**Notes:**

**Notes:**

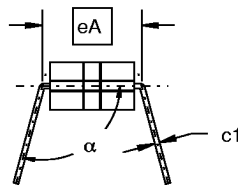
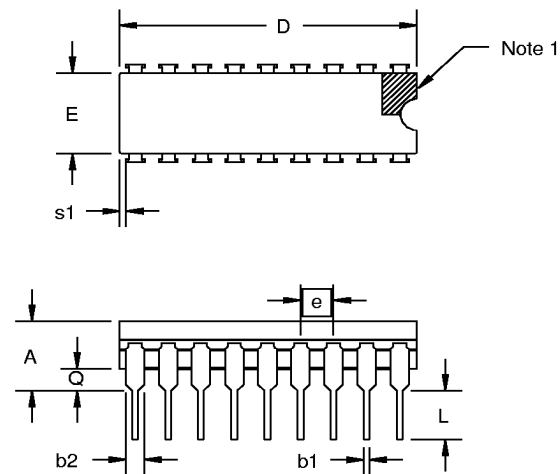
## Mechanical Dimensions

### 18-Lead Ceramic DIP

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.200	—	5.08	
b1	.014	.023	.36	.58	8
b2	.045	.065	1.14	1.65	2, 8
c1	.008	.015	.20	.38	8
D	—	.960	—	24.38	4
E	.220	.310	5.59	7.87	4
e	.100 BSC		2.54 BSC		5, 9
eA	.300 BSC		7.62 BSC		7
L	.125	.200	3.18	5.08	
Q	.015	.070	.38	1.78	3
s1	.005	—	.13	—	6
$\alpha$	90°	105°	90°	105°	

#### Notes:

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 8, 9 and 18 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within  $\pm .010$  (.25mm) of its exact longitudinal position relative to pins 1 and 18.
6. Applies to all four corner's (leads number 1, 8, 9, and 18).
7. "eA" shall be measured at the center of the lead bends or at the centerline of the leads when " $\alpha$ " is 90°.
8. All leads – Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish is applied.
9. Sixteen spaces.



## Ordering Information

Product Number	Temperature Range	Screening	Package	PackageMarking
TDC1046B8C	STD-T <sub>A</sub> = 0°C to 70°C	Commercial	18 Lead Ceramic DIP	1046B8C
TDC1046B8V	EXT-T <sub>C</sub> = -55°C to 125°C	MIL-STD-883	18 Lead Ceramic DIP	1046B8V
5962-87786-01VA	EXT-T <sub>C</sub> = -55°C to 125°C	Per Standard Military Drawing	18 Lead Ceramic DIP	5962-87786-01VA

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