12-Bit, 40MSPS Sampling, +3.3V ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **HIGH SNR: 70dB**
- **HIGH SFDR: 88dBFS**
- **LOW POWER: 195mW**
- **INTERNAL/EXTERNAL REFERENCE OPTION**
- **SINGLE-ENDED OR FULLY DIFFERENTIAL ANALOG INPUT**
- **PROGRAMMABLE INPUT RANGE**
- **LOW DNL: 0.3LSB**
- **SINGLE +3.3V SUPPLY OPERATION**
- **TQFP-48 PACKAGE**

APPLICATIONS

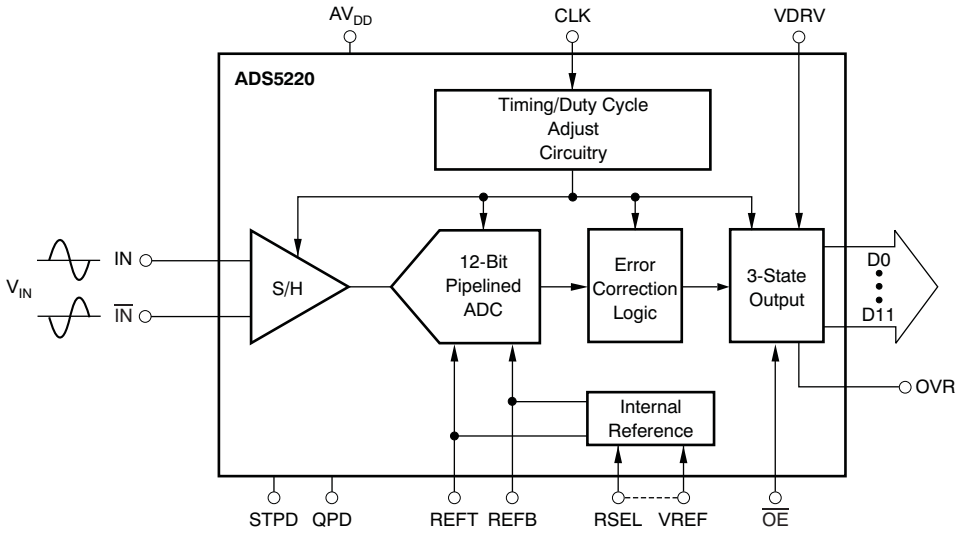
- **WIRELESS LOCAL LOOP**
- **COMMUNICATIONS**
- **MEDICAL IMAGING**
- **PORTABLE INSTRUMENTATION**

DESCRIPTION

The ADS5220 is a pipeline, CMOS analog-to-digital converter (ADC) that operates from a single +3.3V power supply. This converter can be operated with a single-ended input or differential input. The ADS5220 includes a 12-bit quantizer, high bandwidth track-and-hold, and an internal reference. It also allows the user to disable the internal reference and utilize external references which provide excellent gain and offset matching when used in multi-channel applications or in applications where full-scale range adjustment is required.

The ADS5220 employs digital error correction techniques to provide excellent differential linearity for demanding imaging applications. Its low distortion and high SNR give the extra margin needed for medical imaging, communications, video, and test instrumentation. The ADS5220 offers power dissipation of 195mW and also provides two power-down modes.

The ADS5220 is specified at a maximum sampling frequency of 40MSPS and a differential input range of 1V to 2V. The ADS5220 is available in a TQFP-48 package.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS5220	TQFP-48	PFB	–40°C to +85°C	ADS5220PFB	ADS5220PFBT	Tape and Reel, 250
					ADS5220PFBR	Tape and Reel, 2000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

	ADS5220	UNIT
AV_{DD}, DV_{DD}, VDRV	+3.8	V
Analog input	–0.3V to ($+V_S$ + 0.3)	V
Logic input	–0.3V to ($+V_S$ + 0.3)	V
Case temperature	+100	°C
Junction temperature, T_J	+150	°C
Storage temperature	+150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: AV_{DD} = +3.3V

T_{MIN} = –40°C, T_{MAX} = +85°C. Typical values are at T_A = +25°C, sampling rate = 40MSPS, 50% clock duty cycle, AV_{DD} = 3.3V, DV_{DD} = 3.3V, VDRV = 2.5V, –1dBFS, DCA off, internal reference voltage, and $2V_{PP}$ differential input, unless otherwise noted.

PARAMETER	CONDITIONS	ADS5220			UNIT
		MIN	TYP	MAX	
RESOLUTION			12 Tested		Bits
SPECIFIED TEMPERATURE RANGE	Ambient air		–40 to +85		°C
ANALOG INPUT					
Single-Ended Input Range	$2V_{PP}$	0.5		2.5	V
Optional Single-Ended Input Range	$1V_{PP}$	1		2	V
Differential Input Range	$2V_{PP}$	1		2	V
Analog Input Bias Current			1		µA
Input Impedance	Static, no clock		1.25 || 5		MΩ || pF
Analog Input Bandwidth	–3dBFS input		300		MHz
CONVERSION CHARACTERISTICS					
Sample Rate		1M		40M	Samples/s
Data Latency			4.5		Clock cycles
Clock Duty Cycle	Mode select enabled		35 to 65		%
DYNAMIC CHARACTERISTICS					
Differential Linearity Error (largest code error)					
f = 2.4MHz			±0.3	±0.75	LSB
f = 9.7MHz			±0.35		LSB
No Missing Codes			Tested		
Integral Nonlinearity Error, f = 2.4MHz			±0.7	±1.5	LSBs
Spurious-Free Dynamic Range(1)	Referred to full-scale				
f = 2.4MHz			88		dBFS(2)
f = 9.7MHz		83	88		dBFS
f = 19.8MHz			76		dBFS
2-Tone Intermodulation Distortion(3)					
f = 9.5MHz and 10.5MHz (–7dB each tone)			86.3		dBc
Signal-to-Noise Ratio (SNR)	Referred to full-scale				
f = 2.4MHz			70		dBFS
f = 9.7MHz		68.5	70		dBFS
f = 19.8MHz			69		dBFS
Signal-to-(Noise + Distortion) (SINAD)	Referred to full-scale				
f = 2.4MH			69		dBFS
f = 9.7MHz		68	69		dBFS
f = 19.8MHz			68		dBFS
Effective Number of Bits(4), f = 2.4MHz			11.2		Bits
Output Noise	Input Tied to Common-Mode		0.3		LSB_{RMS}
Aperture Delay Time			3.0		ns
Aperture Jitter			1.2		ps_{RMS}
Over-Voltage Recovery Time			1.0		Clock Cycle
Full-Scale Step Acquisition Time			5.0		ns

(1) *Spurious-free dynamic range* refers to the magnitude of the largest harmonic.
(2) dBFS means *dB relative to Full-Scale*.
(3) Two-tone intermodulation distortion is referred to the largest fundamental tone. This number will be 6dB higher if it is referred to the magnitude of the two-tone fundamental envelope.
(4) *Effective Number of Bits* (ENOB) is defined by (SINAD – 1.76) / 6.02.

ELECTRICAL CHARACTERISTICS: AV_{DD} = +3.3V (continued)

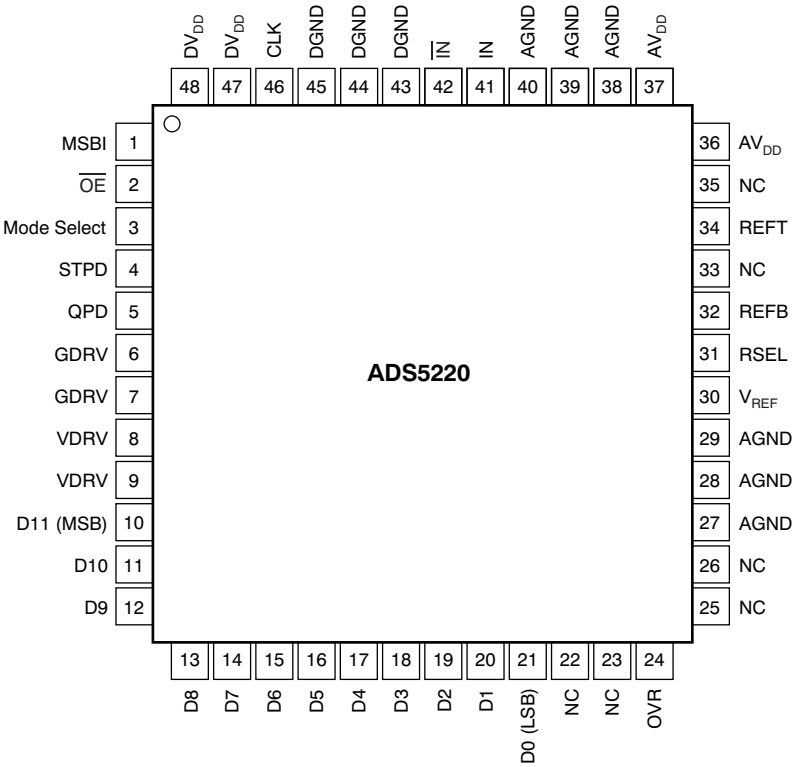
T_{MIN} = –40°C, T_{MAX} = +85°C. Typical values are at T_A = +25°C, sampling rate = 40MSPS, 50% clock duty cycle, AV_{DD} = 3.3V, DV_{DD} = 3.3V, VDRV = 2.5V, –1dBFS, DCA off, internal reference voltage, and $2V_{PP}$ differential input, unless otherwise noted.

PARAMETER	CONDITIONS	ADS5220 MIN	ADS5220 TYP	ADS5220 MAX	UNIT
DIGITAL INPUTS					
Logic Family			CMOS-compatible		
Convert Command	Start conversion		Rising edge of Convert clock		
High-Level Input Current[5] (V_{IN} = $3V_{DD}$)				100	µA
Low-Level Input Current (V_{IN} = 0V)				10	µA
High-Level Input Voltage		+1.7			V
Low-Level Input Voltage				+0.7	V
Input Capacitance			5		pF
DIGITAL OUTPUTS					
Logic Family			CMOS-compatible		
Logic Coding			Straight Offset Binary or BTC		
Low Output Voltage (I_{OL} = 50µA to 1.5mA)				+0.1	V
High Output Voltage (I_{OH} = 50µA to 0.5mA)		+2.4			V
3-State Enable Time			20	40	ns
3-State Disable Time			2	10	ns
Output Capacitance			5		pF
ACCURACY (Internal Reference, $2V_{PP}$, unless otherwise noted)					
Zero Error (referred to midscale)	f_{IN} = 2.4MHz, at 25°C		±0.75	±1.5	%FS
Zero Error Drift (referred to midscale)	f_{IN} = 2.4MHz		5		ppm/°C
Gain Error[6]	at 25°C		±0.4	±3.0	%FS
Gain Error Drift			38		ppm/°C
Power-Supply Rejection of Gain	ΔV_S = ±5%		52		dB
INTERNAL VOLTAGE REFERENCE					
Output Voltage Error (1V)			±10		mV
Load Regulation at 1mA			0.15		%
Output Voltage Error (0.5V)			±5		mV
Load Regulation at 0.5mA			0.1		%
POWER-SUPPLY REQUIREMENTS					
Supply Voltage: AV_{DD}, DV_{DD}	Operating	+3.0	+3.3	+3.6	V
Driver Supply Voltage		+2.3	+2.5	+3.6	V
Supply Current: $+I_S$	Operating (External reference)		59		mA
Power Dissipation:					
VDRV = 2.5V			195	215	mW
VDRV = 3.3V			200		mW
Standard Power-Down			15		mW
Quasi-Power-Down			75		mW
Thermal Resistance, θ_{JA}					
TQFP-48			63.7		°C/W
QFN-48			26.1		°C/W

(5) A 50kΩ pull-down resistor is inserted internally on the $\overline{OE}$ pin.
(6) Includes internal reference.

PIN CONFIGURATION

PFB PACKAGE
TQFP-48
(TOP VIEW)



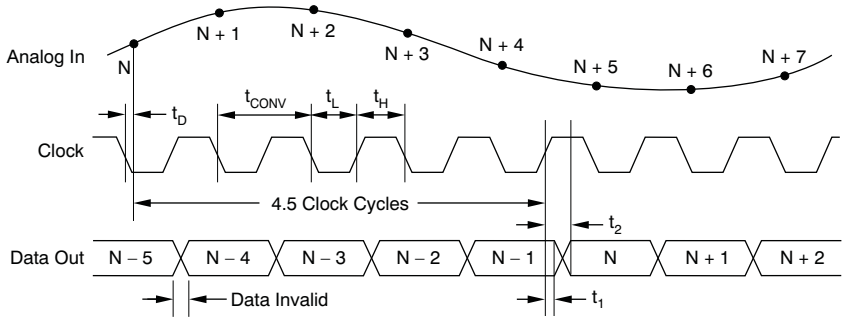
PIN ASSIGNMENTS

PIN		I/O	DESCRIPTION
NO.	NAME		
1	MSBI		Most Significant Bit Invert (HI = Binary Two's Complement, LO = Straight Offset Binary)
2	$\overline{OE}$		Tri-State (LO = Enabled, HI = Tri-State)
3	Mode Select		Duty Cycle Stablilizer (HI = Enabled, LO = Normal Operation)
4	STPD		Standard Power Down (LO = Normal Operation, HI = Enabled)
5	QPD		Quasi Power Down (LO = Normal Operation, HI = Enabled)
6	GDRV		Output Driver Ground
7	GDRV		Output Driver Ground
8	VDRV		Output Driver Supply
9	VDRV		Output Driver Supply
10	D11 (MSB)	O	Data Bit 12
11	D10	O	Data Bit 11
12	D9	O	Data Bit 10
13	D8	O	Data Bit 9
14	D7	O	Data Bit 8
15	D6	O	Data Bit 7
16	D5	O	Data Bit 6
17	D4	O	Data Bit 5
18	D3	O	Data Bit 4
19	D2	O	Data Bit 3

PIN ASSIGNMENTS (continued)

PIN		I/O	DESCRIPTION
NO.	NAME		
20	D1	O	Data Bit 2
21	D0 (LSB)	O	Data Bit 1
22	NC		No internal connection
23	NC		No internal connection
24	OVR		Over-Range Indicator
25	NC		No internal connection
26	NC		No internal connection
27	AGND		Analog Ground
28	AGND		Analog Ground
29	AGND		Analog Ground
30	V_{REF}		Internal Voltage Reference (1/2V Reference)
31	RSEL		Reference Mode Select (see Table 1 for settings)
32	REFB		Bottom Reference Bypass
33	NC		No internal connection
34	REFT		Top Reference Bypass
35	NC		No internal connection
36	AV_{DD}		Analog Supply
37	AV_{DD}		Analog Supply
38	AGND		Analog Ground
39	AGND		Analog Ground
40	AGND		Analog Ground
41	IN	I	Analog Input
42	$\overline{IN}$	I	Complementary Analog Input
43	DGND		Digital Ground
44	DGND		Digital Ground
45	DGND		Digital Ground
46	CLK	I	Convert Clock Input
47	DV_{DD}	I	Digital Supply
48	DV_{DD}	I	Digital Supply

TIMING DIAGRAM



TIMING CHARACTERISTICS

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{CONV}	Convert Clock Period	25		1000	ns
t_L	Clock Pulse LOW	8.75	12.5		ns
t_H	Clock Pulse HIGH	8.75	12.5		ns
t_D	Aperture Delay		3		ns
t_1	New Data Delay Time, C_L = 0pF	3.9			ns
t_2	New Data Delay Time, C_L = 15pF max			12	ns

TYPICAL CHARACTERISTICS: AV_{DD} = 3.3V

T_{MIN} = –40°C, T_{MAX} = +85°C. Typical values are at T_A = +25°C, sampling rate = 40MSPS, 50% clock duty cycle, AV_{DD} = 3.3V, DV_{DD} = 3.3V, VDRV = 2.5V, –1dBFS, DCA off, internal reference voltage, and $2V_{PP}$ differential input, unless otherwise noted.

SPECTRAL PERFORMANCE
(Differential, $2V_{PP}$)

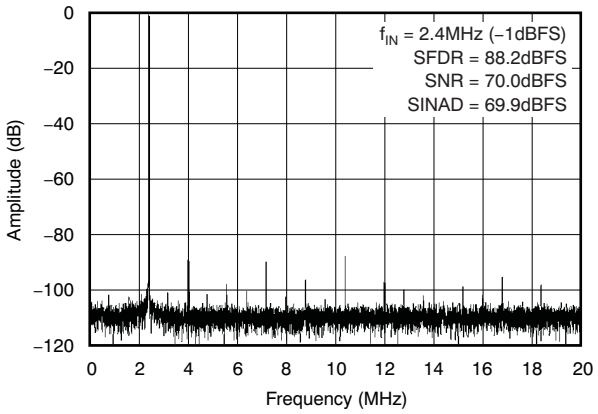


Figure 1.

SPECTRAL PERFORMANCE
(Differential, $2V_{PP}$)

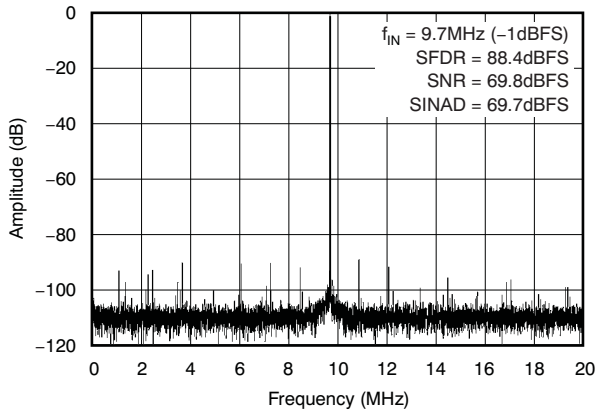


Figure 2.

SPECTRAL PERFORMANCE
EXTERNAL REFERENCE
(Differential, $2V_{PP}$)

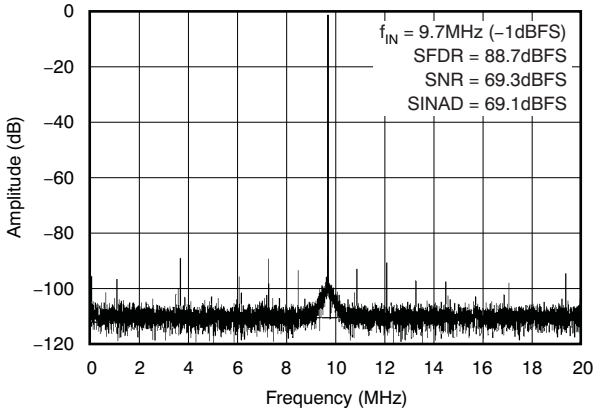


Figure 3.

SPECTRAL PERFORMANCE
PROGRAMMED REFERENCE
(Differential, $1.5V_{PP}$)

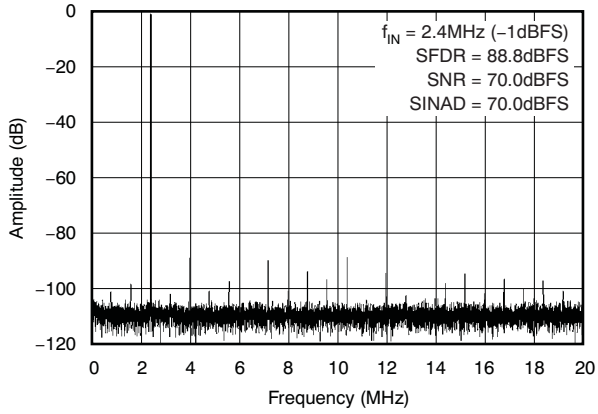


Figure 4.

SPECTRAL PERFORMANCE
(Differential, $1V_{PP}$)

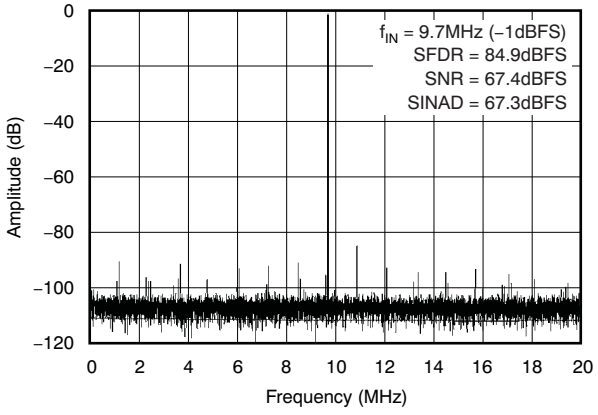


Figure 5.

SPECTRAL PERFORMANCE
(Single-Ended, $1V_{PP}$)

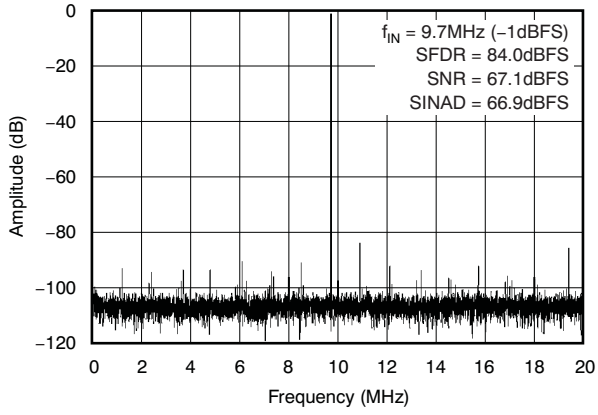


Figure 6.

TYPICAL CHARACTERISTICS: AV_{DD} = 3.3V (continued)

T_{MIN} = –40°C, T_{MAX} = +85°C. Typical values are at T_A = +25°C, sampling rate = 40MSPS, 50% clock duty cycle, AV_{DD} = 3.3V, DV_{DD} = 3.3V, VDRV = 2.5V, –1dBFS, DCA off, internal reference voltage, and $2V_{PP}$ differential input, unless otherwise noted.

SPECTRAL PERFORMANCE (Single-Ended, $2V_{PP}$)

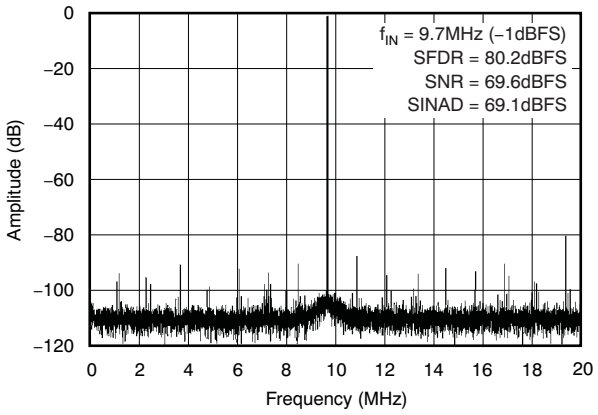


Figure 7.

TWO-TONE INTERMODULATION DISTORTION

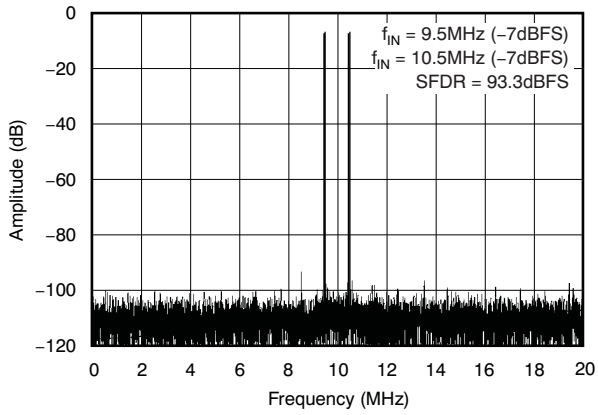


Figure 8.

INTEGRAL LINEARITY ERROR

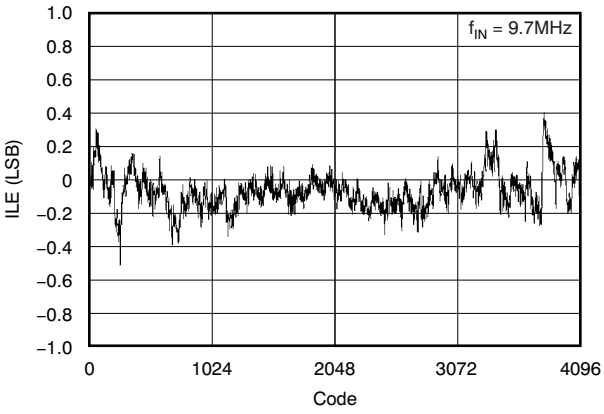


Figure 9.

INTEGRAL LINEARITY ERROR EXTERNAL REFERENCE

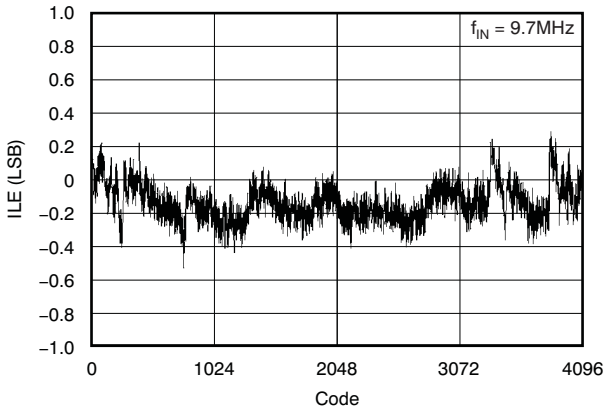


Figure 10.

DIFFERENTIAL LINEARITY ERROR EXTERNAL REFERENCE

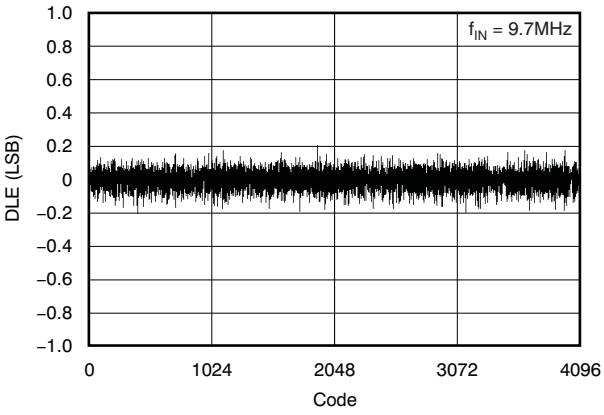


Figure 11.

DIFFERENTIAL LINEARITY ERROR

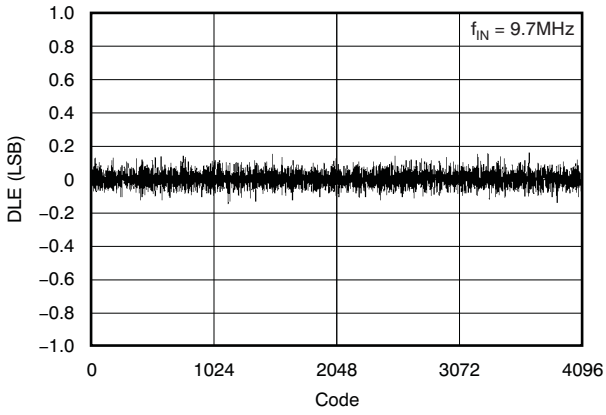


Figure 12.

TYPICAL CHARACTERISTICS: AV_{DD} = 3.3V (continued)

T_{MIN} = –40°C, T_{MAX} = +85°C. Typical values are at T_A = +25°C, sampling rate = 40MSPS, 50% clock duty cycle, AV_{DD} = 3.3V, DV_{DD} = 3.3V, VDRV = 2.5V, –1dBFS, DCA off, internal reference voltage, and $2V_{PP}$ differential input, unless otherwise noted.

SFDR/SNR vs CLOCK DUTY CYCLE (DCA = Duty Cycle Adjust)

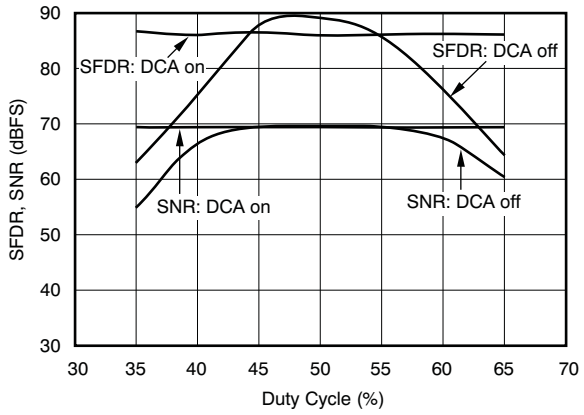


Figure 13.

SWEPT POWER (SNR) EXTERNAL REFERENCE

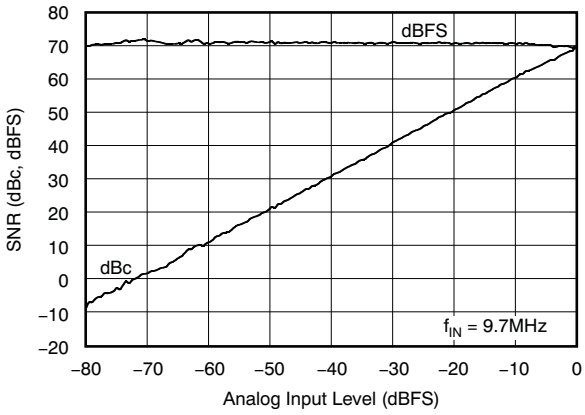


Figure 14.

SWEPT POWER (SFDR)

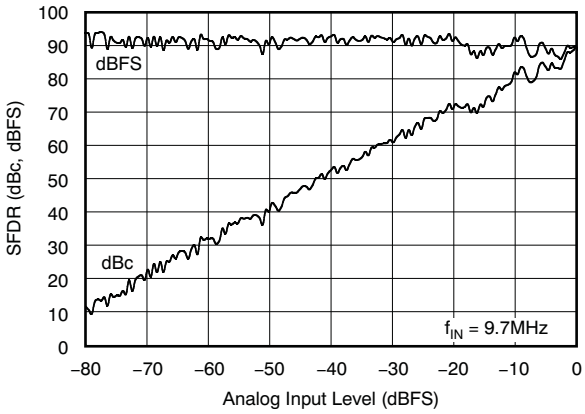


Figure 15.

SNR, SFDR vs INPUT FREQUENCY

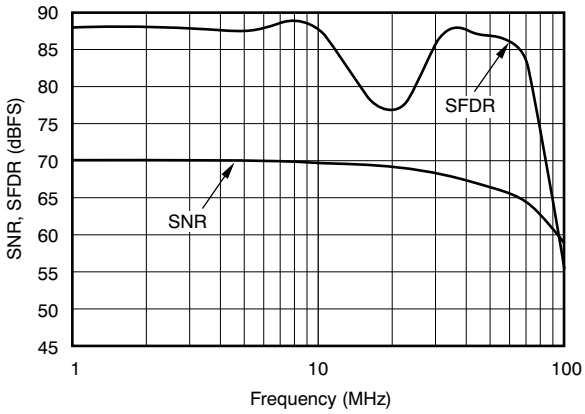


Figure 16.

DYNAMIC PERFORMANCE vs TEMPERATURE

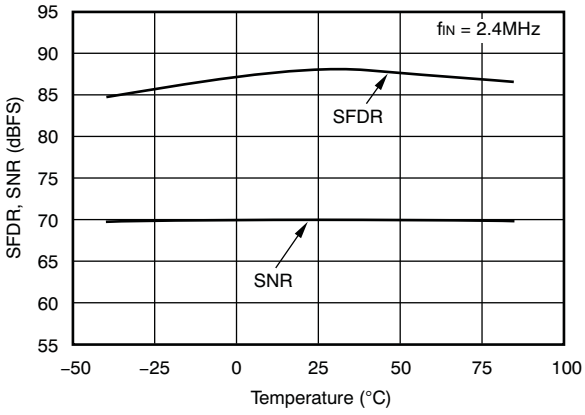


Figure 17.

DYNAMIC PERFORMANCE vs TEMPERATURE

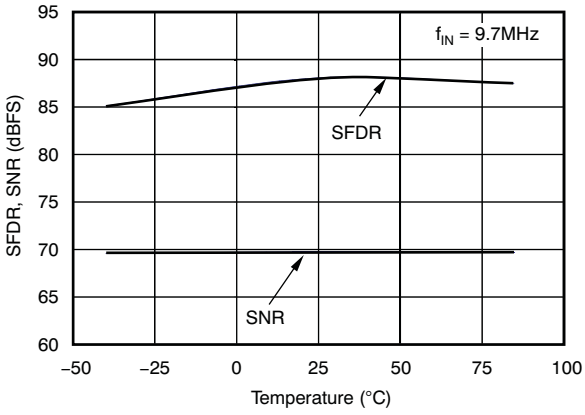


Figure 18.

TYPICAL CHARACTERISTICS: AV_{DD} = 3.3V (continued)

T_{MIN} = –40°C, T_{MAX} = +85°C. Typical values are at T_A = +25°C, sampling rate = 40MSPS, 50% clock duty cycle, AV_{DD} = 3.3V, DV_{DD} = 3.3V, VDRV = 2.5V, –1dBFS, DCA off, internal reference voltage, and $2V_{PP}$ differential input, unless otherwise noted.

OUTPUT NOISE HISTOGRAM (DC Output)

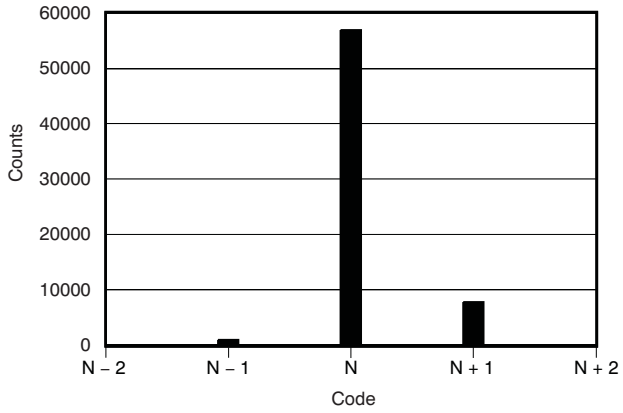


Figure 19.

APPLICATION INFORMATION

THEORY OF OPERATION

The ADS5220 is a 12-bit, 40MSPS, CMOS ADC designed with a fully differential pipeline architecture. The pipeline consists of three sections: a 3-bit quantizer, seven stages with a 1.5-bit quantizer for each stage, and a 4-bit flash. The output of each pipeline stage is processed and formed into 12-bit data in the digital error correction logic section to ensure good differential linearity of the ADC. The converter includes a high bandwidth track-and-hold amplifier in the input stage as shown in Figure 20. The falling edge of the input clock initiates the conversion process. Once the signal is captured by the input track-and-hold, the bits are sequentially encoded starting with the Most Significant Bit (MSB). This process results in a data latency of 4.5 clock cycles . The ADS5220 includes a high accuracy internal reference and also allows the use of an external reference. The input full-scale range is up to $2V_{PP}$ and is selectable based on the reference voltage setting. For normal operation, both analog inputs (IN, $\overline{IN}$) require an external common-mode voltage as a bias. The output data of the ADS5220 are available as a 12-bit parallel word, either coded in a Straight Offset Binary or Binary Two's Complement format. The ADS5220 includes an on-chip duty-cycle adjust (DCA) circuit, controlled through the state of the *Mode Select* pin (3). When activated, this duty-cycle adjust circuit can accommodate for an incoming clock duty-cycle range of 35% to 65%, and re-time it to a 50% duty-cycle, which allows for optimum internal clock timing. The ADS5220 has low power dissipation in normal mode and has two power-down modes. The device operates from a single +3.3V power supply and has a separate digital output driver supply pin.

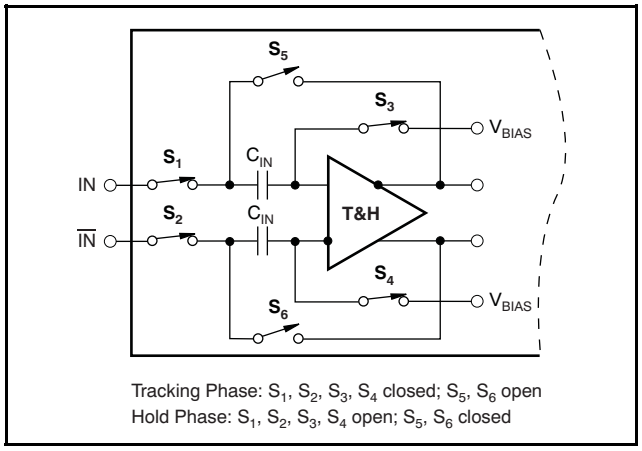


Figure 20. Simplified Circuit of Input Track-and-Hold Amplifier of ADS5220

ANALOG INPUT

Depending on the application and the desired level of performance, the analog input of the ADS5220 can be configured in various ways and driven with different circuits. In any case, the analog interface requirements should be carefully examined before selecting the appropriate circuit configuration. The circuit definition should include considerations on the input frequency band and amplitude, as well as the available power supplies.

INPUT IMPEDANCE

The input impedance of the ADS5220 is capacitive due to the input stray and sampling capacitors. These capacitors effectively result in a dynamic input impedance that is a function of the sampling and input frequency. Figure 21 depicts the differential input impedance of the ADS5220 as a function of the signal input frequency. For applications that use op amps to drive the ADC, it is recommended that a series resistor be added between the amplifier output and the converter inputs. This additional resistor isolates the capacitive input of the converter from the driving source and avoid gain peaking, or instability; furthermore, it creates a 1st-order, low-pass filter (LPF) in conjunction with the specified input capacitance of the ADS5220. The cutoff frequency of this LPF can be further adjusted by adding an external shunt capacitor. In any case, the use of the RC network is optional, but optimizing the values to adapt to the specific application is encouraged.

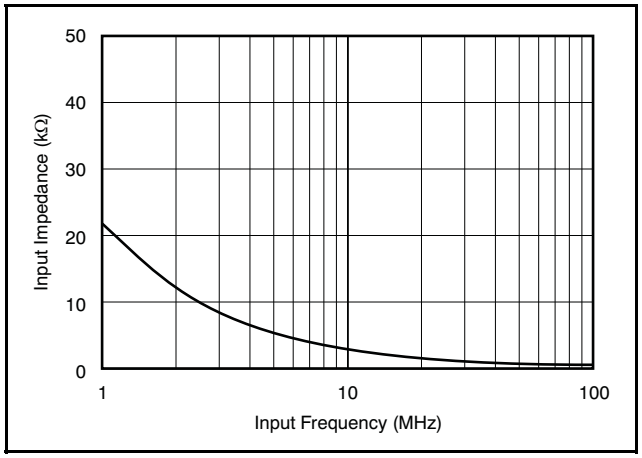


Figure 21. Differential Input Impedance vs Input Frequency

INPUT COMMON-MODE VOLTAGE

The ADS5220 operates from a single +3.3V supply, and requires an external common-mode voltage. This configuration allows a symmetrical signal swing while maintaining sufficient headroom to the supply rails. The common-mode voltage can be generated from an external DC voltage source (for example, an analog +3.3V supply with a simple resistor divider), or from the input signal source with DC-coupling. For a single-ended input configuration, the common-mode voltage is typically +1.25V. When the input configuration is differential, the common-mode voltage is +1.5V.

INPUT FULL-SCALE RANGE

The input full-scale range (FSR) of the ADS5220 is selectable from $1V_{PP}$ to $2V_{PP}$ and any value within this range, by the configuration of the reference select pin RSEL and the reference voltage pin V_{REF} (see Table 1). The input FSR (differential) is always twice V_{REF} (the voltage at the V_{REF} pin) for all reference modes.

By choosing different signal input ranges, trade-offs can be made between noise and distortion performance. For example, applications requiring the maximum signal-to-noise performance (SNR) will benefit from the $2V_{PP}$ input range while lower distortion may be obtained with the reduced input range of $1V_{PP}$. Depending on the input driver configuration the $1V_{PP}$ range may also relax the requirements for the driver, particularly for single-ended, single-supply applications.

DIFFERENTIAL INPUTS

The ADS5220 input structure is designed to accept both a single-ended or differential analog signal. However, the ADS5220 achieves its optimum performance when the analog inputs are driven differentially.

Differential operation of the ADS5220 requires that an input signal at the inputs (IN, $\overline{IN}$) has the same amplitude and is 180 degrees out-of-phase. Differential signals offer a number of advantages:

- The signal amplitude is half that required for the single-ended operation, and is therefore less demanding to achieve, while maintaining good linearity performance from the signal source.
- The reduced signal swing allows for more headroom of the interface circuitry, and therefore also allows a wider selection of the most suitable driver amplifier.
- Minimization of even-order harmonics.
- Improved noise immunity based on the common-mode input rejection of the converter.

ANALOG INPUT DRIVEN BY TRANSFORMER

The ADS5220 can be driven by a transformer, which provides signal AC-coupling and allows a signal conversion from single-ended input to differential output, or from single-ended input to single-ended output. Using a transformer offers a number of advantages. As a passive component, it does not add to the total noise and has better harmonics in wide frequency bands, compared to an op amp driver. By using a step-up transformer, further signal amplification can be realized; as a result, the signal swing from the source can be reduced. For transformer selection, it is important to carefully examine the application requirements and determine the correct model, the desired impedance ratio, and frequency characteristics. Furthermore, the appropriate model must support the targeted distortion level and should not exhibit any core saturation at full-scale voltage levels. A variety of miniature RF transformers from different manufacturers (such as Mini-Circuits, Coilcraft, or Trak) can be selected.

Figure 22 shows a transformer-coupled input configuration of the ADS5220. The ADS5220 receives a differential AC signal from the output of the transformer and common-mode voltage of +1.5V from the center tap. A source termination resistor, R_T, is required, which may be placed at the primary or secondary side of the transformer to satisfy the termination requirements of the source impedance, R_S. The circuit also shows the use of an additional RC low-pass filter placed in series with each converter input to attenuate some of the wideband noise.

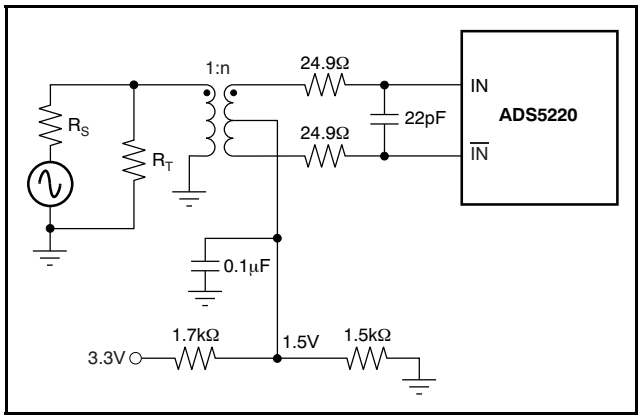


Figure 22. Transformer-Coupled Differential Input Configuration of ADS5220

The resistor values typically range from 10Ω to 50Ω, and capacitors are in the range of 10pF to 100pF for specific application requirements.

ANALOG INPUT DRIVEN BY AMPLIFIER

The ADS5220 can be driven by an operational amplifier with DC or AC signal coupling, as shown in Figure 23 and Figure 24. In Figure 23, the THS4503, a differential amplifier, is used to convert a single-ended input into a differential output with a gain of 2. The THS4503 provides an output common-mode voltage set by the V_{OCM} pin, and is DC-coupled to the input of ADS5220. A low-pass filter can be created by adding small capacitors (for example, 10pF) in parallel with the feedback resistors of the THS4503 as needed for some applications.

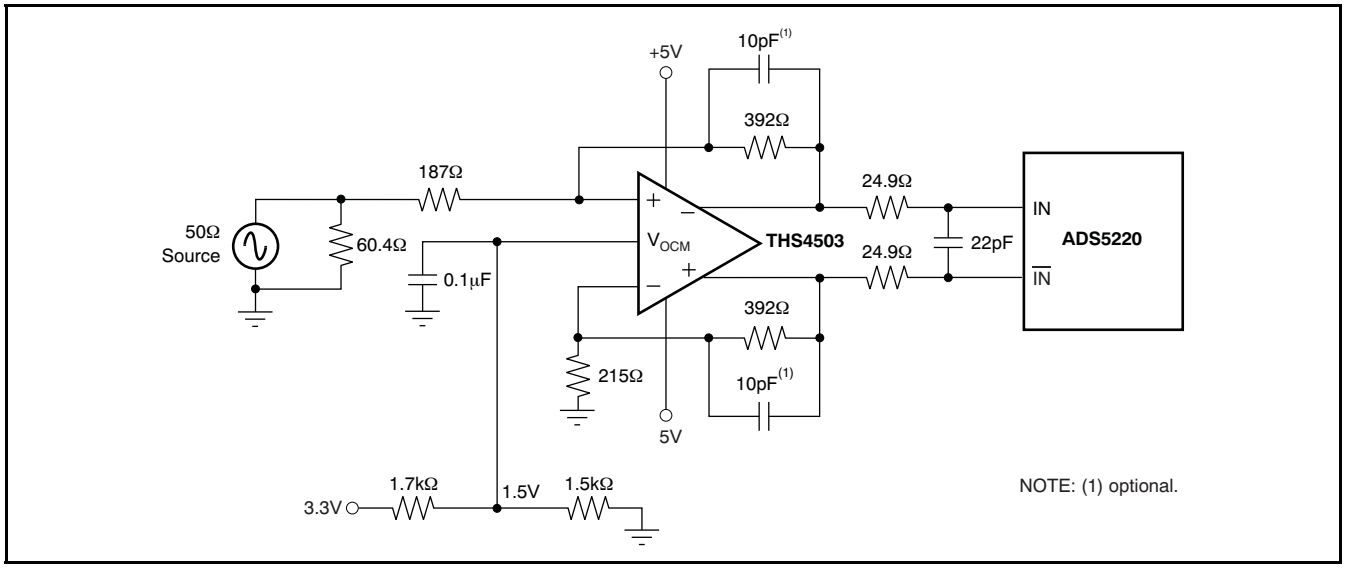


Figure 23. Using the THS4503 Differential Amplifier (Gain = 2) to Drive the ADS5220 in a DC-Coupled Configuration

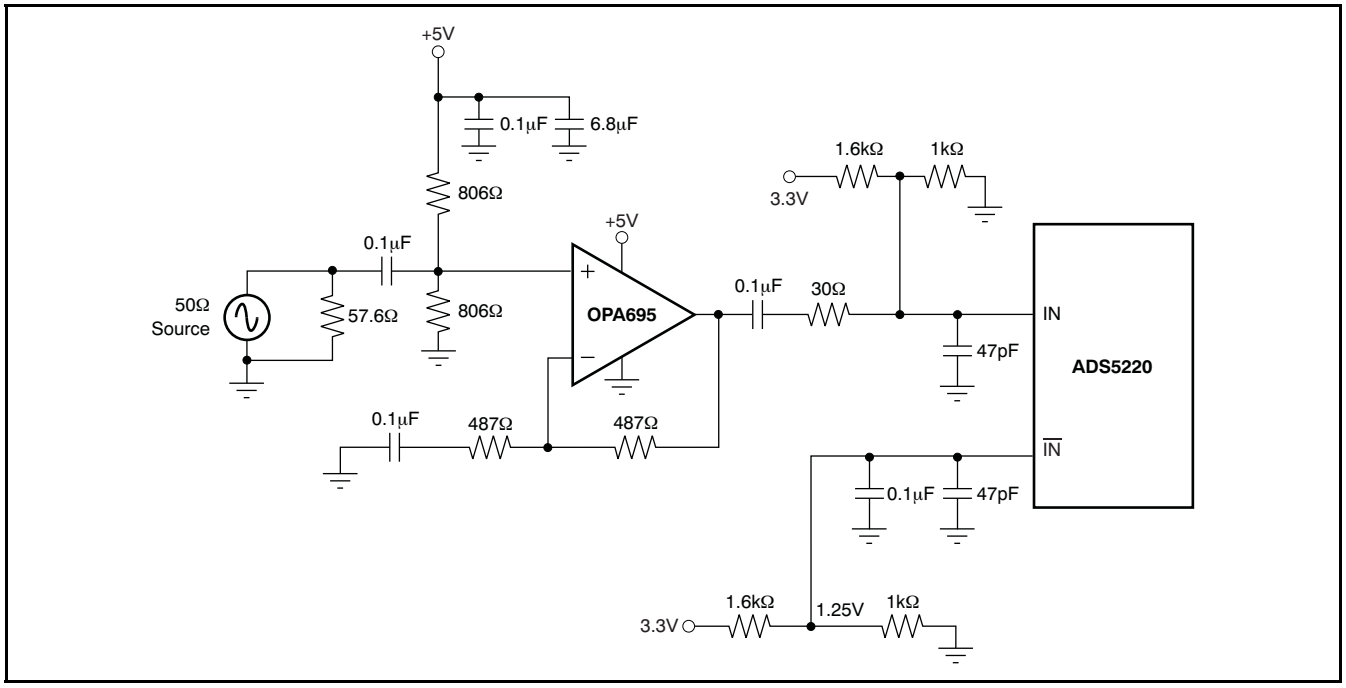


Figure 24. Single-Ended Input of ADS5220 Driven by OPA695 with Gain = 2

Due to the THS4503 driving a capacitive load, small series resistors in the output ensure stable operation. Further details of this and other functions of the THS4503 may be found in its product datasheet, located on the Texas Instruments web site (www.ti.com). In general, differential amplifiers provide a high-performance driver solution for applications that require DC signal coupling.

As shown in Figure 24, an AC-coupled, single-ended input configuration is realized with TI's OPA695 for wideband applications. For narrowband applications, the OPA2822 can be used. In Figure 24, the OPA695 is configured for a single-supply +5V and noninverting operation. The AC gain of the amplifier is 2 and the DC bias of the amplifier is +2.5V, set by the voltage divider from the op amp power supply. The OPA695 is a very high bandwidth, current-feedback op amp that combines 4200V/µs slew rate and low input voltage noise. The OPA695 high slew-rate and output drive capability can support the maximum full-scale input range of the ADS5220 up to high input frequencies.

Further details of the OPA695 can be found in the OPA695 data sheet. The common-mode voltage at the ADS5220 input is +1.25V, set by a voltage divider from +3.3V power supply. The +3.3V power supply must be decoupled, as shown in Figure 30.

CLOCK INPUT

The clock input of the ADS5220 is designed to operate with a single-ended pulse clock with CMOS/TTL level and DC-coupling. There is no external common-mode voltage requirement at the clock input pin (see Figure 25).

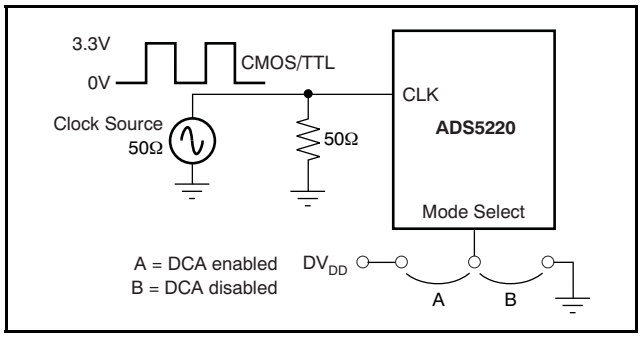


Figure 25. General Input Clock Interface of ADS5220

The clock input of the ADS5220 is referenced to the digital supply (DV_{DD}) and the applied logic levels should comply with the specified levels (LV-logic). To obtain the specified level of performance the clock signal applied to the ADS5220 should have as close to a 50% duty cycle as possible.

This clock signal is particularly important when the ADS5220 is operated at its maximum sampling rate. Since this condition cannot always easily be met, the ADS5220 features an on-chip duty-cycle adjust (DCA) circuit that allows for additional design flexibility. The function of this duty cycle adjust circuit is controlled through the *Mode Select* pin. Its default configuration is for a logic low (internal pull-down) which has the DCA circuit disabled. Applying a logic high, the DCA circuit becomes activated. Now the incoming clock duty cycle can be in the range of 35% to 65% and the DCA circuit adjusts this to be 50% for the internal timing. There may be situations where the user may prefer to disable the DCA function; for example, during asynchronous clocking (that is, when the sampling period is purposely not constant).

In any case, a very low jitter clock is fundamental to preserving the excellent AC performance of the ADS5220. Generally, as input frequency increases, clock jitter becomes more critical to maintain a good signal-to-noise ratio. The following equation can be used to calculate the achievable SNR for a given input frequency and clock jitter (t_{JA} in ps_{RMS}):

$$SNR_{JA} = 20 \log \left[1/(2 \cdot \pi \cdot f_{IN} \cdot t_{JA})\right]$$

Here, the t_{JA} is the RMS aperture jitter from all jitter sources, such as clock edge, input signal and the device. The f_{IN} is input frequency. The crystal oscillator has very low jitter, but if using a clock conditioning circuit (gate, divider, logic level converter, and so forth), the extra jitter and timing variation must be considered. In addition, the input clock is treated as an analog signal and its power supply should be separated from the power supply of the digital output driver to limit the digital noise.

MINIMUM SAMPLING RATE

The pipeline architecture of the ADS5220 uses a switched-capacitor technique in its internal track-and-hold stages. The high sampling speed necessitates the use of very small capacitor values. In order to hold droop errors low, the capacitors require a minimum refresh rate. To maintain accuracy of the acquired sample charge, the sampling clock on the ADS5220 must not drop below the specified minimum of 1MSPS.

REFERENCE

The ADS5220 provides both an internal and an external reference mode through the configuration of pins RSEL and V_{REF} (see Table 1). The input full-scale range (FSR) of the ADS5220 is always twice the voltage at the V_{REF} pin. The REFT and REFB pins are internally buffered, and drive the ADC core for both the external and internal reference modes. When the internal reference mode is selected the voltage at V_{REF} is generated by an internal 0.5V bandgap voltage through a V_{REF} amplifier. This internal buffer amplifier can be used to supply up to 2mA to external circuitry. Selecting the external reference mode powers down this reference amplifier, and the V_{REF} pin becomes the input for the external reference voltage. In the power-down mode, the impedance of the V_{REF} pin is approximately 6kΩ.

Table 1 shows the values for V_{REFT}, V_{REFB}, and V_{REF} for the various modes and full-scale input ranges.

Table 1. Reference Configuration

SELECTED MODE	RSEL PIN CONNECT TO	V_{REF} PIN (V)	INPUT FSR (V_{PP}) (Differential)	REFT (V)	REFTB (V)
Internal Fixed	GND to 0.2V	1.0	2	2	1
Internal Fixed	V_{REF} Pin	0.5	1	1.75	1.25
Internal Program	0.2V to V_{REF}	$0.5 \bullet (1 + R_2/R_1)$	$2 \bullet V_{REF}$	$V_{REF}/2 + 1.5$	$1.5 - V_{REF}/2$
External	AV_{DD} (3.3V)	Ext. 0.5V to 1V	$2 \bullet V_{REF}$	$V_{REF}/2 + 1.5$	$1.5 - V_{REF}/2$

The ADS5220 requires its reference pins to be bypassed as outlined in Figure 26 through Figure 29. The configuration remains the same for the internal or external reference modes. The bypassing should consist of two pairs of 2.2µF ceramic and 15µF tantalum capacitors, and a 10µF tantalum capacitor, as depicted in Figure 26.

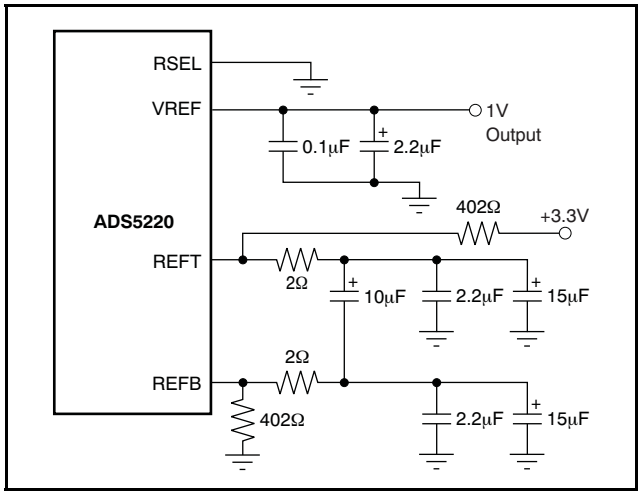


Figure 26. Internal Reference Mode for V_{REF} = 1V

In addition to the bypassing the top reference and bottom reference pins (REFT, REFB) also require a pull-up and a pull-down resistor, respectively. As shown in Figure 26, the pull-up resistor should be connected from the REFT pin to the analog supply (+3.3V AV_{DD}), while the pull-down resistor on the REFB pin should be connected to ground. For proper operation the value of those resistors should be maintained as shown, that is, 402Ω. Also, to ensure optimal settling of the internal reference amplifiers, the external configuration must include two low value resistors located in series with each of the REFT and REFB pins (see Figure 26). For best results, use small surface mount chip resistors and position them as close to the pins as possible.

Internal Reference

There are two internal fixed reference modes and one internal programmable reference mode as shown in Table 1 and Figure 26 through Figure 28. Setting RSEL to ground (or < 0.2V) provides an internal reference voltage of +1.0V at pin V_{REF}, +2V at pin REFT, and +1V at pin REFB. In this case, the input FSR is +2V peak-to-peak.

Connecting RSEL to the V_{REF} pin provides an internal reference voltage of +0.5V at V_{REF}, +1.75V at REFT, and +1.25V at REFB. In this case, the input FSR is +1V peak-to-peak. Setting the resistor divider as in Figure 28 provides an internal voltage between +0.5V and +1V at V_{REF}, which is as follows:

$$V_{REF} = 0.5 \cdot (1 + R_2/R_1)$$

In this case, the voltage at REFT and REFB and input FSR is calculated based on Table 1.

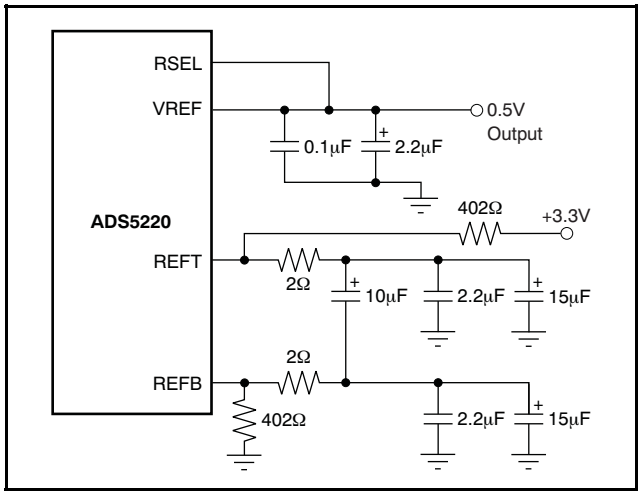


Figure 27. Internal Reference Mode for V_{REF} = 0.5V

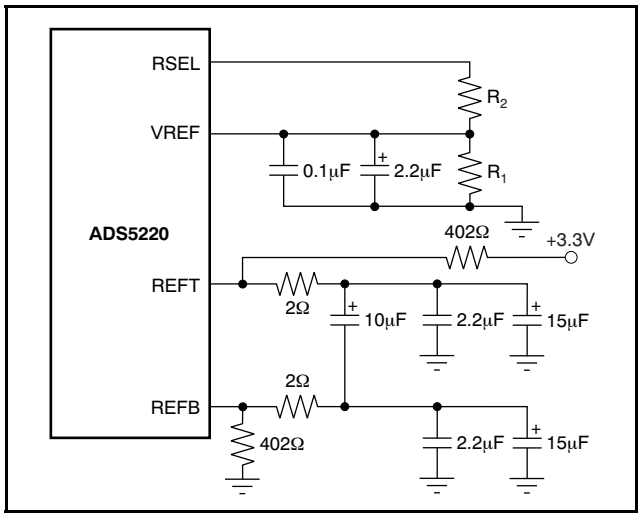


Figure 28. Internal Reference for $V_{REF} = 0.5 \bullet (1 + R_2/R_1)$

External Reference

For even more design flexibility, the ADS5220 can be operated with external references (see Figure 29). Utilization of an external reference voltage may be considered for applications requiring higher accuracy, improved temperature stability, or flexible full-scale range. Particularly in multi-channel applications, the use of a common external reference offers the benefit of improving gain matching between converters. Setting RSEL to AV_{DD} (+3.3V) provides an external reference mode for the ADS5220. In this case, the internal V_{REF} amplifier is powered down, and the V_{REF} pin requires an external reference voltage between +0.5V to +1V to provide an input full-scale range of $1V_{PP}$ to $2V_{PP}$. The REFT and REFB appear with the voltage as shown in Table 1, and input FSR is always twice the voltage at the V_{REF} pin. A voltage reference (REF1004 or TPS79225) and a single-supply amplifier (OPA2234 or OPA4227) can be used to generate a precision external reference.

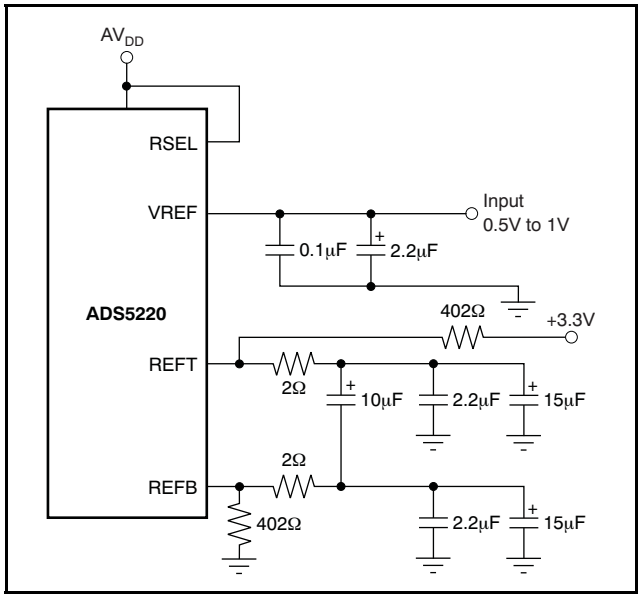


Figure 29. External Reference Configuration

DIGITAL OUTPUTS

Data Output Format

The ADS5220 makes two data output formats available, either the Straight Offset Binary (SOB) code or the Binary Two's Complement (BTC) code. The selection of the output coding is controlled through the MSBI pin. Applying a logic high will enable the BTC coding, whereas a logic low will enable the SOB code. In its default configurations the MSBI pin assumes a logic low level (internal pull-down) and the ADS5220 operates with the SOB output coding. The two code structures are identical with one exception: the MSB is inverted for the BTC format, as shown in Table 2. If the input signal exceeds the FSR, the output code will remain at all 1s or all 0s.

Table 2. Coding Table for Differential Input Configuration with FSR of $2V_{PP}$

DIFFERENTIAL INPUT	STRAIGHT OFFSET BINARY (SOB)	BINARY TWO'S COMPLEMENT (BTC)
+FS – 1LSB (+FS: IN = 2V, $\overline{IN}$ = 1V)	1111 1111 1111	0111 1111 1111
+1/2 FS (IN = 1.75V, $\overline{IN}$ = 1.25V)	1100 0000 0000	0100 0000 0000
Bipolar Zero (IN = $\overline{IN}$ = 1.5V)	1000 0000 0000	0000 0000 0000
–1/2 FS ($\overline{IN}$ = 1.75V, IN = 1.25V)	0100 0000 0000	1100 0000 0000
–FS ($\overline{IN}$ = 2V, IN = 1V)	0000 0000 0000	1000 0000 0000

Output Enable ($\overline{OE}$)

The digital outputs including the OVR pin of the ADS5220 can be set to output enable or output high impedance (tri-state) by the $\overline{OE}$ pin. For normal operation, this pin must be at a logic low (default is internal pull-down), whereas a logic high disables the outputs or sets the output tri-state.

Output Loading

It is recommended to keep the capacitive loading on the data output lines as low as possible, preferably below 10pF. Higher capacitive loading causes larger dynamic currents as the digital outputs are changing. These high current surges can feed back to the analog portion of the ADC and adversely affect device performance. If necessary, external buffers or latches (for example, the SN74LVTH16374) close to the converter output pins can be used to minimize capacitive loading. Buffers or latches also provide the added benefit of isolating the ADS5220 from any digital activities on the bus to limit the high-frequency noise.

Over-Range Indicator

The ADS5220 has control functions for the input voltage over full-scale that includes output data code control and over-range indication. The output data code control of over full-scale is shown in Table 2. In SOB format, for example, when the input voltage is (+FS – 1 LSB) or above this value, the ADS5220 outputs all 1s at 12 data bits; when the input voltage is –FS or below this value, the ADS5220 outputs all 0s at 12 data bits. When the input voltage is 0 (mid-scale) or only the common-mode voltage at the input, the ADS5220 outputs 1 at MSB and 0s at the remaining 11 data bits. Another over-range control

function of the ADS5220 is over-range indication, which is output by the OVR pin. The OVR pin is the function of the reference voltage and the output data bits, and has the same pipeline delay as the output data bits. OVR is at logic low if the input voltage is within the FSR, and is at logic high if the input voltage is over full-scale or under full-scale. OVR changes from logic low to high or logic high to low immediately following the change of the output data, when the input voltage changes from normal value to over FS or from over FS to normal value. The OVR signal remains high for as long as the input signal exceeds the input range limits of the ADS5220. The OVR pin is tri-stated by the use of the output enable pin ($\overline{OE}$).

Timing

The ADS5220 samples the analog signal at the falling edge of its input clock, and outputs the digital data at the rising edge of the input clock after a pipeline delay of 4.5 clocks . There is an aperture delay (typically 3ns) between the sampling edge and the actual sampling time.

There is also a propagation delay between the rising edge of the clock and the time that data is valid on the data bus (see the Timing Diagram). The output data of the ADS5220 is latched data.

POWER SUPPLIES AND POWER DISSIPATION

Analog and Digital Power Supplies

The ADS5220 includes power-supply pins of AV_{DD}, DV_{DD} and VDRV. The analog supply AV_{DD} and digital supply DV_{DD} is +3.3V. The digital output driver supply, VDRV, can be set between +2.5V and +3.3V. AV_{DD}, DV_{DD} and VDRV are not tied together internally. Each of these supply pins must be bypassed separately with at least one 0.1µF ceramic chip capacitor. The analog supply (AV_{DD}) and the digital supply (DV_{DD} or VDRV) may be tied together externally with a ferrite bead or inductor between the supply pins. The ADS5220 is specified with the digital output driver supply, VDRV, set to +2.5V.

It is highly recommended to consider linear supplies instead of switching types. Even with good filtering, switching supplies can radiate noise that could interfere with any high-frequency input signal and cause unwanted modulation products. The supply voltage should stay within the tolerance given in the Electrical Characteristics table. A basic application configuration with the power-supply decoupling is shown in Figure 30.

Power Dissipation

In normal operating mode (STPD = low and QPD = low), the typical total power dissipation of the ADS5220 is 195mW. The majority of the power consumption is a result of biasing; therefore, this part of the total power dissipation is independent of the applied clock frequency. The current on the VDRV supply is directly related to the capacitive loading of the data output pins; care must be taken to minimize such loading.

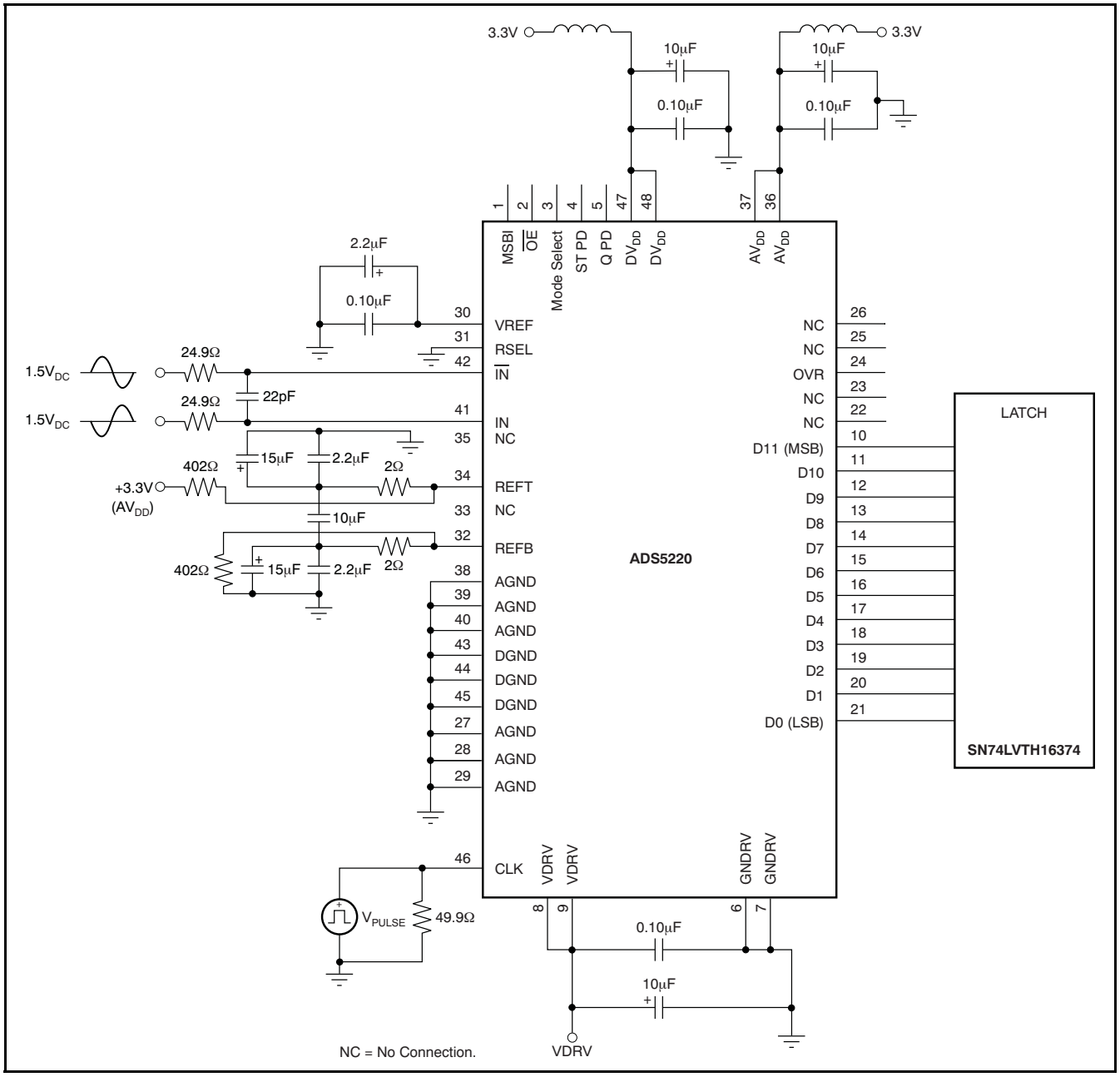


Figure 30. General Configuration for the ADS5220

Power Down

The ADS5220 provides two power-down modes for different application requirements. One is the Standard Power-Down (STPD); the second is the Quasi-Power-Down (QPD). Both pins will assume a logic low level (internal pull-down) and configure the ADS5220 for normal operation. Setting STPD to logic high (and QPD to logic low or high) shuts down the internal ADC core and power down the reference circuit. In this case the power dissipation is typically 15mW. With 10µF external decoupling capacitor at REFT and REFB, it takes about 800µs to fully restore normal operation after the normal mode is enabled. Setting QPD to logic high (and STPD to logic low) shuts down the internal ADC core while the internal reference circuit power remains on. In this case, power dissipation is typically 75mW. It takes about 2µs to fully restore normal operation after the normal mode is enabled. During power-down, data in the converter pipeline will be lost and new valid data is subject to the specified pipeline delay.

LAYOUT AND DECOUPLING

Proper grounding and bypassing, short lead length, and the use of ground planes are particularly important for highfrequency designs. Achieving optimum performance with a fast sampling converter like the ADS5220 requires careful attention to the printed circuit board (PCB) layout in order to minimize the effect of board parasitics and optimize component placement. A multi-layer board usually ensures best results and allows convenient component placement. The ADS5220 must be treated as an analog component, and the AV_{DD} pins connected to a clean analog supply. This configuration ensures the most consistent results, because digital supplies often carry a high level of switching noise that could couple into the converter and degrade the performance. The driver supply pins (VDRV) must also be connected to a low-noise supply. Supplies of adjacent digital circuits can carry substantial current transients. The supply voltage must be thoroughly filtered before connecting to the VDRV supply of the converter. All ground connections on the ADS5220 are internally bonded to the metal flag (bottom of package) that forms a large ground plane. All ground pins must directly connect to an analog ground plane that covers the PCB area under the converter. As a result of its high sampling frequency, the ADS5220 generates high-frequency current transients and noise (clock feedthrough) that are fed back into the supply and reference lines. If not sufficiently bypassed, this adds noise to the conversion process. See Figure 30 for the recommended supply decoupling scheme for the ADS5220. All AVDD pins should be bypassed with a combination of 0.1µF ceramic chip capacitors (0805, low ESR) and a 10µF tantalum tank capacitor. A similar approach may be used on the digital supply pins DVDD and driver supply pins, VDRV. In order to minimize the lead and trace inductance, the capacitors must be located as close to the supply pins as possible. They are best placed directly under the package where double-sided component mounting is allowed. In addition, larger bipolar decoupling capacitors (2.2µF to 10µF), effective at lower frequencies, may also be used on the main supply pins. They can be placed on the PCB in close proximity (< 0.5 inches) to the ADC. If the analog inputs to the ADS5220 are driven differentially, it is especially important to optimize towards a highly symmetrical layout. Small trace length differences can create phase shifts compromising a good distortion performance. For this reason, the use of two single op amps rather than one dual amplifier enables a more symmetrical layout and a better match of parasitic capacitances. The pin orientation of the ADS5220 package follows a flow-through design with the analog inputs located on one side of the package, whereas the digital outputs are located on the opposite side of the quad-flat package. This configuration provides a good physical isolation between the analog and digital connections. While designing the layout, it is important to keep the analog signal traces separated from any digital lines to prevent noise coupling onto the analog portion. Try to match trace length for the differential clock signal (if used) to avoid mismatches in propagation delays. Single-ended clock lines must be short and should not cross any other signal traces. Short circuit traces on the digital outputs minimize capacitive loading. Trace length must be kept short to the receiving gate (< 2 inches) with only one CMOS gate connected to one digital output. If possible, the digital data outputs should be buffered (with the TI SN74LVTH16374, for example). Dynamic performance can also be improved with the insertion of series resistors at each data output line. This sets a defined time constant and reduces the slew rate that would otherwise flow as the fast edge rate. The resistor value may be chosen to give a time constant of 15% to 25% of the used data.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from C Revision (May 2006) to D Revision **Page**

- Changed document format to XML 1
- Changed Data Latency from 5 to 4.5 clock cycles 3
- Changed Timing Diagram 7
- Changed Timing Characteristics table 7
- Changed from "eight middle" to "seven" stages in *Theory of Operation* section (regarding pipeline sections) 11
- Changed from "rising" to "falling" edge in *Theory of Operation* section (regarding initiation of conversion) 11
- Changed from "5" to "4.5" clock cycles in *Theory of Operation* section (regarding data latency) 11
- Changed Figure 21. Corrected grid lines and X,Y axes. 12
- Changed from "rising" to "falling" edge in *Timing* section (regarding analog signal sampling) 18
- Changed from "5" to "4.5" clocks in *Timing* section (regarding pipeline delay) 18

Changes from B Revision (March 2005) to C Revision **Page**

- Changed device ordering number. 2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
ADS5220PFBT	NRND	TQFP	PFB	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
ADS5220PFBTG4	NRND	TQFP	PFB	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
ADS5221PFBT	NRND	TQFP	PFB	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ADS5221PFBTG4	NRND	TQFP	PFB	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

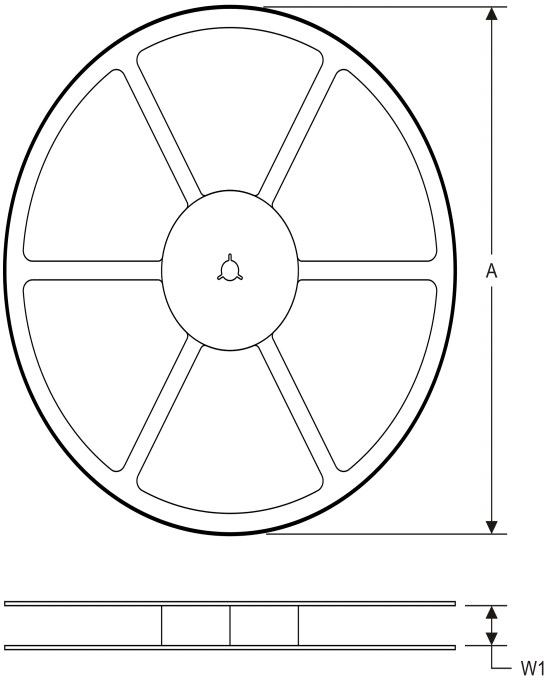
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

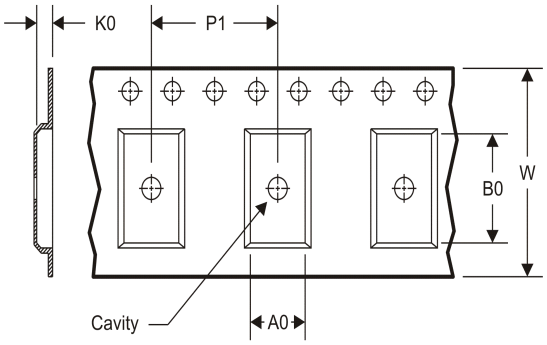
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



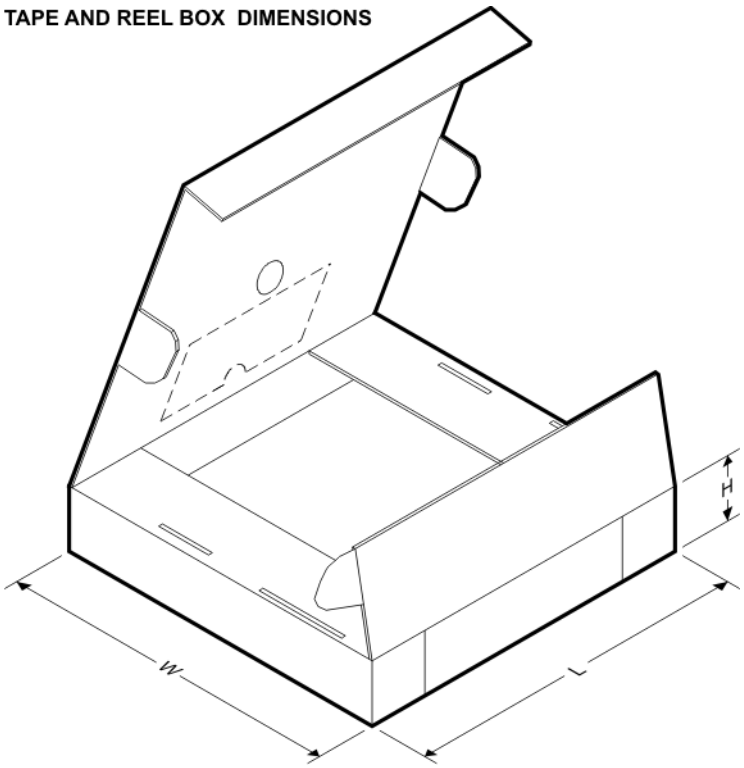
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS5220PFBT	TQFP	PFB	48	250	177.8	16.4	9.6	9.6	1.5	12.0	16.0	Q2
ADS5221PFBT	TQFP	PFB	48	250	177.8	16.4	9.6	9.6	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS

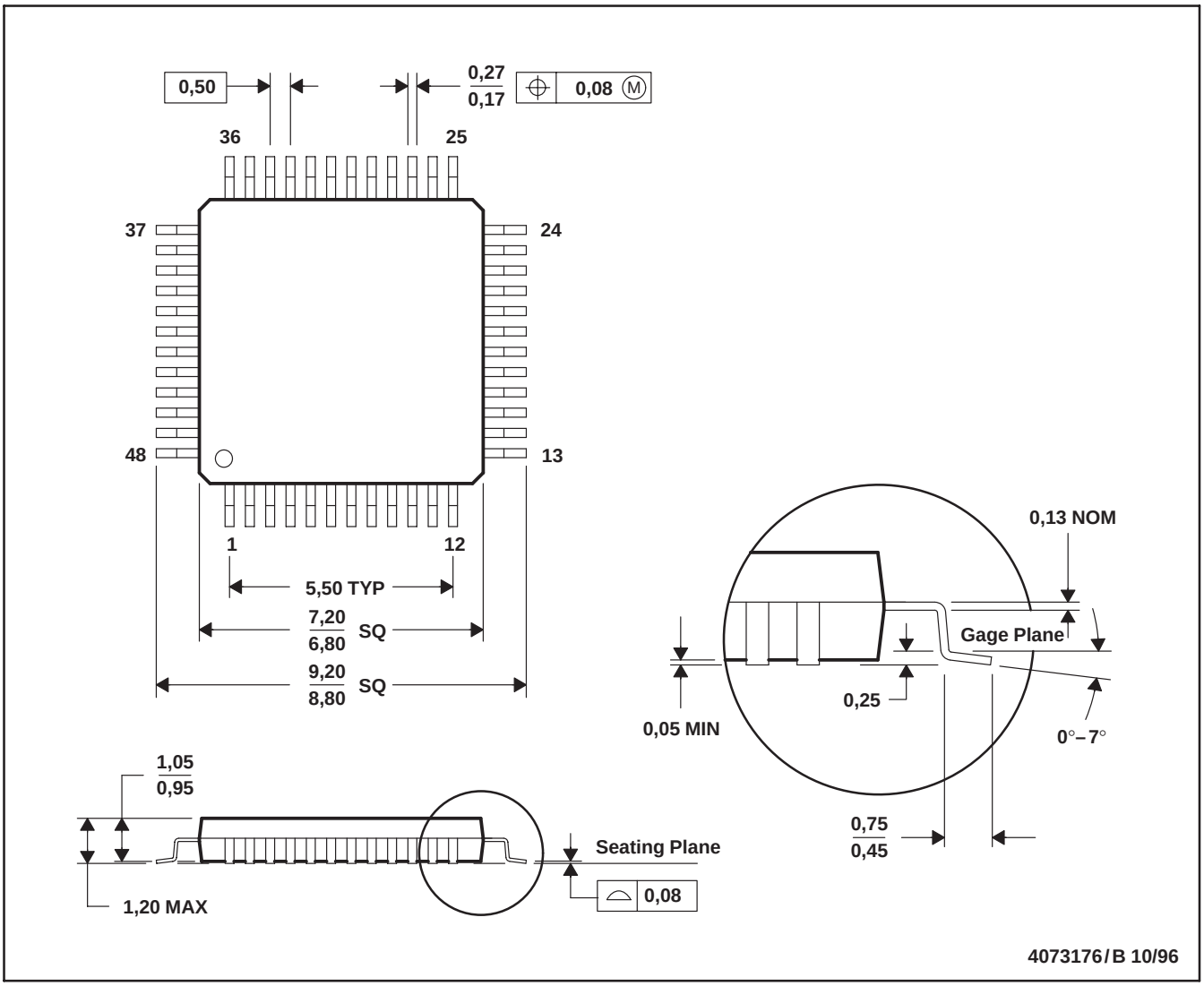


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS5220PFBT	TQFP	PFB	48	250	210.0	185.0	35.0
ADS5221PFBT	TQFP	PFB	48	250	210.0	185.0	35.0

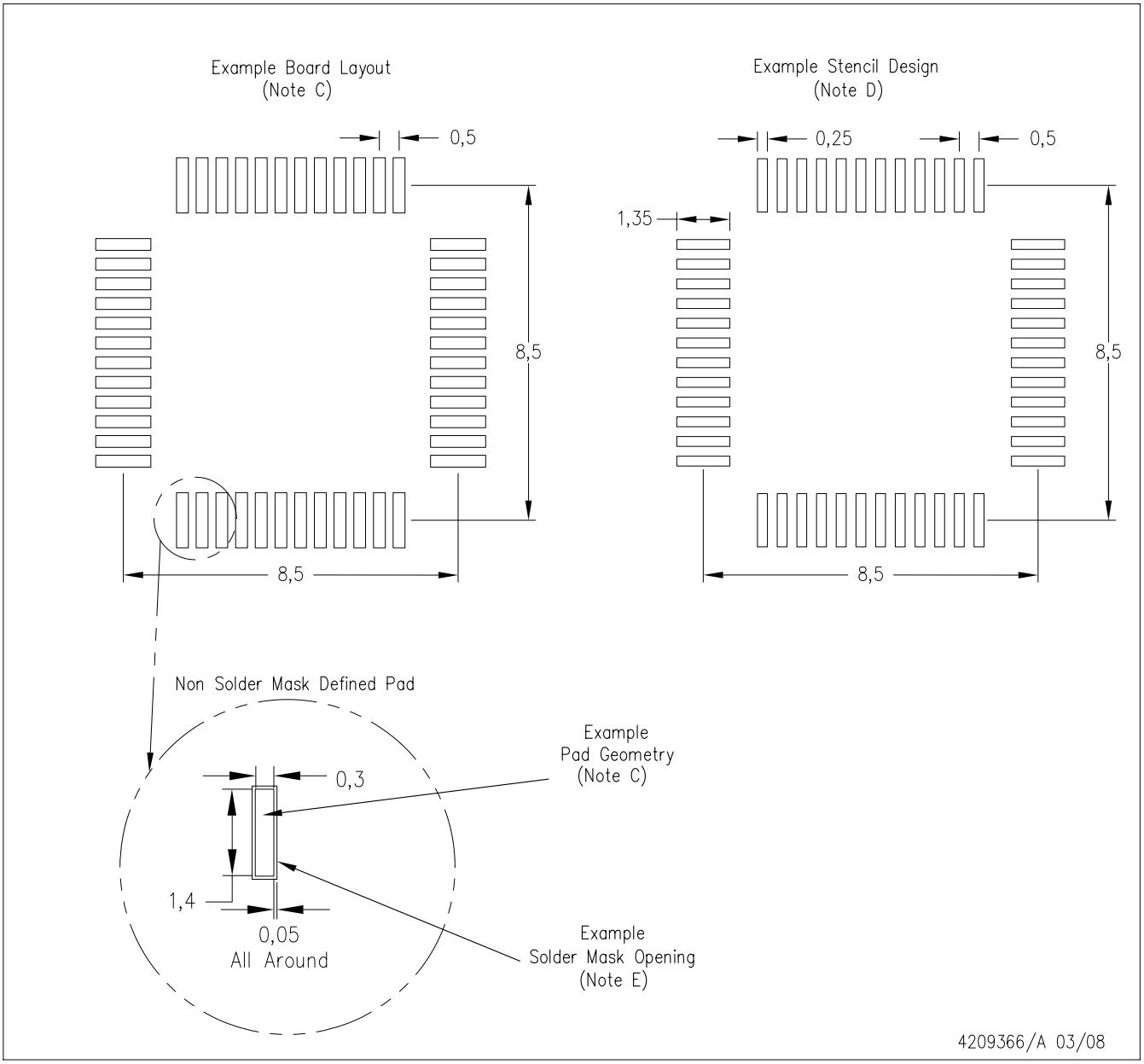
MTQF019A – JANUARY 1995 – REVISED JANUARY 1998

PFB (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

PFB (S–PQFP–G48)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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