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SHORT CYCLING THE 8-PIN ADS78xx FAMILY

By Bonnie C. Baker

The most recent 8-pin, 12-bit A/D converters that Burr-Brown has introduced to the market are advertised as high speed, micro power, low priced sampling SAR devices. During product development and the initial introduction period, the engineering effort was placed on optimizing the combination of 12 bits with high speed, low power and low cost. Burr-Brown Applications has revisited these converters to find that the claims of high speed and micro power at 12 bits are only part of the story. If power savings is a priority and fewer bits are tolerable in the application, these parts can be operated at much higher speeds and with considerably lower power dissipation. The products that are discussed in this application note are the ADS7816, ADS7817 and ADS7822 (Figure 1).

The data sheet key specifications for these products are shown in Table I. The maximum through-put rate stated in Table I assumes that the devices operate at that speed with less error than stated in the maximum linearity error specifications. This is, of course, in a 12-bit system. The differentiating specifications between these three products are speed, power, and supply voltage. As shown in Table I, the power dissipation of the ADS7816 at a 200kHz continuous sampling rate is 1.9mW. If the application allows for a conservative 16 clock cycles to complete the conversion, the clock rate for the ADS7816 and ADS7817 would be 3.2MHz and for the ADS7822, 1.2MHz.

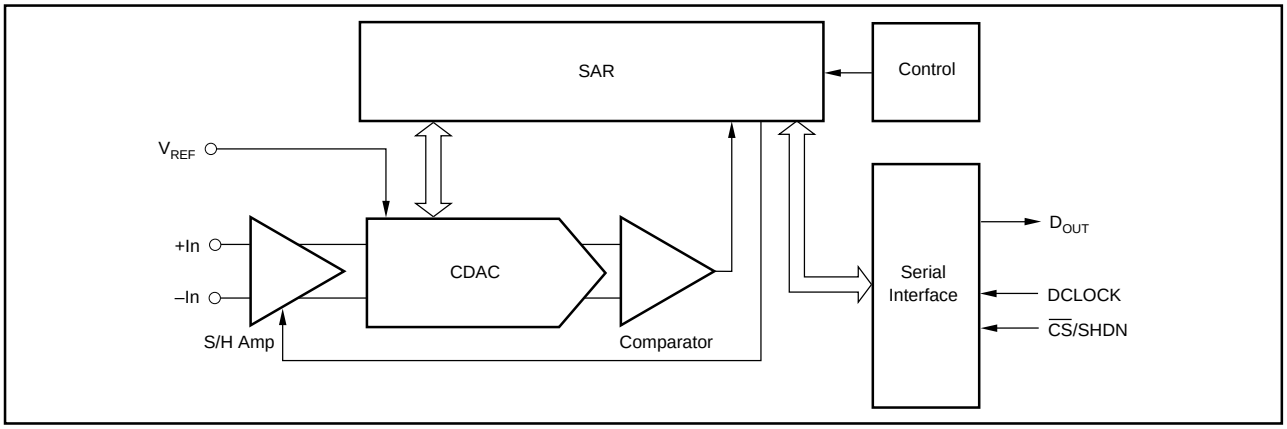

Figure 1. The Basic Topology of the ADS7816, ADS7817, and ADS7822 is Shown in this Figure. All three devices are 12-bit, 8-pin, SAR converters with serial outputs.

	ADS7817C (V_{REF} = 2.5V)	ADS7816C (V_{REF} = 5V)	ADS7822C (V_{REF} = 3V)
Maximum Through-put Rate, $1/t_{CYC}$	200kHz	200kHz	75kHz
Maximum system clock rate assuming 16 clocks for one conversion plus data transfer	3.2MHz	3.2MHz	1.2MHz
Typical Power Dissipation at Specified Through-put Rate	2.3mW	1.9mW	0.54mW
Maximum Integral Linearity Error	±1LSB	±1LSB	±0.75LSB
Maximum Differential Linearity Error	±1LSB	±0.75LSB	±0.75LSB
Power Supply for above Specifications	5.0V	5.0V	2.7V
Input Structure	Fully Differential	Single-Ended with Sampled Ground Sense	Single-Ended with Sampled Ground Sense

TABLE I. Published Specifications of Three of the 12-Bit, Micro-power, Sampling A/D Converters.

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All three devices communicate with a processor by way of a synchronous 3-wire interface. The basic timing diagrams for these A/D converters is shown in Figures 2 and 3. As shown in Figure 2, a falling $\overline{CS}$ signal initiates the conversion process. This is usually synchronized with the falling edge of the system clock (DCLOCK). The first 1.5 to 2 clock periods after $\overline{CS}$ falls are used to sample the analog input signal. Following this sampling time, the converter transmits one null bit and then the 12 bits of the conversion, starting with the MSB. At the end of the transmission of these 12 bits and with the falling edge of the system clock, $\overline{CS}$ is brought high. A high $\overline{CS}$ also puts the DOUT pin into high impedance mode. $\overline{CS}$ must be kept high for at least one clock cycle, thus completing one conversion/data transfer cycle. The power down mode is initiated by the converter with the transmission of the last bit or the LSB. If $\overline{CS}$ is kept high, the device will remain in the power down mode until $\overline{CS}$ goes low, as described above.

The power down mode can be used to conserve over all power. To illustrate this point the ADS7816 is used as an example. If the desired conversion rate for the application is 20kHz, the clock rate can be set to a minimum of 320kHz (for 12-bit operation) or a maximum of 3.2MHz. In the case where the clock is set to 320kHz, the converter is powered for most of the conversion cycle ($1/t_{CYC}$). In this case, the power dissipation of a typical ADS7816 would be 1.425mW. In contrast, the clock can be set at its maximum rate of 3.2MHz. A 20kHz conversion rate is obtained by sending "bursts" of 16 clock cycles to the converter every 50µs. These bursts put the A/D converter in its fully powered state for 5µs and in the power down mode for 45µs (assuming that $\overline{CS}$ is kept high during the 45µs). Now the power dissipation of the ADS7816 will be a typical of 210µW. This improvement in power dissipation is very effective in battery power applications.

SHORT CYCLING USING OUTPUT DATA TRUNCATION TECHNIQUES

The timing process described above should be implemented if a full 12 bits of the serial data out is required. In instances where fewer bits are acceptable, such as 10 bits or 8 bits, the transmission of the data on the D_{OUT} pin can be terminated by prematurely by bringing $\overline{CS}$ high. When $\overline{CS}$ is brought high prematurely, the transmission of the serial data from the A/D converter will stop and D_{OUT} will go into a high impedance mode. An example of the timing for 8-bit

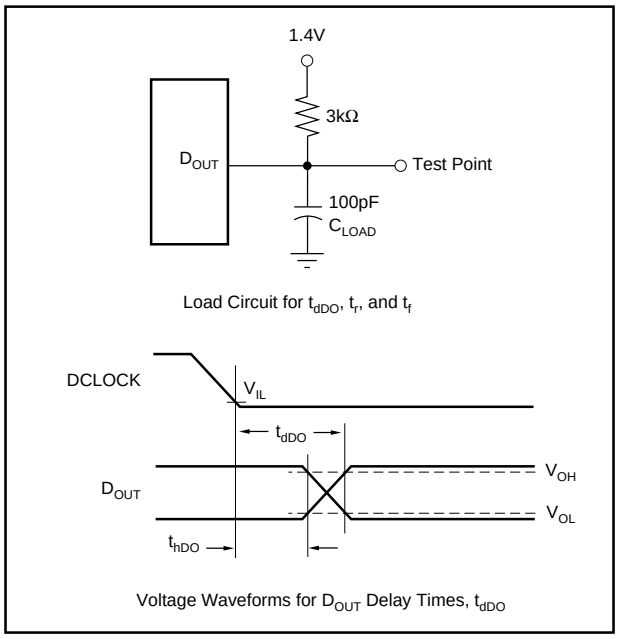


FIGURE 3. The Timing Relationship Between DCLOCK and the Serial Data Output at D_{OUT} of the Converters is Shown Here. V_{IL} and V_{OL} is defined at 10% above logic low, V_{OH} is defined at 10% below logic high.

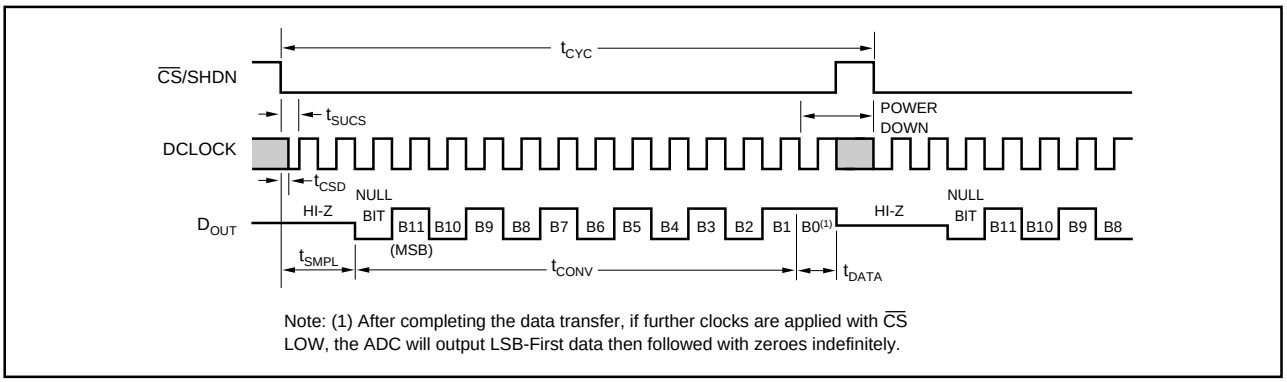


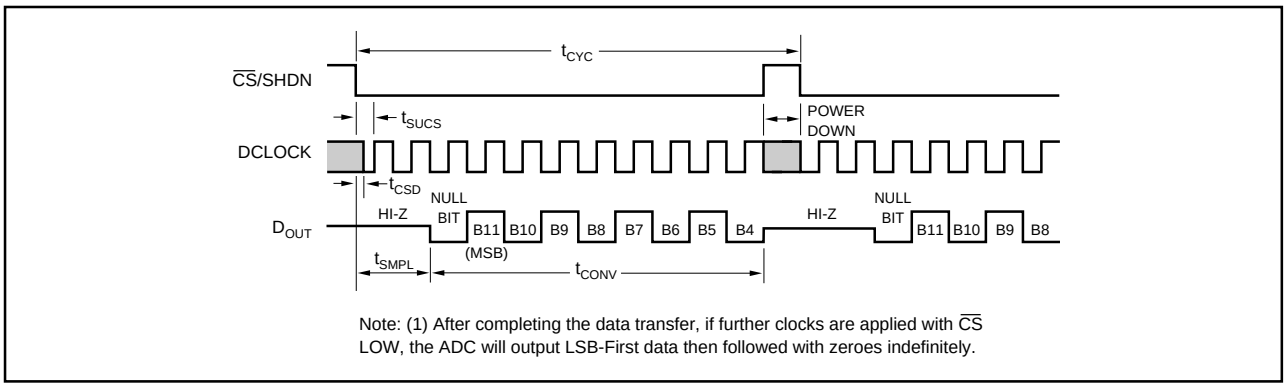
FIGURE 2. The Standard Timing Diagram for the ADS7816, ADS7817, and ADS7822 is Shown Here. In this figure $\overline{CS}$ and the transfer of the D_{OUT} to the processor is initiated by the falling edge of DCLOCK.

operation is shown in Figure 4. This technique, known as short cycling, can be used to increase the through-put rate or reduce the average power dissipation. A comparison of data rate versus power dissipation of the ADS7817 is shown in Figure 5. In this diagram, the clock rate is kept constant at 3.2MHz. The data rate of the converter is adjusted by extending the amount of time that the device is in its power down mode, implemented by making $\overline{CS}$ high. This simple technique of short cycling does not compromise the 12-bit performance of the converter, it simply terminates the transmission of bits. Consequently, performance specifications such as INL, DNL, THD and SNR are not degraded. This technique is briefly discussed in the data sheet for each product.

The limiting factor for the maximum data rate of these converters (regardless of the number of bits actually latched) is the set-up and hold times of D_{OUT}. This is most effectively shown in the timing diagram in Figure 3. The specification of particular interest is t_{dDO}, the "DCLOCK falling to next D_{OUT} valid" specification. In the case of the ADS7816 and ADS7817, the maximum (over full temperature range) t_{dDO} is equal to 150ns. Given that the processor will latch the data in on the rising edge of the clock, the output data of the converter must be valid at the time of the clock rising edge. This limits the maximum clock rate to $(1 / (2 \cdot t_{dDO}))$ or 3.33MHz. For these devices, 3.2MHz was conservatively specified as the clock rate.

CONCLUSION

If only 8 or 10 bits are required from the A/D converter the ADS7822, ADS7816 and ADS7817 serial output data can be truncated to the desired number of bits. This allows for a lower overall conversion time because fewer clock cycles are used to produce the desired number of output bits. In the case of a 10-bit conversion 14 clock cycles are required for the conversion. In the case of 8 bits, 12 clock cycles are required. This technique offers an opportunity to lower the overall power dissipation by approximately 12.5% for 10 bits and 25% for 8 bits for the same throughput rate.



Note: (1) After completing the data transfer, if further clocks are applied with $\overline{CS}$ LOW, the ADC will output LSB-First data then followed with zeroes indefinitely.

FIGURE 4. These A/D Converters can be Short Cycled by Bringing $\overline{CS}$ High Prematurely. All serial output data is halted at that time. This timing diagram illustrates the performance of the ADS7816, ADS7817, and ADS7822 being utilized as 8-bit converters.

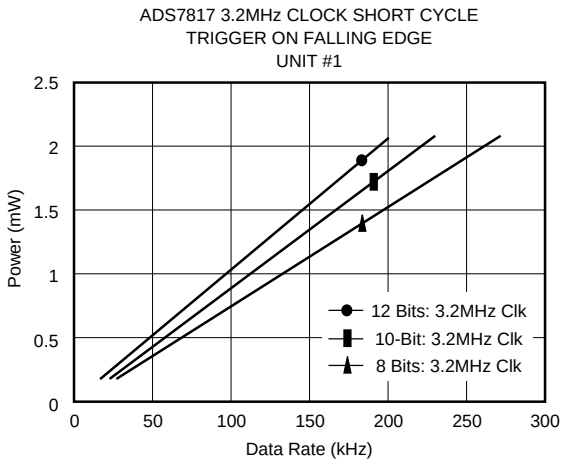


FIGURE 5. Using the ADS7817 as a Example, the Timing Technique Illustrated in Figure 4 is Used to Short Cycle the Device to 10 Bits and 8 Bits. Note that in all examples the system clock, DCLOCK, is kept at 3.2MHz.

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