

8 k × 8 NONVOLATILE SRAM (5 V, 3.3 V)

FEATURES

- Data Retention for at least 10 Years Without Power
- Automatic Write-Protection During Power-up/Power-down Cycles
- Conventional SRAM Operation, Including Unlimited Write Cycles
- Internal Isolation of Battery before Power Application
- 5-V or 3.3-V Operation
- Industry Standard 28-Pin DIP Pinout

GENERAL DESCRIPTION

The CMOS bq4010/Y/LY is a nonvolatile 65,536-bit static RAM organized as 8,192 words by 8 bits. The integral control circuitry and lithium energy source provide reliable nonvolatility coupled with the unlimited write cycles of standard SRAM.

The control circuitry constantly monitors the single supply for an out-of-tolerance condition. When V_{CC} falls out of tolerance, the SRAM is unconditionally write-protected to prevent an inadvertent write operation.

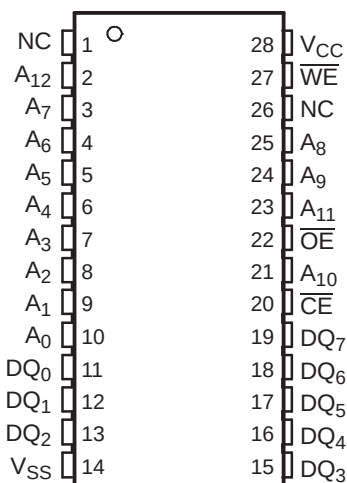
At this time the integral energy source is switched on to sustain the memory until after V_{CC} returns valid.

The bq4010/Y/LY uses extremely low standby current CMOS SRAMs, coupled with small lithium coin cells to provide nonvolatility without long write-cycle times and the write-cycle limitations associated with EEPROM.

The bq4010/Y/LY requires no external circuitry and is compatible with the industry-standard 64-Kb SRAM pinout.

PIN CONNECTIONS

28-Pin DIP Module
(TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

DEVICE INFORMATION**Table 1. TERMINAL FUNCTIONS**

TERMINAL		I/O	DESCRIPTION
NAME	NUMBER		
A ₀	10	I	Address inputs
A ₁	9	I	
A ₂	8	I	
A ₃	7	I	
A ₄	6	I	
A ₅	5	I	
A ₆	4	I	
A ₇	3	I	
A ₈	25	I	
A ₉	24	I	
A ₁₀	21	I	
A ₁₁	23	I	
A ₁₂	2	I	
$\overline{CE}$	20	I	Chip-enable input
DQ ₀	11	I/O	Data input/output
DQ ₁	12	I/O	
DQ ₂	13	I/O	
DQ ₃	15	I/O	
DQ ₄	16	I/O	
DQ ₅	17	I/O	
DQ ₆	18	I/O	
DQ ₇	19	I/O	
NC	1	-	No connect
	26		
$\overline{OE}$	22	I	Output enable input
V _{CC}	28	I	Supply voltage input
V _{SS}	14	-	Ground
$\overline{WE}$	27	I	Write enable input

FUNCTIONAL DESCRIPTION

When power is valid, the bq4010/Y/LY operates as a standard CMOS SRAM. During power-down and power-up cycles, the bq4010/Y/LY acts as a nonvolatile memory, automatically protecting and preserving the memory contents.

Power-down/power-up control circuitry constantly monitors the V_{CC} supply for a power-fail-detect threshold V_{PFD}. The bq4010 monitors for V_{PFD} = 4.62 V typical for use in 5-V systems with 5% supply tolerance. The bq4010Y monitors for V_{PFD} = 4.37 V typical for use in 5-V systems with 10% supply tolerance. The bq4010LY monitors for V_{PFD} = 2.90 V (typ) for use in 3.3-V systems.

When V_{CC} falls below the V_{PFD} threshold, the SRAM automatically write-protects the data. All outputs become high impedance, and all inputs are treated as *don't care*. If a valid access is in process at the time of power-fail detection, the memory cycle continues to completion. If the memory cycle fails to terminate within time t_{WPT}, write-protection takes place.

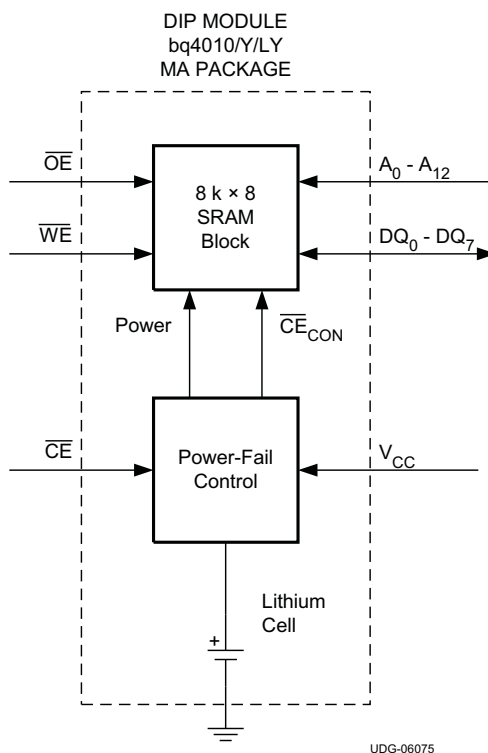
As V_{CC} falls past V_{PFD} and approaches V_{SO}, the control circuitry switches to the internal lithium backup supply, which provides data retention until valid V_{CC} is applied.

When V_{CC} returns to a level above the internal backup cell voltage, the supply is switched back to V_{CC} . After V_{CC} ramps above the V_{PFD} threshold, write-protection continues for a time t_{CER} (120 ms maximum in 5-V system, 85 ms maximum in 3.3-V system) to allow for processor stabilization. Normal memory operation may resume after this time.

The internal coin cells used by the bq4010/Y/LY have an extremely long shelf life and provide data retention for more than 10 years in the absence of system power.

As shipped from TI, the integral lithium cells of the MT-type module are electrically isolated from the memory. (Self-discharge in this condition is approximately 0.5% per year.) Following the first application of V_{CC} , this isolation is broken, and the lithium backup provides data retention on subsequent power-downs.

BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O OPERATION	POWER
Not selected	H	X	X	High-Z	Standby
Output disable	L	H	H	High-Z	Active
Read	L	H	L	D_{OUT}	Active
Write	L	L	X	D_{IN}	Active

ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of the datasheet, or see the TI website at www.ti.com.

SELECTION GUIDE

DEVICE NUMBER	MAXIMUM ACCESS TIME (ns)	NEGATIVE SUPPLY TOLERANCE (%)	NOMINAL INPUT VOLTAGE V _{CC} (V)	TEMPERATURE (°C)
bq4010MA-70	70	-5	5	0 to 70
bq4010MA-85	85			
bq4010MA-150	150			
bq4010MA-200	200			
bq4010YMA-70	70	-10		-40 to 85
bq4010YMA-85	85			
bq4010YMA-150	150			
bq4010YMA-200	200			
bq4010YMA-70N	70			
bq4010YMA-85N	85			
bq4010YMA-150N	150			
bq4010LYMA-70N	70			

PART NUMBERING

PRODUCT LINE	MEMORY DENSITY	INPUT VOLTAGE (V)	NEGATIVE SUPPLY TOLERANCE	PACKAGE	SPEED (ns)	TEMPERATURE (°C)
bq40	10	L	Y	MA	70	N
	10 = 8 k × 8	Blank = 5	Blank = 5%	MA = DIP	70	Blank = Commercial
	11 = 32 k × 8	L = 3.3	Y = 10%		85	(0 to 70)
	13 = 128 k × 8				100	
	14 = 256 k × 8				120	N = Industrial
	15 = 512 k × 8				150	(-40 to 85)
	16 = 1024 k × 8				200	
	17 = 2048 k × 8					

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

PARAMETER		CONDITION		VALUE	UNIT
V _{CC}	DC voltage applied on VCC relative to VSS		bq4010Y	−0.3 to 7.0	V
			bq4010	−0.3 to 7.0	
			bq4010LY	−0.3 to 6.0	
V _T	DC voltage applied on any pin excluding VCC relative to VSS	V _{VT} ≤ V _{CC} + 0.3 V	bq4010Y	−0.3 to 7.0	V
			bq4010	−0.3 to 7.0	
			bq4010LY	−0.3 to (V _{CC} + 0.3)	
T _{OPR}	Operating temperature	Commercial		0 to 70	°C
		Industrial		−40 to 85	
T _{STG}	Storage temperature	Commercial		−10 to 70	
		Industrial		−40 to 85	
T _{BIAS}	Temperature under bias	Commercial		−10 to 70	
		Industrial		−40 to 85	
T _{SOLDER}	Soldering temperature	For 10 seconds		260	

(1) Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (T_A = T_{OPR})

		MIN	TYP ⁽¹⁾	MAX	UNIT
V _{CC}	Supply voltage	bq4010Y	4.50	5.00	5.50
		bq4010	4.75	5.00	5.50
		bq4010LY	3.00	3.30	3.60
V _{SS}	Supply voltage	0	0	0	V
V _{IL}	Low-level input voltage	−0.3		0.8	
V _{IH}	High-level Input voltage	2.2		V _{CC} + 0.3	

(1) Typical values indicate operation at T_A = 25°C.

DC ELECTRICAL CHARACTERISTICS

T_A = T_{OPR}, V_{CC(min)} ≤ V_{CC} ≤ V_{CC(max)}

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
I _{LI}	Input leakage current	V _{IN} = V _{SS} to V _{CC}			±1	μA
I _{LO}	Output leakage current	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$			±1	
V _{OH}	Output high voltage	I _{OH} = –1.0 mA	2.4			V
V _{OL}	Output low voltage	I _{OL} = 2.1 mA			0.4	
I _{SB1}	Standby supply current	$\overline{CE} = V_{IH}$		1	2	μA
I _{SB2}	Standby supply current	$\overline{CE} \geq V_{CC} - 0.2$ V, 0V ≤ V _{IN} ≤ 0.2 V, or V _{IN} ≥ V _{CC} – 0.2		0.1	1	mA
I _{CC}	Operating supply current	bq4010			50	mA
		bq4010Y	Minimum cycle, duty = 100%, CE = V _{IL} , I _{I/O} = 0 mA			
		bq4010LY			30	
V _{PFD}	Power-fail-detect voltage	bq4010	4.55	4.62	4.75	V
		bq4010Y	4.30	4.37	4.50	
		bq4010LY	2.85	2.90	2.95	
V _{SO}	Supply switch-over voltage	bq4010		3		
		bq4010Y		3		
		bq4010LY		2.9		

(1) Typical values indicate operation at T_A = 25°C, V_{CC} = 5.0 V or V_{CC} = 3.3 V.

CAPACITANCE ($T_A = 25^{\circ}\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = 5.0\text{ V}$ or $V_{CC} = 3.3\text{ V}$)

PARAMETER ⁽¹⁾		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$C_{I/O}$	Input/output capacitance	Output voltage = 0 V			8	pF
C_{IN}	Input capacitance	Input voltage = 0 V			10	

(1) Ensured by design. Not production tested.

AC TEST CONDITIONS

PARAMETER	TEST CONDITIONS	
	5 V	3.3 V
Input pulse levels	0 V to 3.0 V	0 V to V_{CC}
Input rise and fall times	5 ns	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)	50 %
Output load (including scope and jig)	See Figure 1 and Figure 2	See Figure 3 and Figure 4

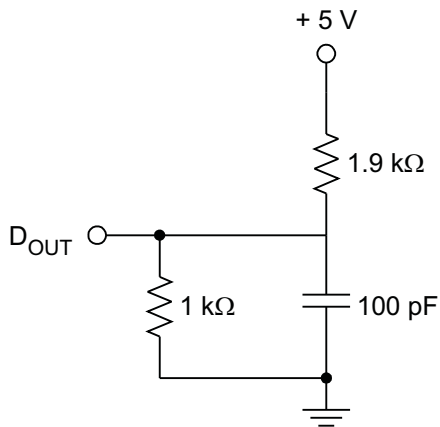


Figure 1. 5-V Output Load A

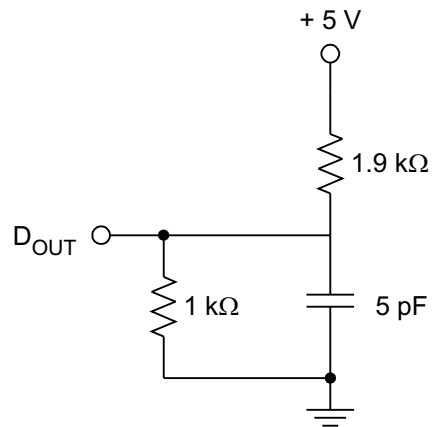


Figure 2. 5-V Output Load B

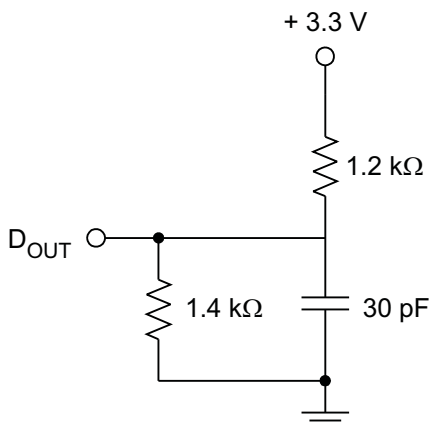


Figure 3. 3.3-V Output Load A

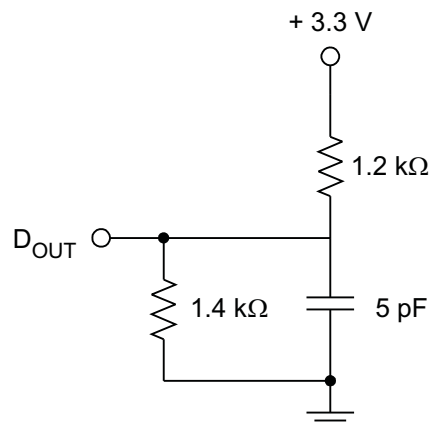
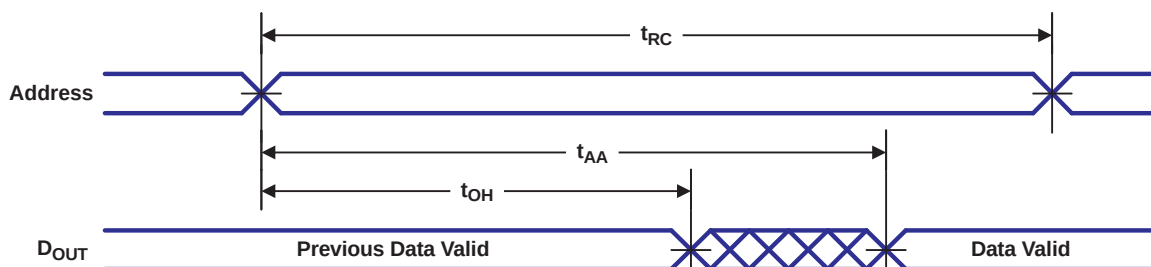


Figure 4. 3.3-V Output Load B

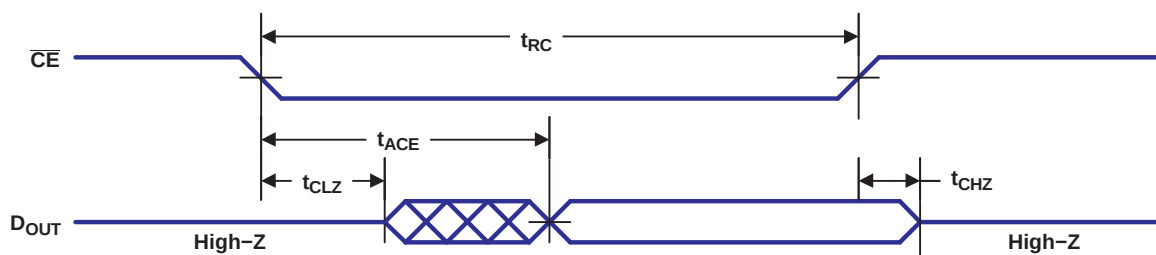
Table 2. READ CYCLE ($T_A = T_{OPR}$, $V_{CC(min)} \leq V_{CC} \leq V_{CC(max)}$)

PARAMETER		TEST CONDITIONS	-70		-85		-150		-200		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Read cycle time		70		85		150		200		ns
t_{AA}	Address access time	Output load A		70		85		150		200	
t_{ACE}	Chip enable access time			70		85		150		200	
t_{OE}	Output enable to output valid			35		45		70		90	
t_{CLZ}	Chip enable to output in low Z	Output load B		5		5		5		5	
t_{OLZ}	Output enable to output in low Z			0		0		0		0	
t_{CHZ}	Chip disable to output in high Z			0	25	0	25	0	25	0	25
t_{OHZ}	Output disable to output in high Z			0	25	0	25	0	25	0	25
t_{OH}	Output hold from address change	Output load A		10		10		10		10	



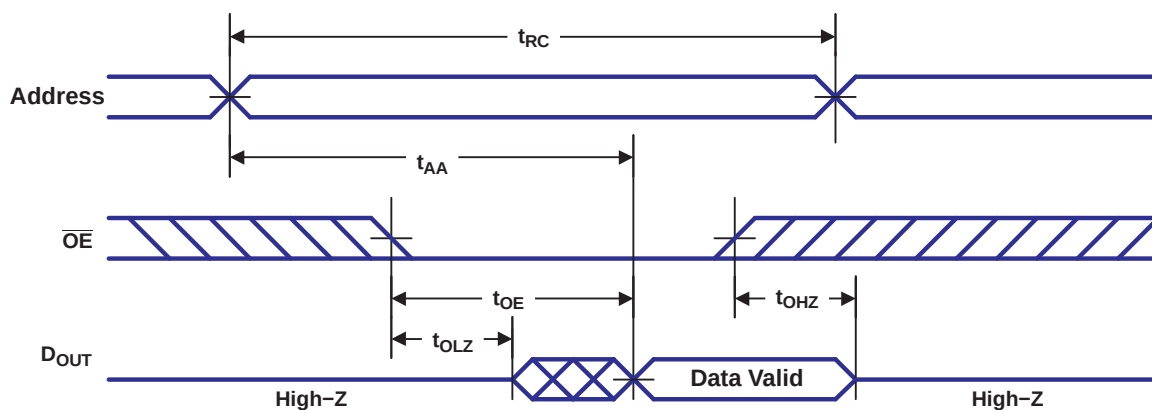
- (1) $\overline{WE}$ is held high for a read cycle.
- (2) Device is continuously selected: $\overline{CE} = \overline{OE} = V_{IL}$.

Figure 5. Read Cycle No. 1 (Address Access) ⁽¹⁾⁽²⁾



- (1) $\overline{WE}$ is held high for a read cycle.
- (2) Device is continuously selected: $\overline{CE} = \overline{OE} = V_{IL}$.
- (3) Address is valid prior to or coincident with $\overline{CE}$ transition low.

Figure 6. Read Cycle No. 2 ($\overline{CE}$ Access) ⁽¹⁾⁽²⁾⁽³⁾



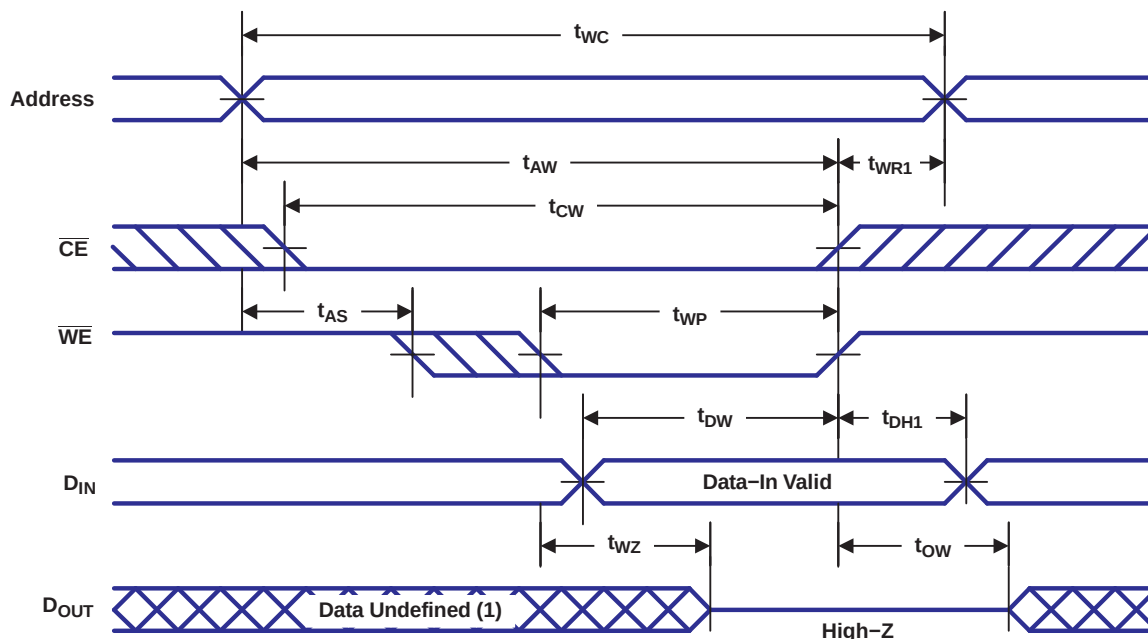
- (1) $\overline{WE}$ is held high for a read cycle.
- (2) Device is continuously selected: $\overline{CE} = V_{IL}$.

Figure 7. Read Cycle No. 3 ($\overline{OE}$ Access) ⁽¹⁾⁽²⁾

Table 3. WRITE CYCLE ($T_A = T_{OPR}$, $V_{CC(min)} \leq V_{CC} \leq V_{CC(max)}$)

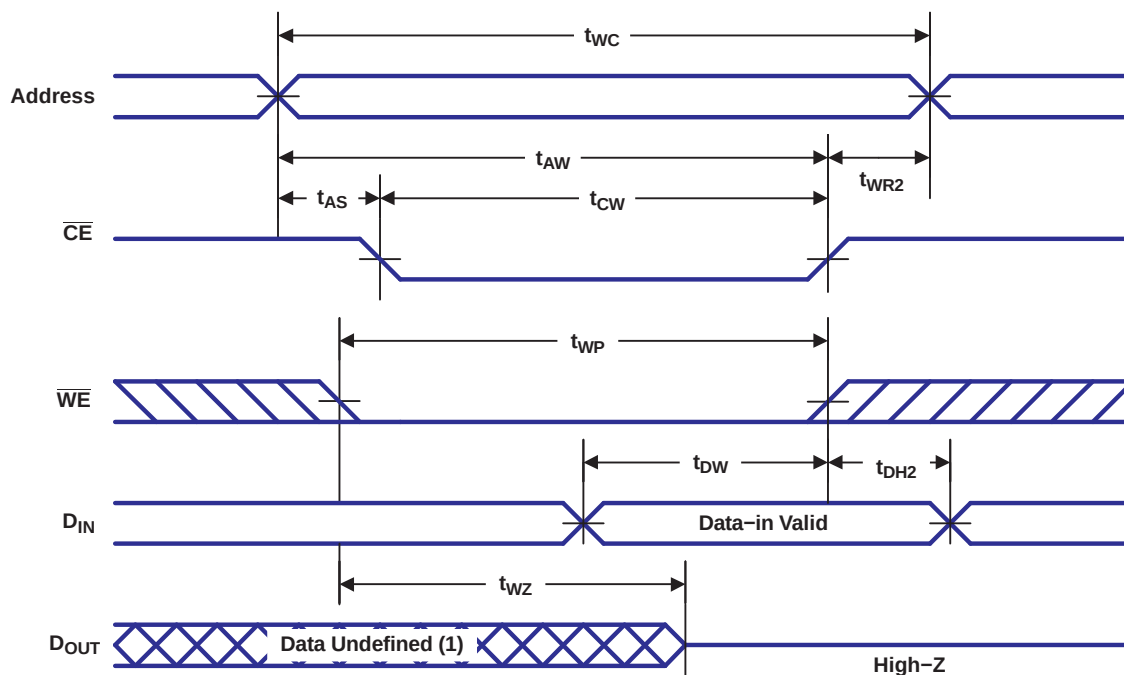
PARAMETER		TEST CONDITIONS	-70		-85		-150		-200		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{WC}	Write cycle time		70		85		150		200		ns
t_{CW}	Chip enable to end of write	See ⁽¹⁾	65		75		100		150		
t_{AW}	Address valid to end of write	See ⁽¹⁾	65		75		90		150		
t_{AS}	Address setup time	Measured from address valid to beginning of write. ⁽²⁾	0		0		0		0		
t_{WP}	Write pulse width	Measured from beginning of write to end of write. ⁽¹⁾	55		65		90		130		
t_{WR1}	Write recovery time (write cycle 1)	Measured from $\overline{WE}$ going high to end of write cycle. ⁽³⁾	5		5		5		5		
t_{WR2}	Write recovery time (write cycle 2)	Measured from $\overline{CE}$ going high to end of write cycle. ⁽³⁾	15		15		15		15		
t_{DW}	Data valid to end of write	Measured to first low-to-high transition of either $\overline{CE}$ or $\overline{WE}$.	30		35		50		70		
t_{DH1}	Data hold time (write cycle 1)	Measured from $\overline{WE}$ going high to end of write cycle. ⁽⁴⁾	0		0		0		0		
t_{DH2}	Data hold time (write cycle 2)	Measured from $\overline{CE}$ going high to end of write cycle. ⁽⁴⁾	0		0		0		0		
t_{WZ}	Write enabled to output in high Z	I/O pins are in output state. ⁽⁵⁾	0	25	0	30	0	50	0	70	
t_{OW}	Output active from end of write	I/O pins are in output state. ⁽⁵⁾	5		5		5		5		

- (1) A write ends at the earlier transition of $\overline{CE}$ going high and $\overline{WE}$ going high.
(2) A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CE}$ going low and $\overline{WE}$ going low.
(3) Either t_{WR1} or t_{WR2} must be met.
(4) Either t_{DH1} or t_{DH2} must be met.
(5) If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high-impedance state.



- (1) $\overline{CE}$ or $\overline{WE}$ must be high during address transition.
(2) Because I/O may be active ($\overline{OE}$ low) during this period, data input signals of opposite polarity to the outputs must not be applied.
(3) If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.

Figure 8. Write Cycle No. 1 ($\overline{WE}$ -Controlled) ⁽¹⁾⁽²⁾⁽³⁾



- (1) $\overline{CE}$ or $\overline{WE}$ must be high during address transition.
- (2) Because I/O may be active ($\overline{OE}$ low) during this period, data input signals of opposite polarity to the outputs must not be applied.
- (3) If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.
- (4) Either t_{WR1} or t_{WR2} must be met.
- (5) Either t_{DH1} or t_{DH2} must be met.

Figure 9. Write Cycle No. 2 ($\overline{CE}$ -Controlled) ⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾⁽⁵⁾

Table 4. 5-V POWER-DOWN/POWER-UP ($T_A = T_{OPR}$)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
t_{PF}	V_{CC} slew, 4.75 to 4.25 V		300			μ s
t_{FS}	V_{CC} slew, 4.25 to V_{SO}		10			μ s
t_{PU}	V_{CC} slew, V_{SO} to V_{PFD} (max.)		0			μ s
t_{CER}	Chip enable recovery time	Time during which SRAM is write-protected after V_{CC} passes V_{PFD} on power-up.	40	80	120	ms
t_{DR}	Data-retention time in absence of V_{CC}	$T_A = 25^\circ\text{C}$ ⁽²⁾	10			years
t_{WPT}	Write-protect time	Delay after V_{CC} slews down past V_{PFD} before SRAM is writeprotected.	40	100	150	μ s

(1) Typical values indicate operation at $T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{V}$.

(2) Batteries are disconnected from circuit until after V_{CC} is applied for the first time. t_{DR} is the accumulated time in absence of power beginning when power is first applied to the device.

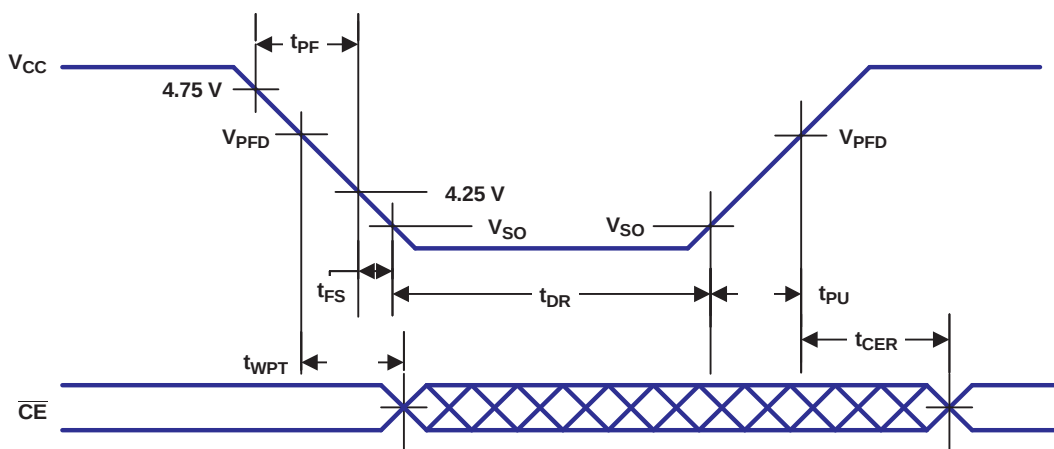


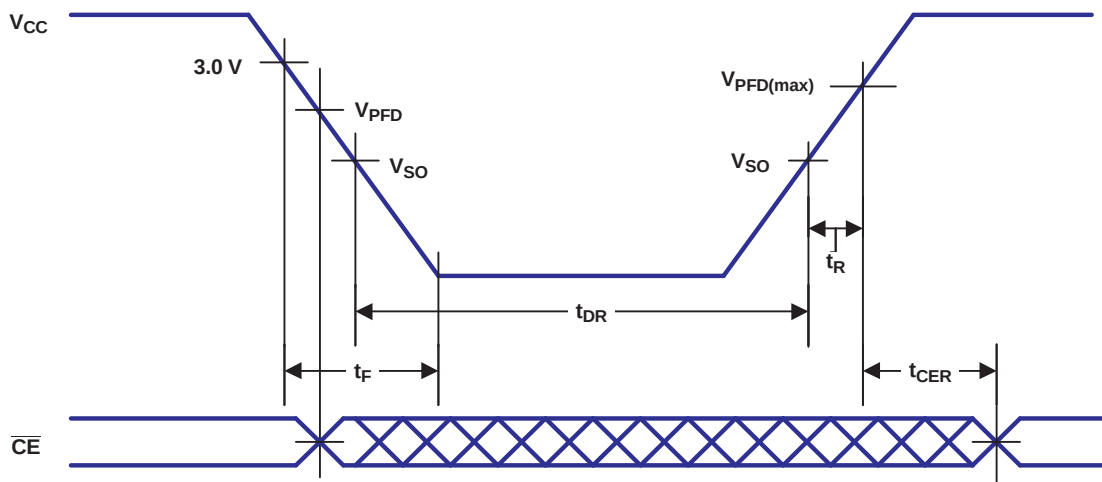
Figure 10. 5-V Power-Down/Power-Up Timing

Table 5. 3.3-V POWER-DOWN/POWER-UP ($T_A = T_{OPR}$)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
t_F	V_{CC} slew, 3 V to 0 V		300			μs
t_R	V_{CC} slew, V_{SO} to $V_{PFD(max)}$		100			
t_{CER}	Chip enable recovery time	Time during which SRAM is write-protected after V_{CC} passes V_{PFD} on power-up.	10		85	ms
t_{DR}	Data-retention time in absence of V_{CC}	$T_A = 25^\circ C^{(2)}$	10			years

(1) Typical values indicate operation at $T_A = 25^\circ C$, $V_{CC} = 3.3$ V.

(2) Batteries are disconnected from circuit until after V_{CC} is applied for the first time. Data retention time (t_{DR}) is the accumulated time in absence of power beginning when power is first applied to the device.

**Figure 11. 3.3-V Power-Down/Power-Up Timing****CAUTION:**

Negative undershoots below the absolute maximum rating of -0.3 V in battery-backup mode may affect data integrity.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
BQ4010LYMA-70N	ACTIVE	DIP MOD ULE	MA	28	1	Pb-Free (RoHS)	CU SN	N / A for Pkg Type
BQ4010MA-150	NRND	DIP MOD ULE	MA	28	1	Pb-Free (RoHS)	CU SN	N / A for Pkg Type
BQ4010MA-200	NRND	DIP MOD ULE	MA	28	14	Pb-Free (RoHS)	CU SN	N / A for Pkg Type
BQ4010MA-70	ACTIVE	DIP MOD ULE	MA	28	14	Pb-Free (RoHS)	CU SN	N / A for Pkg Type
BQ4010MA-85	NRND	DIP MOD ULE	MA	28	1	Pb-Free (RoHS)	CU SN	N / A for Pkg Type
BQ4010YMA-150	NRND	DIP MOD ULE	MA	28	1	Pb-Free (RoHS)	CU SN	N / A for Pkg Type
BQ4010YMA-150N	NRND	DIP MOD ULE	MA	28	1	Pb-Free (RoHS)	CU SN	N / A for Pkg Type
BQ4010YMA-200	NRND	DIP MOD ULE	MA	28	14	Pb-Free (RoHS)	CU SN	N / A for Pkg Type
BQ4010YMA-70	ACTIVE	DIP MOD ULE	MA	28	14	Pb-Free (RoHS)	CU SN	N / A for Pkg Type
BQ4010YMA-70N	ACTIVE	DIP MOD ULE	MA	28	1	Pb-Free (RoHS)	CU SN	N / A for Pkg Type
BQ4010YMA-85	NRND	DIP MOD ULE	MA	28	1	Pb-Free (RoHS)	CU SN	N / A for Pkg Type
BQ4010YMA-85N	NRND	DIP MOD ULE	MA	28	1	Pb-Free (RoHS)	CU SN	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

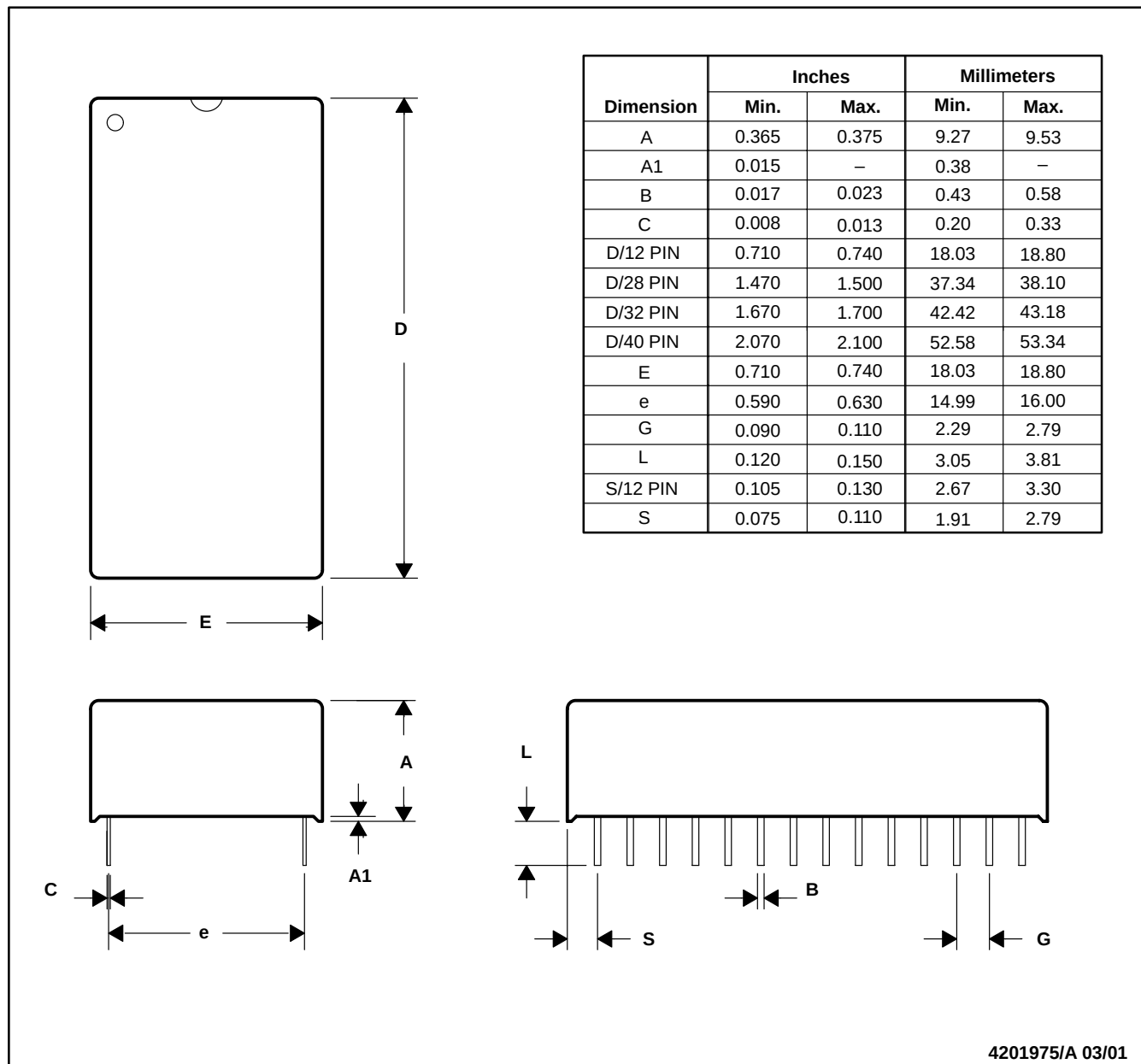
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

MA (R-PDIP-T**)

PLASTIC DUAL-IN-LINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in inches (mm).
 B. This drawing is subject to change without notice.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
RF/IF and ZigBee® Solutions	www.ti.com/lprf

Applications

Audio	www.ti.com/audio
Automotive	www.ti.com/automotive
Broadband	www.ti.com/broadband
Digital Control	www.ti.com/digitalcontrol
Medical	www.ti.com/medical
Military	www.ti.com/military
Optical Networking	www.ti.com/opticalnetwork
Security	www.ti.com/security
Telephony	www.ti.com/telephony
Video & Imaging	www.ti.com/video
Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2008, Texas Instruments Incorporated