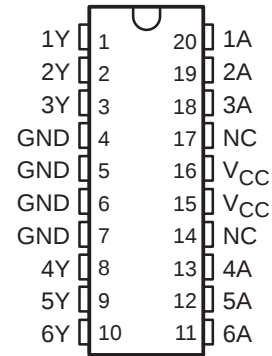


- CDC204 Replaces 74AC11204
- Low-Skew Propagation Delay Specifications for Clock-Driver Applications
- CMOS-Compatible Inputs and Outputs
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Pin Configurations Minimize High-Speed Switching Noise
- *EPIC*™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline Package (DW))

DW PACKAGE
(TOP VIEW)



NC – No internal connection

description

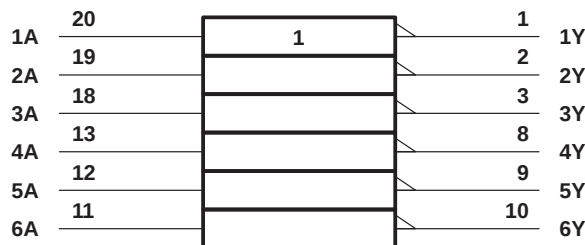
The CDC204 contains six independent inverters. The device performs the Boolean function $Y = \bar{A}$. It is designed specifically for applications requiring low skew between switching outputs.

The CDC204 is characterized for operation from $T_A = 25^\circ\text{C}$ to 70°C .

FUNCTION TABLE

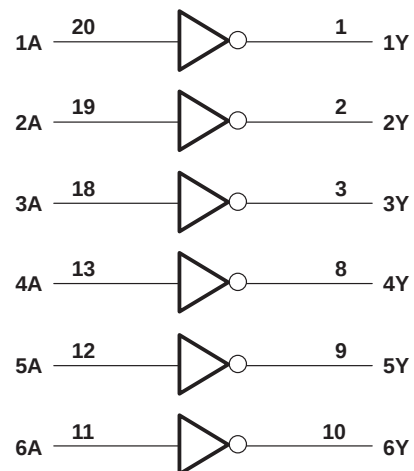
INPUT A	OUTPUT Y
H	L
L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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CDC204

HEX INVERTER/CLOCK DRIVER

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND	± 150 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2)	1.6 W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage	$V_{CC} = 4.75$ V		3.3	V
		$V_{CC} = 5.25$ V		3.7	
V_{IL}	Low-level input voltage	$V_{CC} = 4.75$ V		1.4	V
		$V_{CC} = 5.25$ V		1.6	
V_I	Input voltage	0		V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 4.75$ V		–24	mA
		$V_{CC} = 5.25$ V		–24	
I_{OL}	Low-level output current	$V_{CC} = 4.75$ V		24	mA
		$V_{CC} = 5.25$ V		24	
$\Delta t / \Delta v$	Input transition rise or fall rate	0		10	ns/V
f_{clock}	Input clock frequency			80	MHz
T_A	Operating free-air temperature	25		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A [†]	MIN	TYP	MAX	UNIT
V _{OH} High-level voltage output	I _{OH} = – 50 μA	V _{CC} = 4.75 V	25°C	4.65			V	
			Full range	4.65				
		V _{CC} = 5.25 V	25°C	5.15				
			Full range	5.15				
	I _{OH} = – 24 mA	V _{CC} = 4.75 V	25°C	4.19				
			Full range	4.05				
		V _{CC} = 5.25 V	25°C	4.68				
			Full range	4.55				
	I _{OH} = – 75 mA [‡] , V _{CC} = 5.25 V		Full range	3.6				
V _{OL} Low-level voltage output	I _{OL} = 50 μA	V _{CC} = 4.75 V	25°C			0.1	V	
			Full range			0.1		
		V _{CC} = 5.25 V	25°C			0.1		
			Full range			0.1		
	I _{OL} = 24 mA	V _{CC} = 4.75 V	25°C			0.36		
			Full range			0.44		
		V _{CC} = 5.25 V	25°C			0.36		
			Full range			0.44		
	I _{OL} = 75 mA [‡] , V _{CC} = 5.25 V		Full range			1.65		
I _I Input current	V _I = V _{CC} or GND V _{CC} = 5.25 V	25°C			±0.1	μA		
		Full range			±1			
I _{CC} Supply current	V _I = V _{CC} or GND, V _{CC} = 5.25 V, I _O = 0	25°C			4	μA		
		Full range			40			
C _i Input capacitance	V _I = V _{CC} or GND, V _{CC} = 5 V	25°C		4		pF		

[†] Full range is T_A = 25°C to 70°C.

[‡] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.25 V (see Note 3 and Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t _{PLH} Propagation delay time, low-to-high level (see Figure 1)	A	Y	3.7	5.7	ns
t _{PHL} Propagation delay time, high-to-low level (see Figure 1)			2.9	5.7	
t _{sk(o)} Output skew time (see Figure 2)	A	Y		1	ns

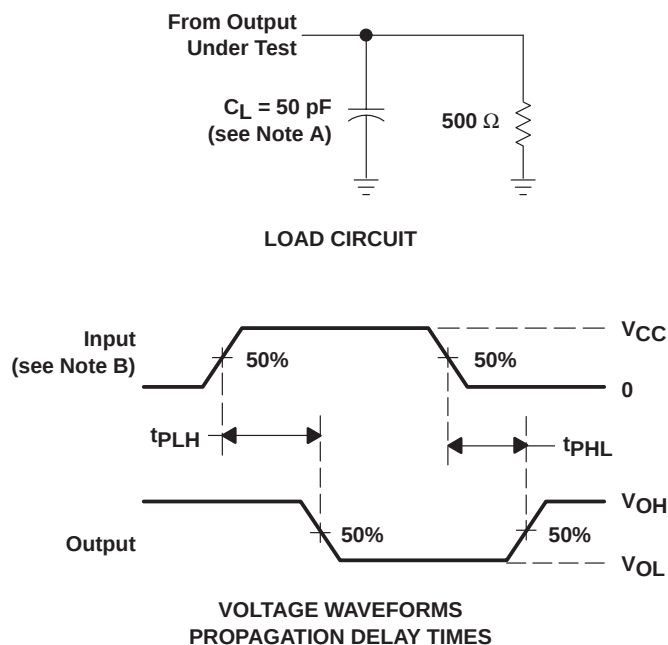
NOTE 3: All specifications are valid only for all outputs switching simultaneously and in phase.

CDC204

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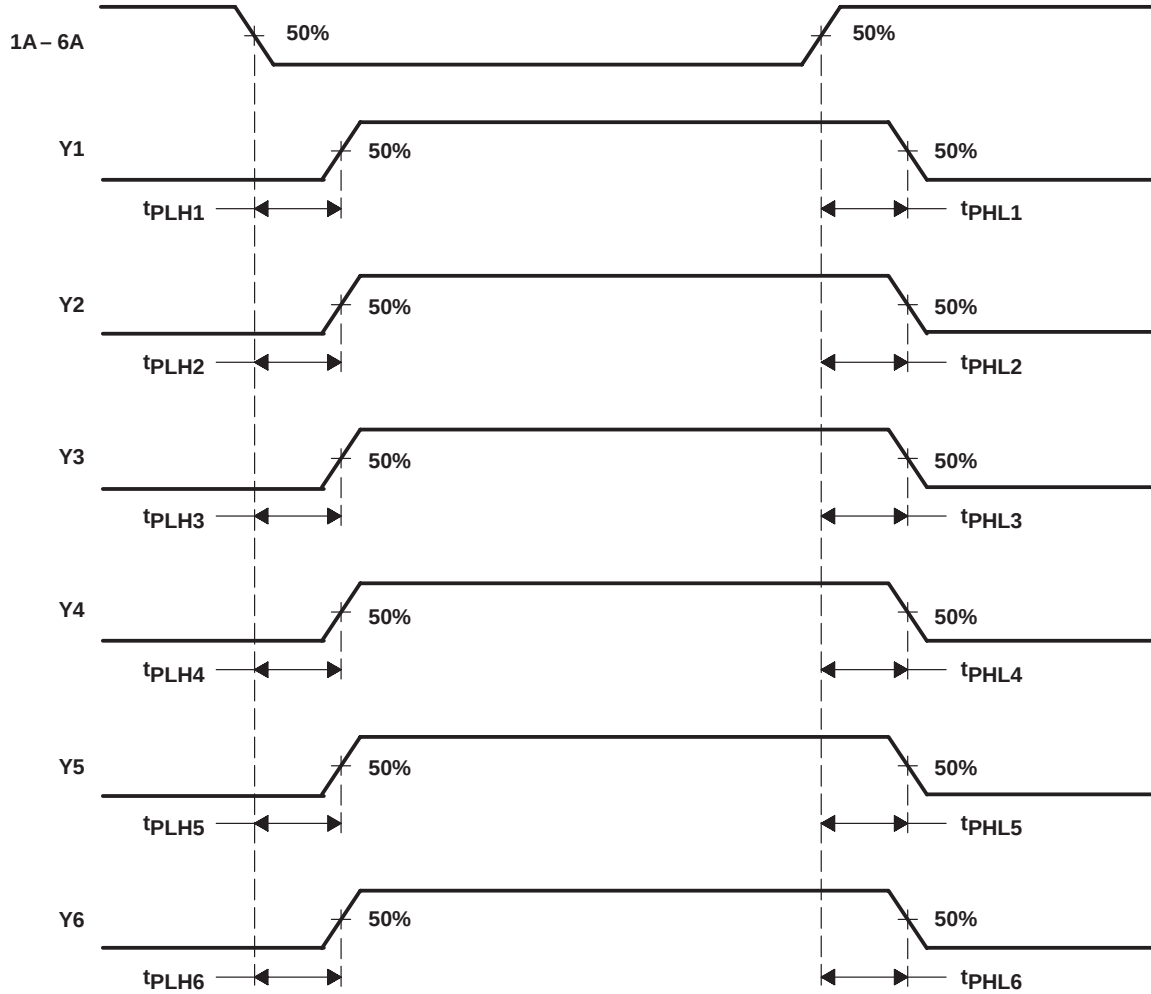
PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTE A: Output skew, $t_{sk(o)}$, is calculated as the greater of:

- The difference between the fastest and slowest of t_{PHLn} ($n = 1, 2, \dots, 6$)
- The difference between the fastest and slowest of t_{PLHn} ($n = 1, 2, \dots, 6$)

Figure 2. Waveforms for Calculation of $t_{sk(o)}$

CDC204

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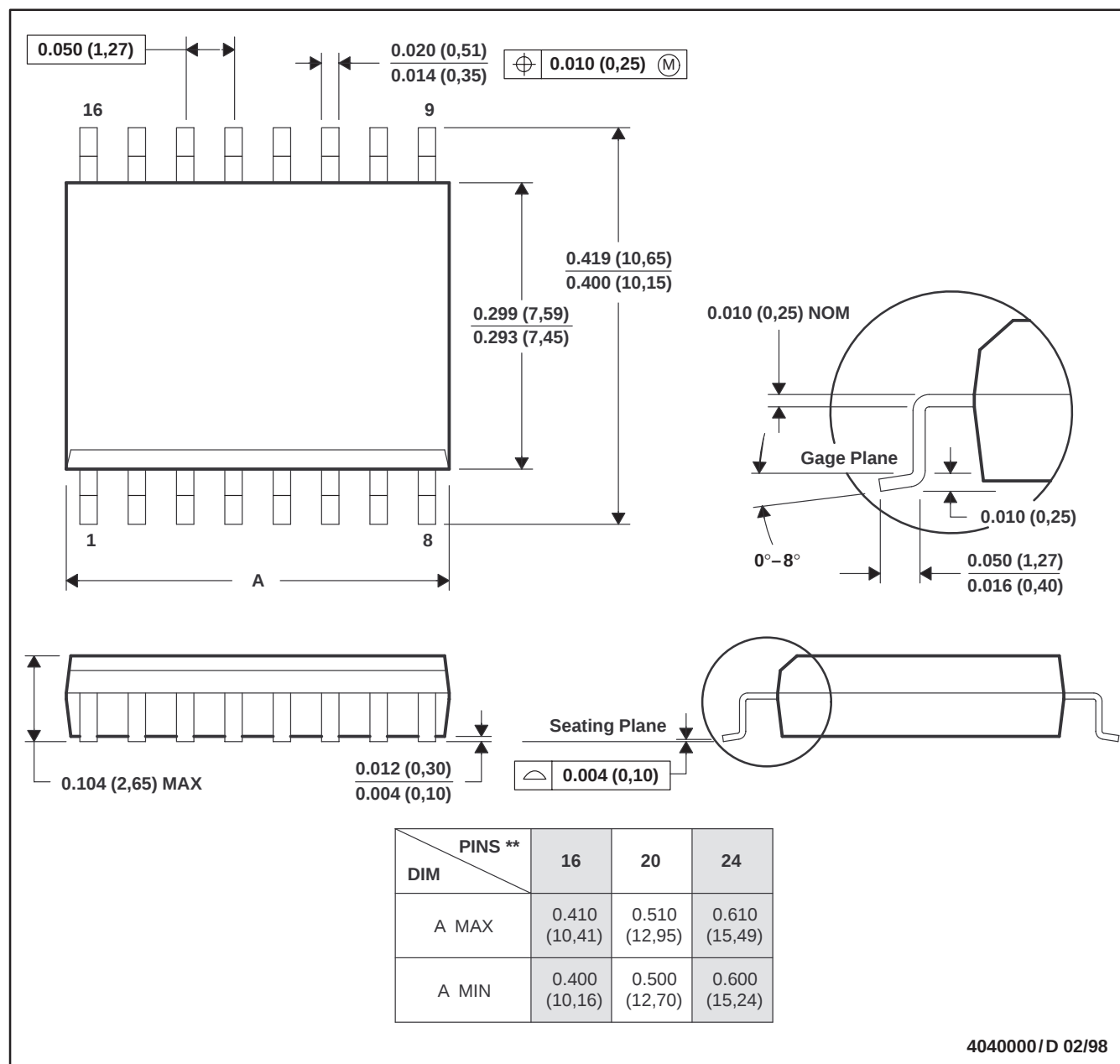
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MECHANICAL INFORMATION

DW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

16 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-013

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CDC204DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CDC204DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CDC204DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CDC204DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CDC204N	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

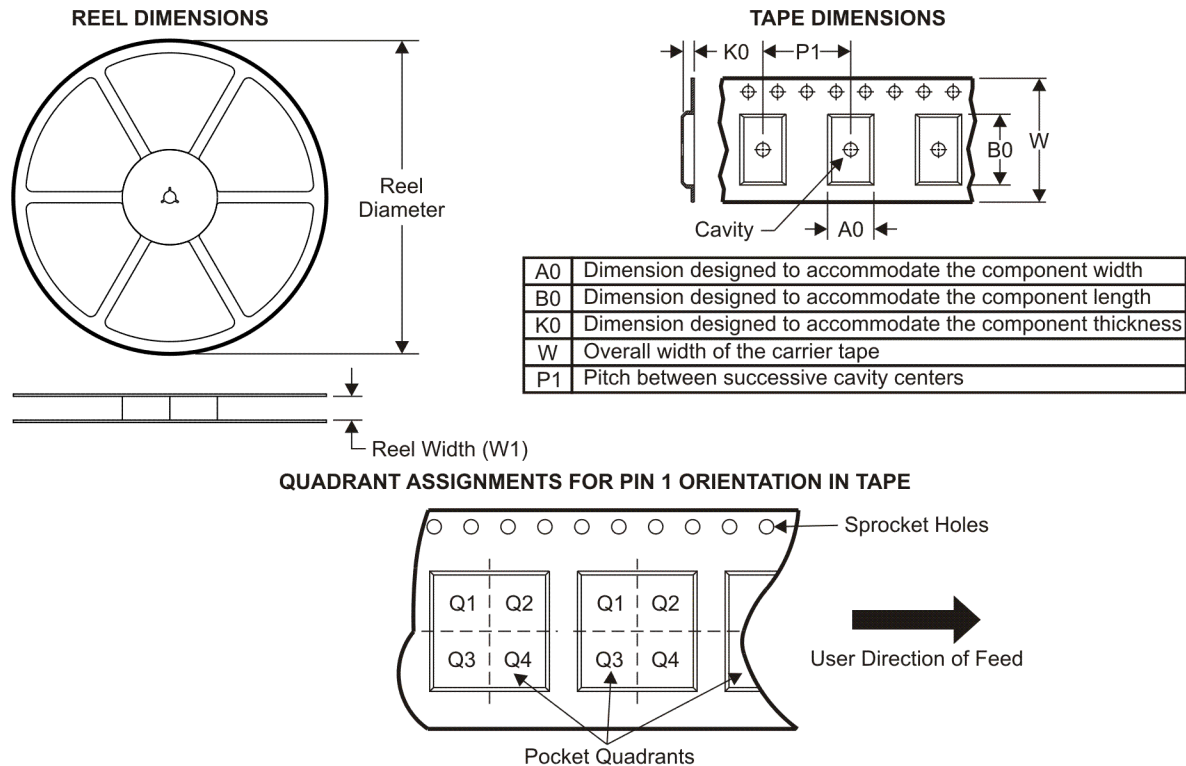
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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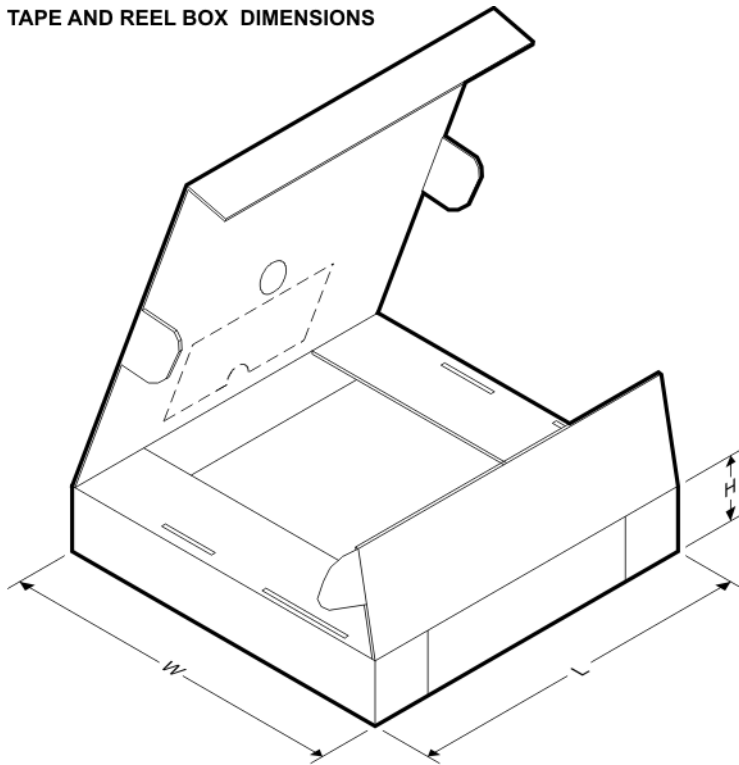
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDC204DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDC204DWR	SOIC	DW	20	2000	346.0	346.0	41.0

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