

1.8-V PHASE LOCK LOOP CLOCK DRIVER

SCAS688D–JUNE 2005–REVISED JULY 2007

FEATURES

- 1.8-V Phase Lock Loop Clock Driver for Double Data Rate (DDR II) Applications
- Spread Spectrum Clock Compatible
- Operating Frequency: 10 MHz to 400 MHz
- Low Current Consumption: <135 mA
- Low Jitter (Cycle-Cycle): ± 30 ps
- Low Output Skew: 35 ps
- Low Period Jitter: ± 20 ps
- Low Dynamic Phase Offset: ± 15 ps
- Low Static Phase Offset: ± 50 ps
- Distributes One Differential Clock Input to Ten Differential Outputs
- 52-Ball μ BGA (MicroStar™ Junior BGA, 0,65-mm pitch) and 40-Pin MLF
- External Feedback Pins (FBIN, $\overline{\text{FBIN}}$) are Used to Synchronize the Outputs to the Input Clocks
- Meets or Exceeds JESD82-8 PLL Standard for PC2-3200/4300
- Fail-Safe Inputs

DESCRIPTION

The CDCU877 is a high-performance, low-jitter, low-skew, zero-delay buffer that distributes a differential clock input pair (CK, $\overline{\text{CK}}$) to ten differential pairs of clock outputs (Yn, $\overline{\text{Yn}}$) and to one differential pair of feedback clock outputs (FBOUT, $\overline{\text{FBOUT}}$). The clock outputs are controlled by the input clocks (CK, $\overline{\text{CK}}$), the feedback clocks (FBIN, $\overline{\text{FBIN}}$), the LVCMOS control pins (OE, OS), and the analog power input (AV_{DD}). When OE is low, the clock outputs, except FBOUT/ $\overline{\text{FBOUT}}$, are disabled while the internal PLL continues to maintain its locked-in frequency. OS (output select) is a program pin that must be tied to GND or V_{DD}. When OS is high, OE functions as previously described. When OS and OE are both low, OE has no effect on Y7/ $\overline{\text{Y7}}$, they are free running. When AV_{DD} is grounded, the PLL is turned off and bypassed for test purposes.

When both clock inputs (CK, $\overline{\text{CK}}$) are logic low, the device enters in a low power mode. An input logic detection circuit on the differential inputs, independent from input buffers, detects the logic low level and performs in a low power state where all outputs, the feedback, and the PLL are off. When the clock inputs transition from being logic low to being differential signals, the PLL turns back on, the inputs and the outputs are enabled, and the PLL obtains phase lock between the feedback clock pair (FBIN, $\overline{\text{FBIN}}$) and the clock input pair (CK, $\overline{\text{CK}}$) within the specified stabilization time.

The CDCU877 is able to track spread spectrum clocking (SSC) for reduced EMI. This device operates from -40°C to 85°C .

ORDERING INFORMATION

T _A	52-BALL BGA ⁽¹⁾	40-Pin MLF
-40°C to 85°C	CDCU877ZQL	CDCU877RHA
	CDCU877AZQL	CDCU877ARHA
	CDCU877GQL	CDCU877RTB
	CDCU877AGQL	CDCU877ARTB

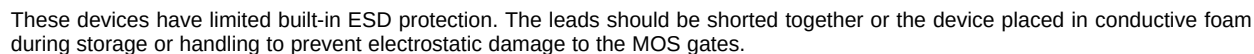
- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

MicroStar is a trademark of Texas Instruments.

SCAS688D – JUNE 2005 – REVISED JULY 2007



The diagram shows a 6-pin package with the following pin connections:

- Pin 1:** Y1
- Pin 2:** Y0
- Pin 3:** GND
- Pin 4:** Y0
- Pin 5:** Y5
- Pin 6:** Y6

Internal connections and labels within the package include:

- Top Row:** A, B, C, D, E, F, G, H, J, K
- Bottom Row:** Y1, Y0, GND, Y0, GND, Y5, Y6
- Left Side:** Y1, GND, Y2, GND, Y2, VDDQ, CK, VDDQ, CK, VDDQ, AGND, VDDQ, VDDQ, AVDD, GND, Y3, GND
- Right Side:** Y6, GND, Y7, GND, Y7, OS, VDDQ, FBIN, VDDQ, FBIN, OE, FBOUT, VDDQ, FBOUT, GND, Y8, GND

Labels 'NB' (Not Bypassed) are present in several locations, indicating specific internal connections or configurations.

- A. NC = No Connection
B. NB = No Ball

40-pin HP-VFQFP-N (6,0 x 6,0 mm Body Size,
0,5 mm Pitch, M0#220, Variation VJJD-2,
E2 = D2 = 2,9 mm $\pm$ 0,15 mm) Package Pinouts

1.8-V PHASE LOCK LOOP CLOCK DRIVER

SCAS688D – JUNE 2005 – REVISED JULY 2007

TERMINAL FUNCTIONS

TERMINAL		RHA/RTB	I/O	DESCRIPTION
NAME	GQL/ZQL			
AGND	G1	7		Analog ground
AV _{DD}	H1	8		Analog power
CK	E1	4	I	Clock input with a (10 kΩ to 100 kΩ) pulldown resistor
$\overline{\text{CK}}$	F1	5	I	Complementary clock input with a (10 kΩ to 100 kΩ) pulldown resistor
FBIN	E6	27	I	Feedback clock input
$\overline{\text{FBIN}}$	F6	26	I	Complementary feedback clock input
FBOU _T	H6	24	O	Feedback clock output
$\overline{\text{FBOU}}\overline{\text{T}}$	G6	25	O	Complementary feedback clock output
OE	F5	22	I	Output enable (asynchronous)
OS	D5	21	I	Output select (tied to GND or V _{DD})
GND	B2, B3, B4, B5, C2, C5, H2, H5, J2, J3, J4, J5	10		Ground
V _{DDQ}	D2, D3, D4, E2, E5, F2, G2, G3, G4, G5	1, 6, 9, 15, 20, 23, 28, 31, 36		Logic and output power
Y[0:9]	A2, A1, D1, J1, K3, A5, A6, D6, J6, K4	3, 11, 14, 16, 19, 29, 33, 34, 38, 39	O	Clock outputs
$\overline{\text{Y}}[0:9]$	A3, B1, C1, K1, K2, A4, B6, C6, K6, K5	2, 12, 13, 18, 17, 30, 32, 35, 37, 40	O	Complementary clock outputs

FUNCTION TABLE

INPUTS					OUTPUTS				
AVDD	OE	OS	CK	$\overline{\text{CK}}$	Y	$\overline{\text{Y}}$	FBOU _T	$\overline{\text{FBOU}}\overline{\text{T}}$	PLL
GND	H	X	L	H	L	H	L	H	Bypassed/Off
GND	H	X	H	L	H	L	H	L	Bypassed/Off
GND	L	H	L	H	L _Z	L _Z	L	H	Bypassed/Off
GND	L	L	H	L	L _Z Y7 Active	L _Z $\overline{\text{Y}}7$ Active	H	L	Bypassed/Off
1.8 V Nominal	L	H	L	H	L _Z	L _Z	L	H	On
1.8 V Nominal	L	L	H	L	L _Z Y7 Active	L _Z $\overline{\text{Y}}7$ Active	H	L	On
1.8 V Nominal	H	X	L	H	L	H	L	H	On
1.8 V Nominal	H	X	H	L	H	L	H	L	On
1.8 V Nominal	X	X	L	L	L _Z	L _Z	L _Z	L _Z	Off
X	X	X	H	H	Reserved				

1.8-V PHASE LOCK LOOP CLOCK DRIVER

SCAS688D – JUNE 2005 – REVISED JULY 2007

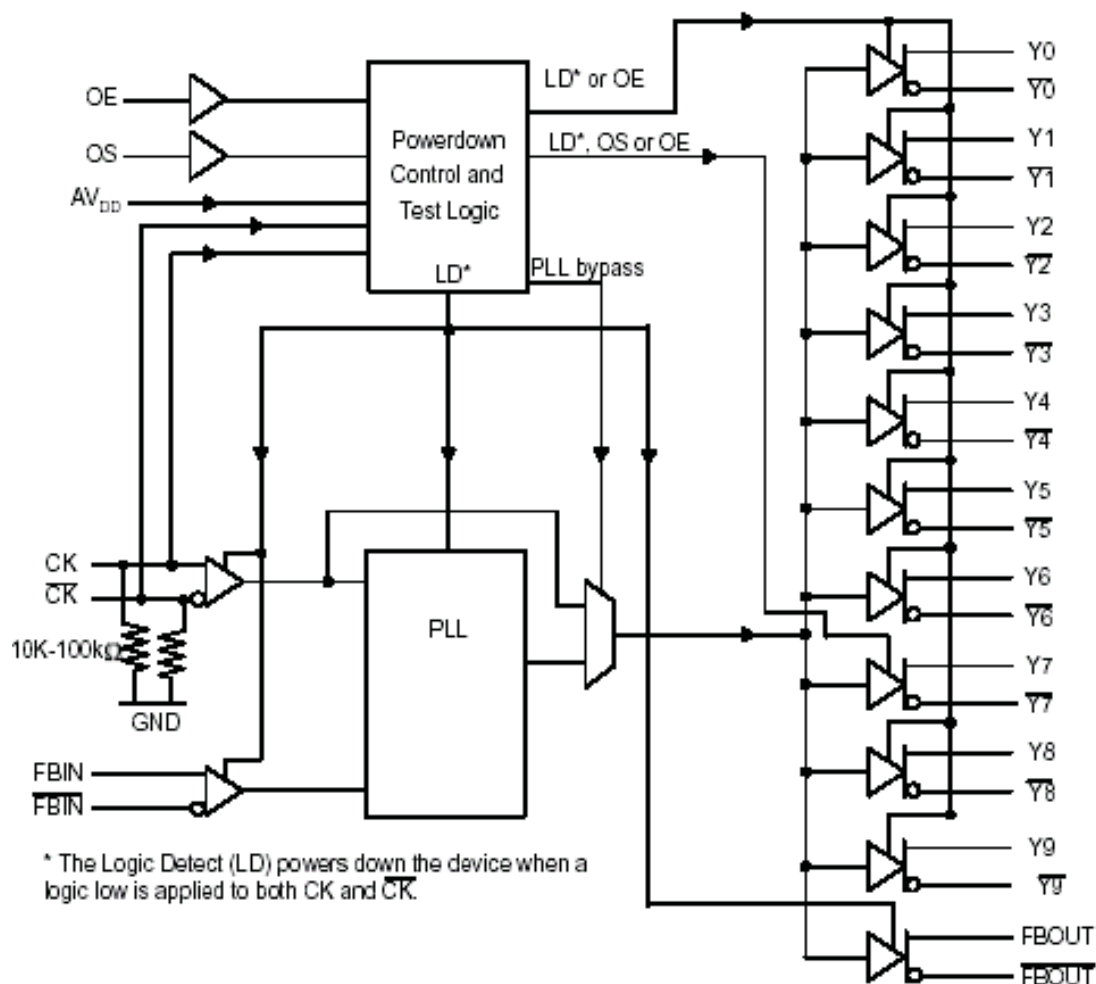


Figure 1. LOGIC DIAGRAM (POSITIVE LOGIC)

1.8-V PHASE LOCK LOOP CLOCK DRIVER

SCAS688D – JUNE 2005 – REVISED JULY 2007

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range	V _{DDQ} or AV _{DD}	–0.5	2.5	V
V _I	Input voltage range ⁽²⁾⁽³⁾		–0.5	V _{DDQ} + 0.5	V
V _O	Output voltage range ⁽²⁾⁽³⁾		–0.5	V _{DDQ} + 0.5	V
I _{IK}	Input clamp current	V _I < 0 or V _I > V _{DDQ}		±50	mA
I _{OK}	Output clamp current	V _O < 0 or V _O > V _{DDQ}		±50	mA
I _O	Continuous output current	V _O = 0 to V _{DDQ}		±50	mA
	Continuous current through each V _{DDQ} or GND			±100	mA
T _{stg}	Storage temperature range		–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) This value is limited to 2.5 V maximum.

Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V _{CC}	Output supply voltage, V _{DDQ}		1.7	1.8	1.9	V
	Supply Voltage, AV _{DD} ⁽¹⁾			V _{DDQ}		V
V _{IL}	Low-level input voltage ⁽²⁾	OE, OS			0.35 × V _{DDQ}	V
V _{IH}	High-level input voltage ⁽²⁾	CK, $\overline{\text{CK}}$	0.65 × V _{DDQ}			V
I _{OH}	High-level output current (see Figure 2)				–9	mA
I _{OL}	Low-level output current (see Figure 2)				9	mA
V _{IX}	Input differential-pair cross voltage		(V _{DDQ} /2) – 0.15		(V _{DDQ} /2) + 0.15	V
V _I	Input voltage level		–0.3		V _{DDQ} + 0.3	V
V _{ID}	Input differential voltage ⁽²⁾ (see Figure 9)	DC	0.3		V _{DDQ} + 0.4	V
		AC	0.6		V _{DDQ} + 0.4	V
T _A	Operating free-air temperature		–40		85	°C

- (1) The PLL is turned off and bypassed for test purposes when AV_{DD} is grounded. During this test mode, V_{DDQ} remains within the recommended operating conditions and no timing parameters are specified.
- (2) V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{\text{CK}}$, see Figure 9 for definition. The CK and $\overline{\text{CK}}$, V_{IH} and V_{IL} limits define the dc low and high levels for the logic detect state.

1.8-V PHASE LOCK LOOP CLOCK DRIVER

SCAS688D – JUNE 2005 – REVISED JULY 2007

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	AV _{DD} , V _{DDQ}	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{IK}	Input	I _I = 18 mA	1.7			-1.2	V
V _{OH}	High-level output voltage	I _{OH} = -100 µA	1.7 to 1.9	V _{DDQ} - 0.2			V
		I _{OH} = -9 mA	1.7	1.1			
V _{OL}	Low-level output voltage	I _{OL} = 100 µA				0.1	V
		I _{OL} = 9 mA	1.7			0.6	
I _{O(DL)}	Low-level output current, dissabled	V _{O(DL)} = 100 mV, OE = L	1.7	100			µA
V _{OD}	Differential output voltage ⁽¹⁾		1.7	0.5			V
I _I	Input current	CK, $\overline{\text{CK}}$	1.9			±250	µA
		OE, OS, FBIN, $\overline{\text{FBIN}}$	1.9			±10	
I _{DD(LD)}	Supply current, static (I _{DDQ} + I _{ADD})	CK and $\overline{\text{CK}}$ = L	1.9			500	µA
I _{DD}	Supply current, dynamic (I _{DDQ} + I _{ADD}) (see Note ⁽²⁾ for CPD calculation)	CK and $\overline{\text{CK}}$ = 270 MHz. All outputs are open (not connected to a PCB)	1.9			135	mA
		All outputs are loaded with 2 pF and 120-Ω termination resistor	1.9			235	
C _I	Input capacitance	CK, $\overline{\text{CK}}$	1.8	2		3	pF
		FBIN, $\overline{\text{FBIN}}$	1.8	2		3	
C _{I(Δ)}	Change in input current	CK, $\overline{\text{CK}}$	1.8			0.25	
		FBIN, $\overline{\text{FBIN}}$	1.8			0.25	

(1) V_{OD} is the magnitude of the difference between the true and complimentary outputs. See Figure 9 for a definition.(2) Total I_{DD} = I_{DDQ} + I_{ADD} = f_{CK} × C_{PD} × V_{DDQ}, solving for C_{PD} = (I_{DDQ} + I_{ADD})/(f_{CK} × V_{DDQ}) where f_{CK} is the input frequency, V_{DDQ} is the power supply, and C_{PD} is the power dissipation capacitance.

Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
f _{CK}	Clock frequency (operating) ⁽¹⁾⁽²⁾	AV _{DD} , V _{DD} = 1.8 V ±0.1 V	10	400	MHz
	Clock frequency (application) ⁽¹⁾⁽³⁾		160	340	MHz
t _{DC}	Duty cycle, input clock		40%	60%	
t _L	Stabilization time ⁽⁴⁾			12	µs

(1) The PLL must be able to handle spread spectrum induced skew.

(2) Operating clock frequency indicates a range over which the PLL must be able to lock, but in which it is not required to meet the other timing parameters (used for low speed system debug).

(3) Application clock frequency indicates a range over which the PLL must meet all timing parameters.

(4) Stabilization time is the time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal after power up. During normal operation, the stabilization time is also the time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal when CK and $\overline{\text{CK}}$ go to a logic low state, enter the power-down mode and later return to active operation. CK and $\overline{\text{CK}}$ may be left floating after they have been driven low for one complete clock cycle.

1.8-V PHASE LOCK LOOP CLOCK DRIVER

SCAS688D – JUNE 2005 – REVISED JULY 2007

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see ⁽¹⁾) AV_{DD} , $V_{DD} = 1.8\text{ V} \pm 0.1\text{ V}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{en}	Enable time, OE to any $\overline{Y}/\overline{Y}$	See Figure 11			8	ns
t_{dis}	Disable time, OE to any $\overline{Y}/\overline{Y}$	See Figure 11			8	ns
$t_{jit(cc+)}$	Cycle-to-cycle period jitter ⁽²⁾	160 MHz to 190 MHz, see Figure 4	0		40	ps
$t_{jit(cc-)}$			0		-40	
$t_{jit(cc+)}$	Cycle-to-cycle period jitter ⁽²⁾	160 MHz to 340 MHz, see Figure 4	0		30	ps
$t_{jit(cc-)}$			0		-30	
$t_{(w)}$	Static phase offset time ⁽³⁾	See Figure 5	-50		50	ps
$t_{(w)dyn}$	Dynamic phase offset time	See Figure 10	-15		15	ps
$t_{sk(o)}$	Output clock skew	See Figure 6			35	ps
$t_{jit(per)}$	Period jitter ⁽⁴⁾⁽²⁾	160 MHz to 190 MHz, see Figure 7	-30		30	ps
		190 MHz to 340 MHz, see Figure 7	-20		20	
$t_{jit(hper)}$	Half-period jitter ⁽⁴⁾⁽²⁾	160 MHz to 190 MHz, see Figure 8	-115		115	ps
		190 MHz to 250 MHz, see Figure 8	-70		70	
		250 MHz to 300 MHz, see Figure 8	-40		40	
		300 MHz to 340 MHz, see Figure 8	-60		60	
SR	Slew rate, OE	See Figure 3 and Figure 9	0.5			V/ns
	Input clock slew rate	See Figure 3 and Figure 9	1	2.5	4	
	Output clock slew rate ⁽⁵⁾⁽⁶⁾ (no load)	See Figure 3 and Figure 9	1.5	2.5	3	
V_{OX}	Output differential-pair cross voltage ⁽⁷⁾	CDCU877, See Figure 2	$(V_{DDQ}/2) - 0.1$		$(V_{DDQ}/2) + 0.1$	V
		CDCU877A ⁽⁸⁾ , See Figure 2 (0 - 85°C)	$(V_{DDQ}/2) - 0.1$		$(V_{DDQ}/2) + 0.1$	
	SSC modulation frequency		30		33	kHz
	SSC clock input frequency deviation		0%		-0.5%	
	PLL loop bandwidth		2			MHz

- (1) There are two different terminations that are used with the following tests. The load/board in [Figure 2](#) is used to measure the input and output differential-pair cross voltage only. The load/board in [Figure 3](#) is used to measure all other tests. For consistency, equal length cables must be used.
- (2) This parameter is specified by design and characterization.
- (3) Phase static offset time does not include jitter.
- (4) Period jitter, half-period jitter specifications are separate specifications that must be met independently of each other.
- (5) The output slew rate is determined from the IBIS model with a 120- Ω load only.
- (6) To eliminate the impact of input slew rates on static phase offset, the input skew rates of reference clock input CK and $\overline{CK}$ and feedback clock inputs FBIN and $\overline{FBIN}$ are recommended to be nearly equal. The 2.5-V/ns skew rates are shown as a recommended target. Compliance with these typical values is not mandatory if it can adequately shown that alternative characteristics meet the requirements of the registered DDR2 DIMM application.
- (7) Output differential-pair cross voltage specified at the DRAM clock input or the test load.
- (8) V_{OX} of CDCU877A is on average 30 mV lower than that of CDCU877 for the same application.

1.8-V PHASE LOCK LOOP CLOCK DRIVER

SCAS688D–JUNE 2005–REVISED JULY 2007

PARAMETER MEASUREMENT INFORMATION

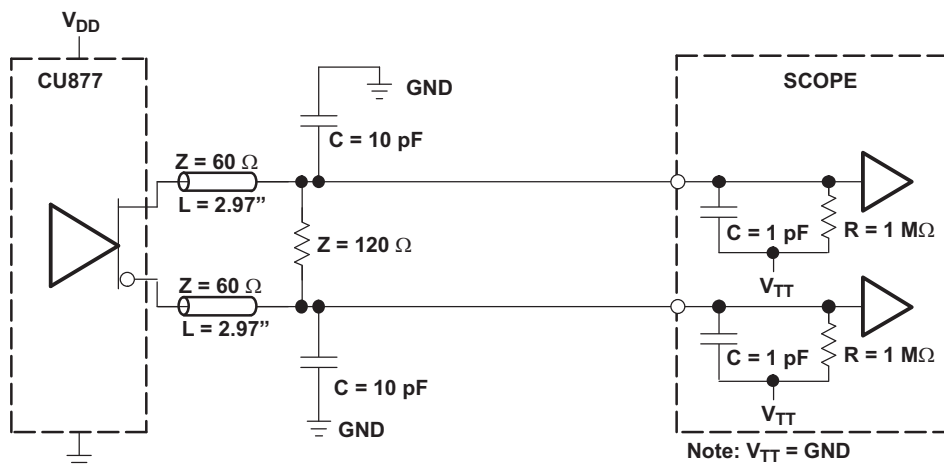


Figure 2. Output Load Test Circuit 1

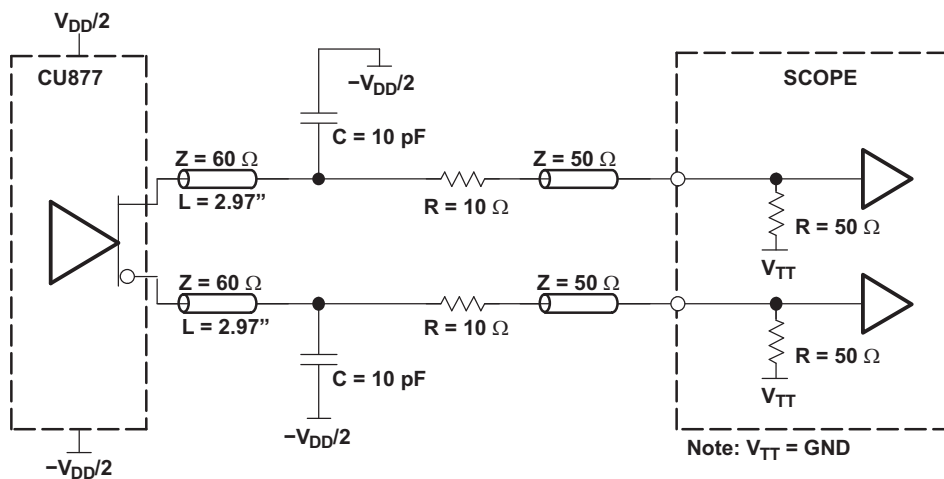


Figure 3. Output Load Test Circuit 2

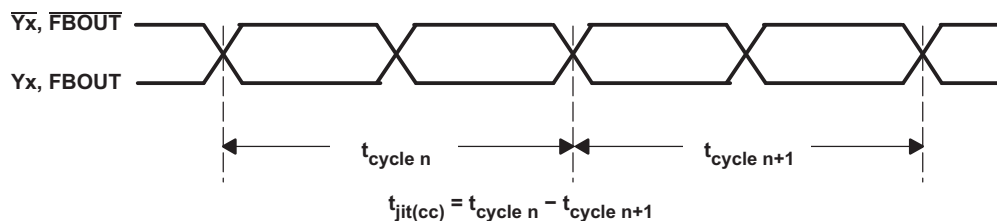


Figure 4. Cycle-To-Cycle Period Jitter

PARAMETER MEASUREMENT INFORMATION (continued)

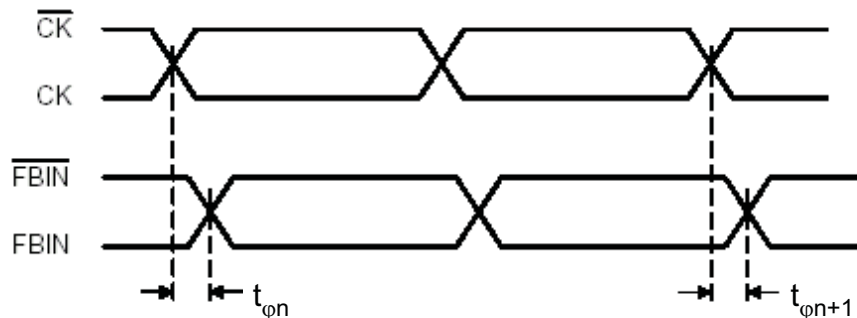


Figure 5. Static Phase Offset

$$t_{\phi} = \frac{\sum_{n=1}^N t_{\phi n}}{N}$$

(N is the large number of samples)

(N > 1000 samples)

(1)

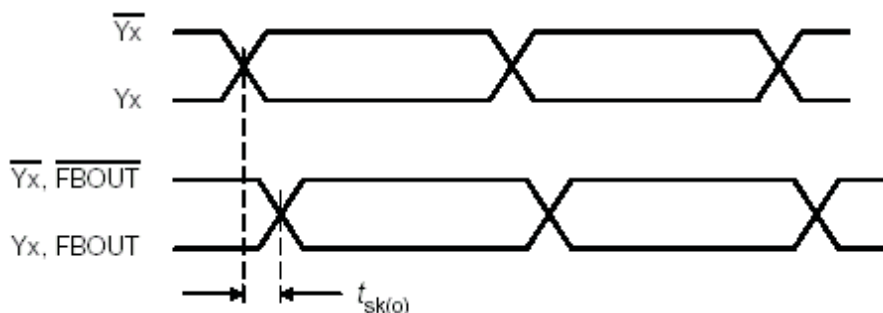


Figure 6. Output Skew

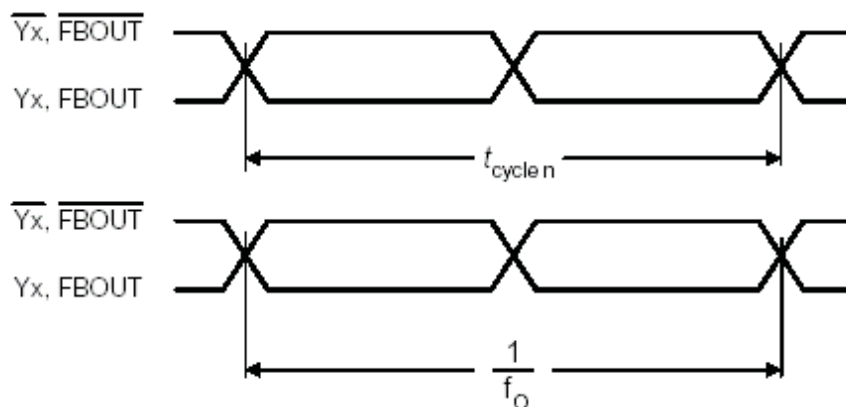


Figure 7. Period Jitter

$$t_{jit(per)} = t_{cycle\ n} - \frac{1}{f_o}$$

(f_o average input frequency measured at CK/CK-bar)

(2)

PARAMETER MEASUREMENT INFORMATION (continued)

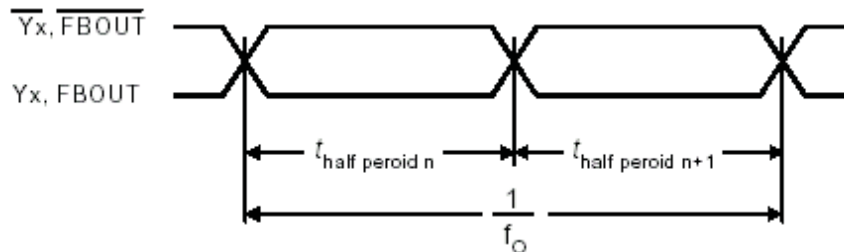


Figure 8. Half-Period Jitter

$$t_{jit(hper)} = t_{half\ period\ n} - \frac{1}{2 \times f_O}$$

n = any half cycle

(f_O average input frequency measured at CK/ $\overline{CK}$)

(3)

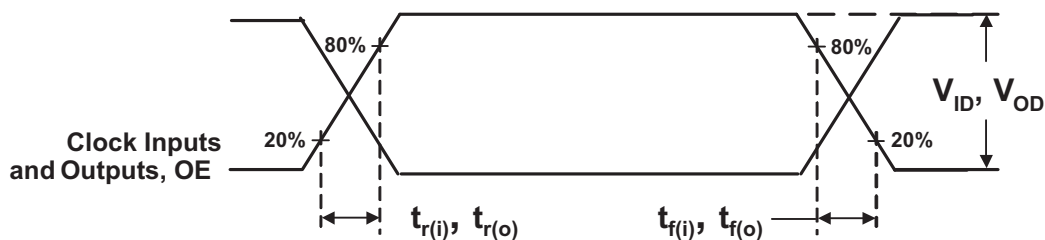


Figure 9. Input and Output Slew Rates

$$slrr_{(i/o)} = \frac{V_{80\%} - V_{20\%}}{t_{r(i/o)}}$$

$$slrf_{(i/o)} = \frac{V_{80\%} - V_{20\%}}{t_{f(i/o)}}$$

(4)

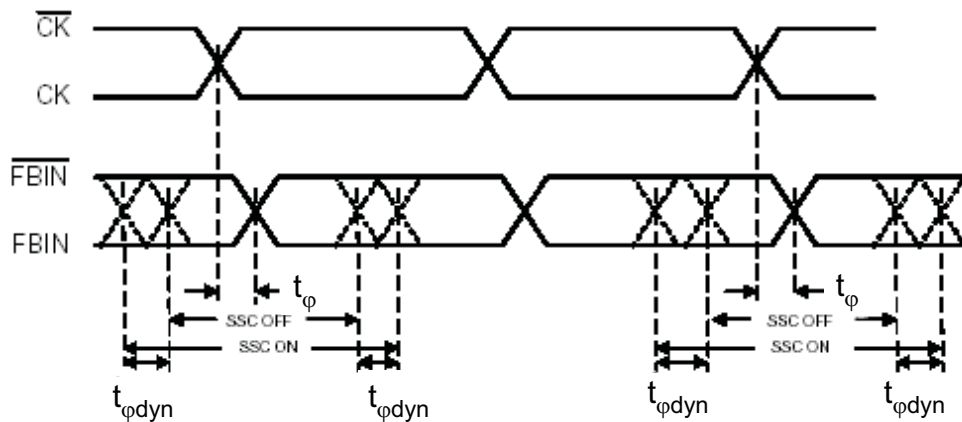


Figure 10. Dynamic Phase Offset

PARAMETER MEASUREMENT INFORMATION (continued)

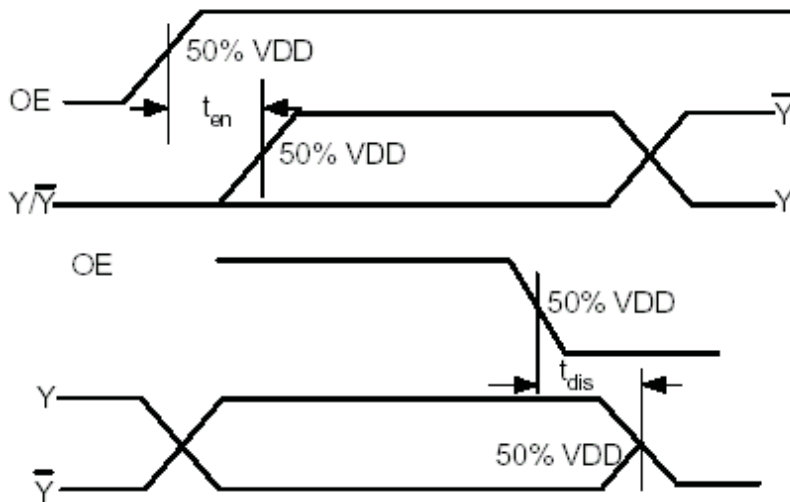
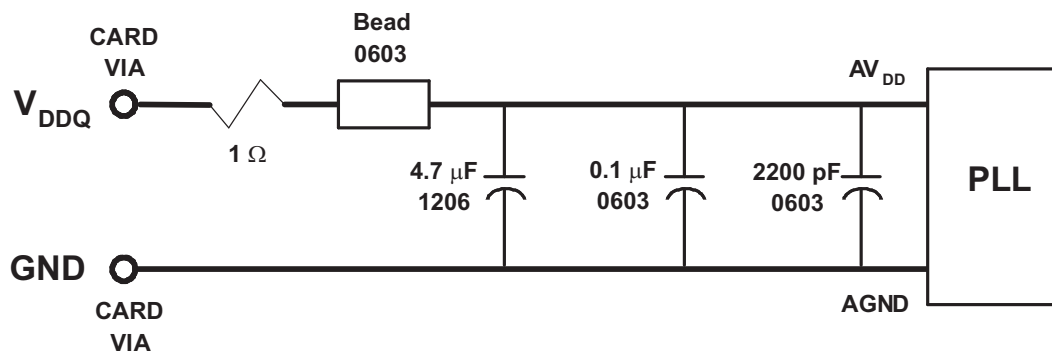


Figure 11. Time Delay Between OE and Clock Output (Y, $\bar{Y}$)

RECOMMENDED AV_{DD} FILTERING



- Place the 2200-pF capacitor close to the PLL.
- Use a wide trace for the PLL analog power and ground. Connect PLL and capacitors to AGND trace and connect trace to one GND via (farthest from the PLL).
- Recommended bead: Fair-Rite PN 2506036017Y0 or equivalent (0.8 Ω dc maximum, 600 Ω at 100 MHz).

Figure 12. Recommended AV_{DD} Filtering

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
CDCU877AGQLT	ACTIVE	BGA MICROSTAR JUNIOR	GQL	52	250	TBD	SNPB	Level-2-235C-1 YEAR	
CDCU877ARHAR	ACTIVE	VQFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
CDCU877ARHARG4	ACTIVE	VQFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
CDCU877ARHAT	ACTIVE	VQFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
CDCU877ARHATG4	ACTIVE	VQFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
CDCU877ARTBR	OBSOLETE	VQFN	RTB	40		TBD	Call TI	Call TI	
CDCU877AZQLR	ACTIVE	BGA MICROSTAR JUNIOR	ZQL	52	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-2-260C-1 YEAR	
CDCU877AZQLT	ACTIVE	BGA MICROSTAR JUNIOR	ZQL	52	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-2-260C-1 YEAR	
CDCU877GQLR	ACTIVE	BGA MICROSTAR JUNIOR	GQL	52	1000	TBD	SNPB	Level-2-235C-1 YEAR	
CDCU877GQLT	ACTIVE	BGA MICROSTAR JUNIOR	GQL	52	250	TBD	SNPB	Level-2-235C-1 YEAR	
CDCU877RHAR	ACTIVE	VQFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
CDCU877RHARG4	ACTIVE	VQFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
CDCU877RHAT	ACTIVE	VQFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
CDCU877RHATG4	ACTIVE	VQFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
CDCU877RTBR	OBSOLETE	VQFN	RHA	40		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
CDCU877RTBT	OBSOLETE	VQFN	RTB	40		TBD	Call TI	Call TI	
CDCU877ZQLR	ACTIVE	BGA MICROSTAR JUNIOR	ZQL	52	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-2-260C-1 YEAR	
CDCU877ZQLT	ACTIVE	BGA MICROSTAR JUNIOR	ZQL	52	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-2-260C-1 YEAR	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

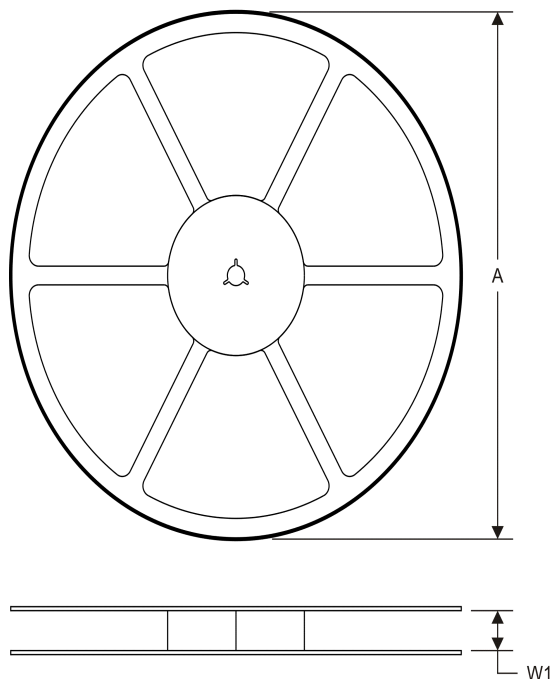
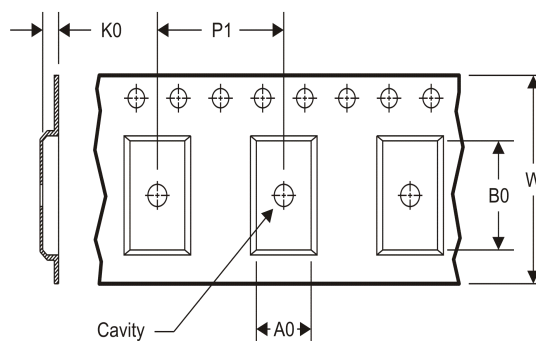
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


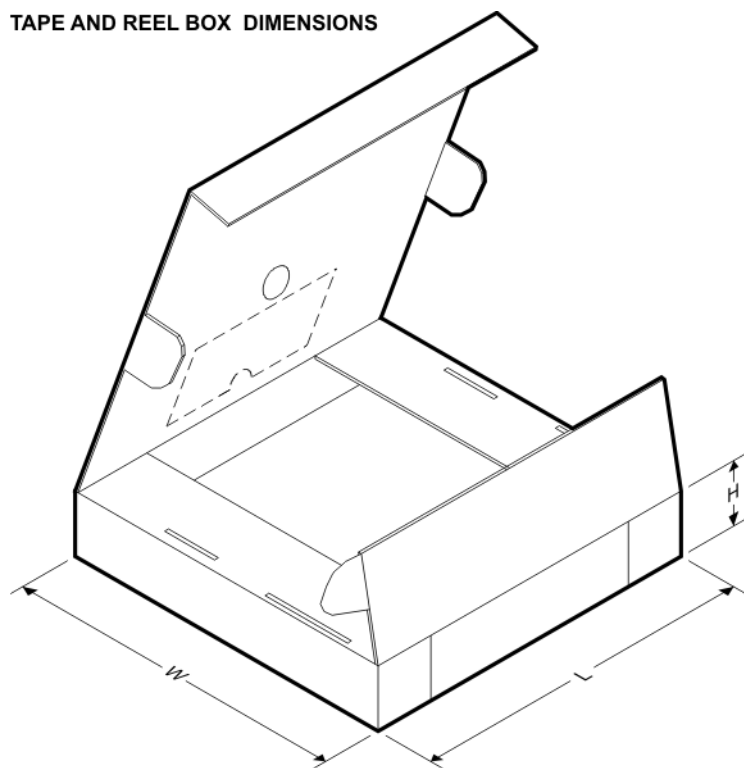
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCU877AGQLT	BGA MICROSTAR JUNIOR	GQL	52	250	330.0	16.4	4.8	7.3	1.5	8.0	16.0	Q1
CDCU877ARHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
CDCU877ARHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
CDCU877AZQLR	BGA MICROSTAR JUNIOR	ZQL	52	1000	330.0	16.4	4.8	7.3	1.5	8.0	16.0	Q1
CDCU877AZQLT	BGA MICROSTAR JUNIOR	ZQL	52	250	330.0	16.4	4.8	7.3	1.5	8.0	16.0	Q1
CDCU877GQLR	BGA MICROSTAR JUNIOR	GQL	52	1000	330.0	16.4	4.8	7.3	1.5	8.0	16.0	Q1
CDCU877GQLT	BGA MICROSTAR JUNIOR	GQL	52	250	330.0	16.4	4.8	7.3	1.5	8.0	16.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCU877RHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
CDCU877RHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
CDCU877ZQLR	BGA MICROSTAR JUNIOR	ZQL	52	1000	330.0	16.4	4.8	7.3	1.5	8.0	16.0	Q1
CDCU877ZQLT	BGA MICROSTAR JUNIOR	ZQL	52	250	330.0	16.4	4.8	7.3	1.5	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


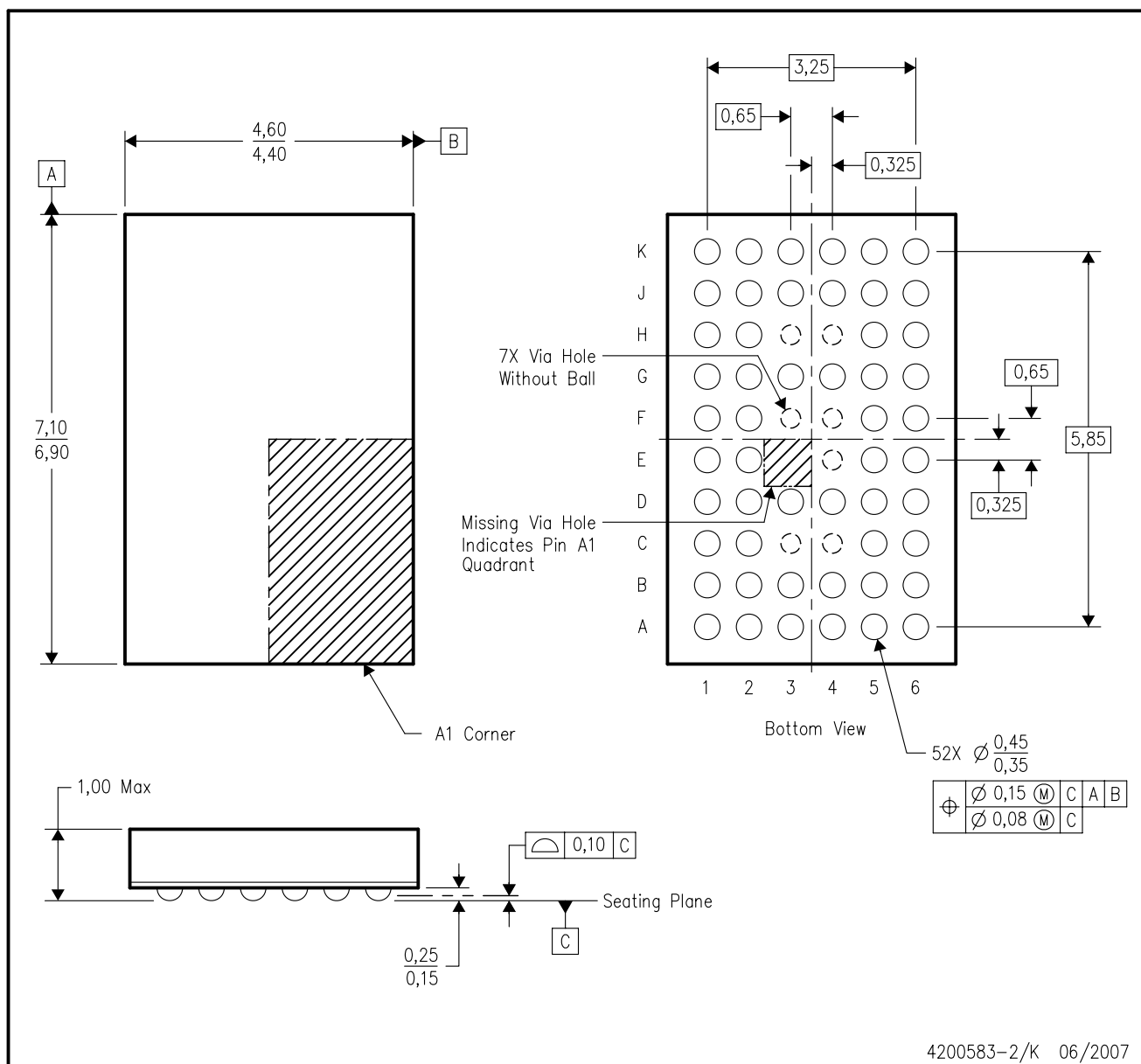
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCU877AGQLT	BGA MICROSTAR JUNIOR	GQL	52	250	336.6	336.6	28.6
CDCU877ARHAR	VQFN	RHA	40	2500	367.0	367.0	38.0
CDCU877ARHAT	VQFN	RHA	40	250	210.0	185.0	35.0
CDCU877AZQLR	BGA MICROSTAR JUNIOR	ZQL	52	1000	336.6	336.6	28.6
CDCU877AZQLT	BGA MICROSTAR JUNIOR	ZQL	52	250	336.6	336.6	28.6
CDCU877GQLR	BGA MICROSTAR JUNIOR	GQL	52	1000	336.6	336.6	28.6

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCU877GQLT	BGA MICROSTAR JUNIOR	GQL	52	250	336.6	336.6	28.6
CDCU877RHAR	VQFN	RHA	40	2500	367.0	367.0	38.0
CDCU877RHAT	VQFN	RHA	40	250	210.0	185.0	35.0
CDCU877ZQLR	BGA MICROSTAR JUNIOR	ZQL	52	1000	336.6	336.6	28.6
CDCU877ZQLT	BGA MICROSTAR JUNIOR	ZQL	52	250	336.6	336.6	28.6

GQL (R-PBGA-N52)

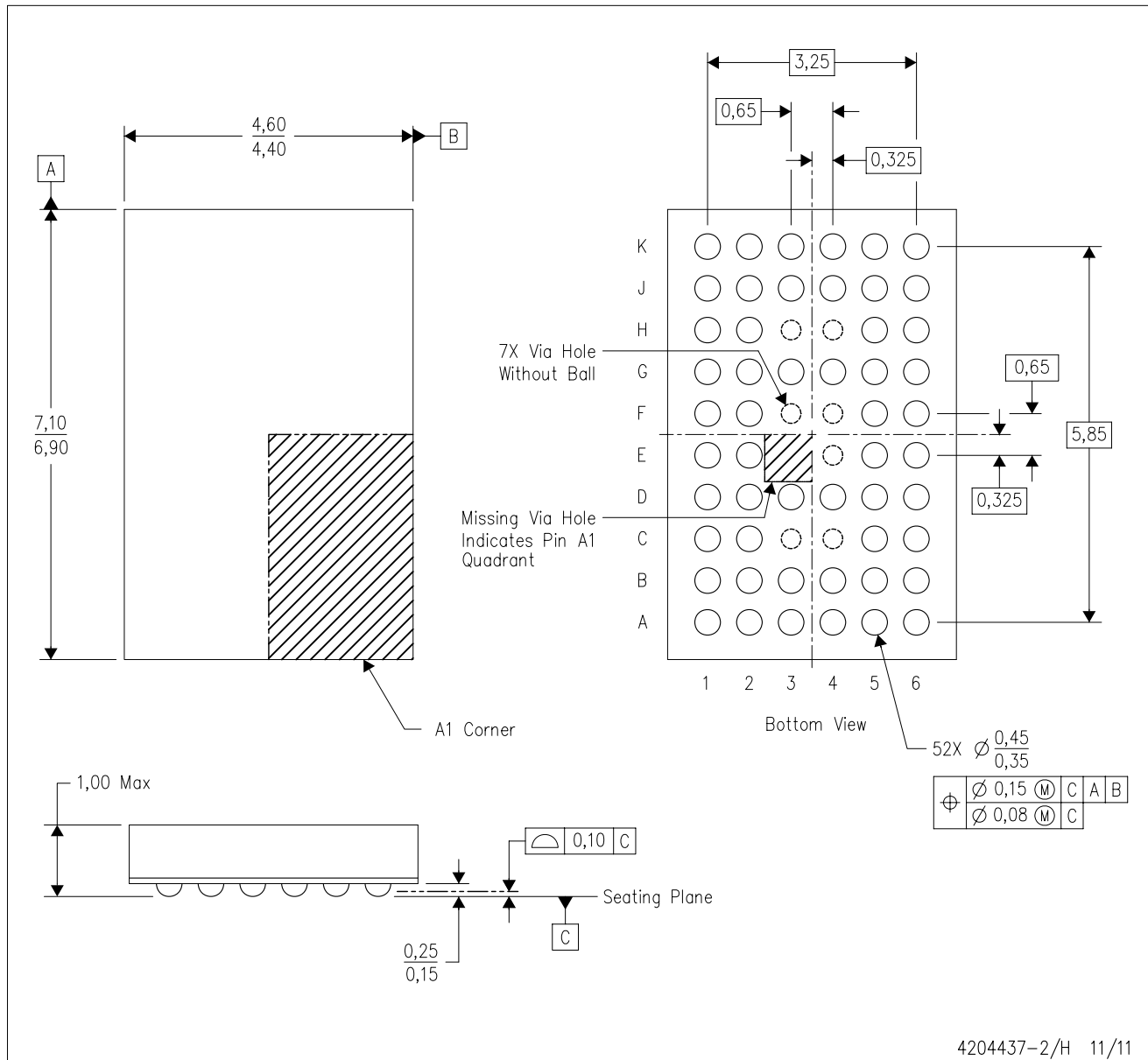
PLASTIC BALL GRID ARRAY



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Falls within JEDEC MO-285 variation BA-2.
 - This package is tin-lead (SnPb). Refer to the 52 ZQL package (drawing 4204437) for lead-free.

ZQL (R-PBGA-N52)

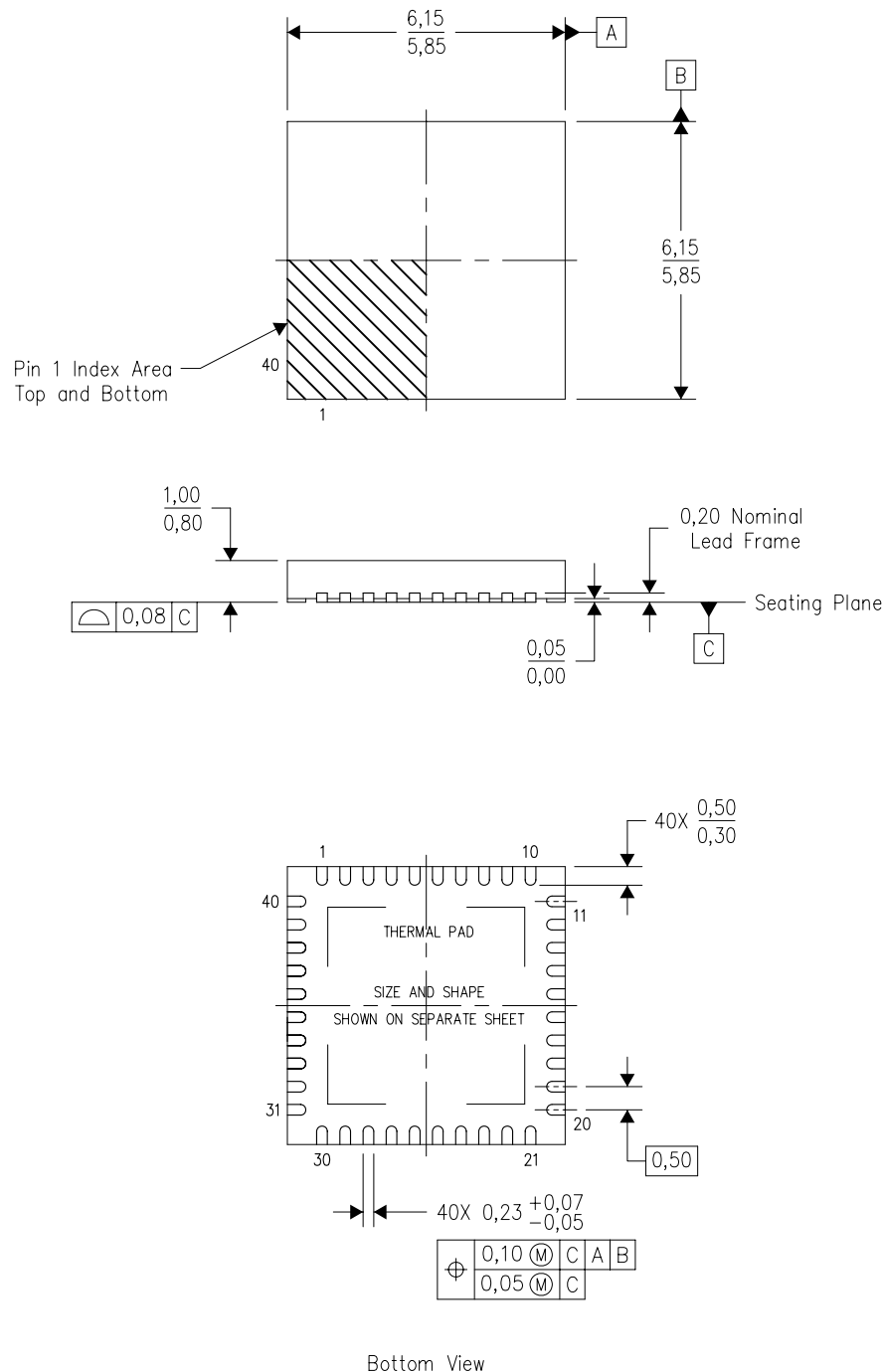
PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-285 variation BA-2.
 - D. This package is Pb-free. Refer to the 52 GQL package (drawing 4200583) for tin-lead (SnPb).

RHA (S-PVQFN-N40)

PLASTIC QUAD FLATPACK NO-LEAD



4204276/E 06/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) Package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - F. Package complies to JEDEC MO-220 variation VJJD-2.

THERMAL PAD MECHANICAL DATA

RHA (S-PVQFN-N40)

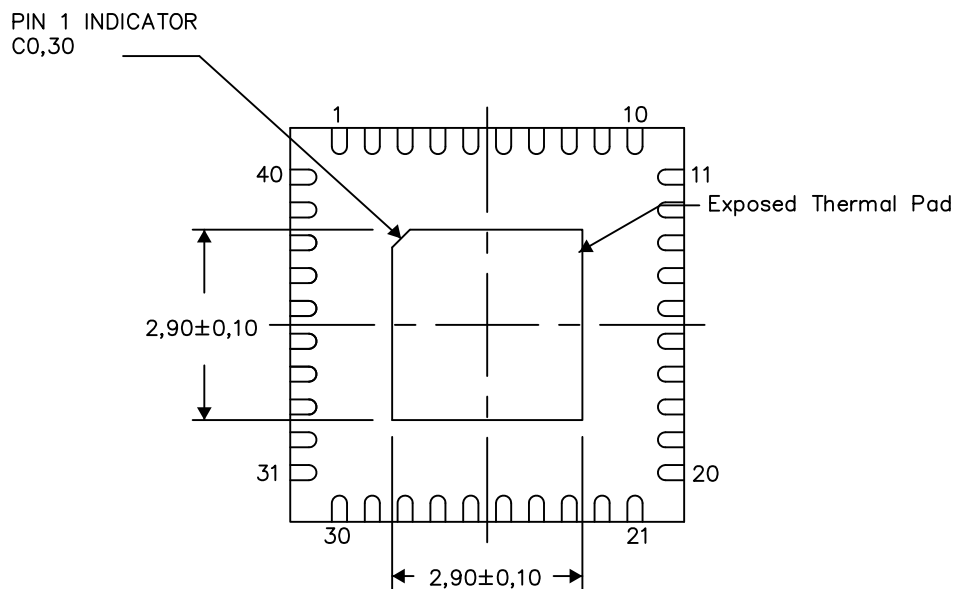
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

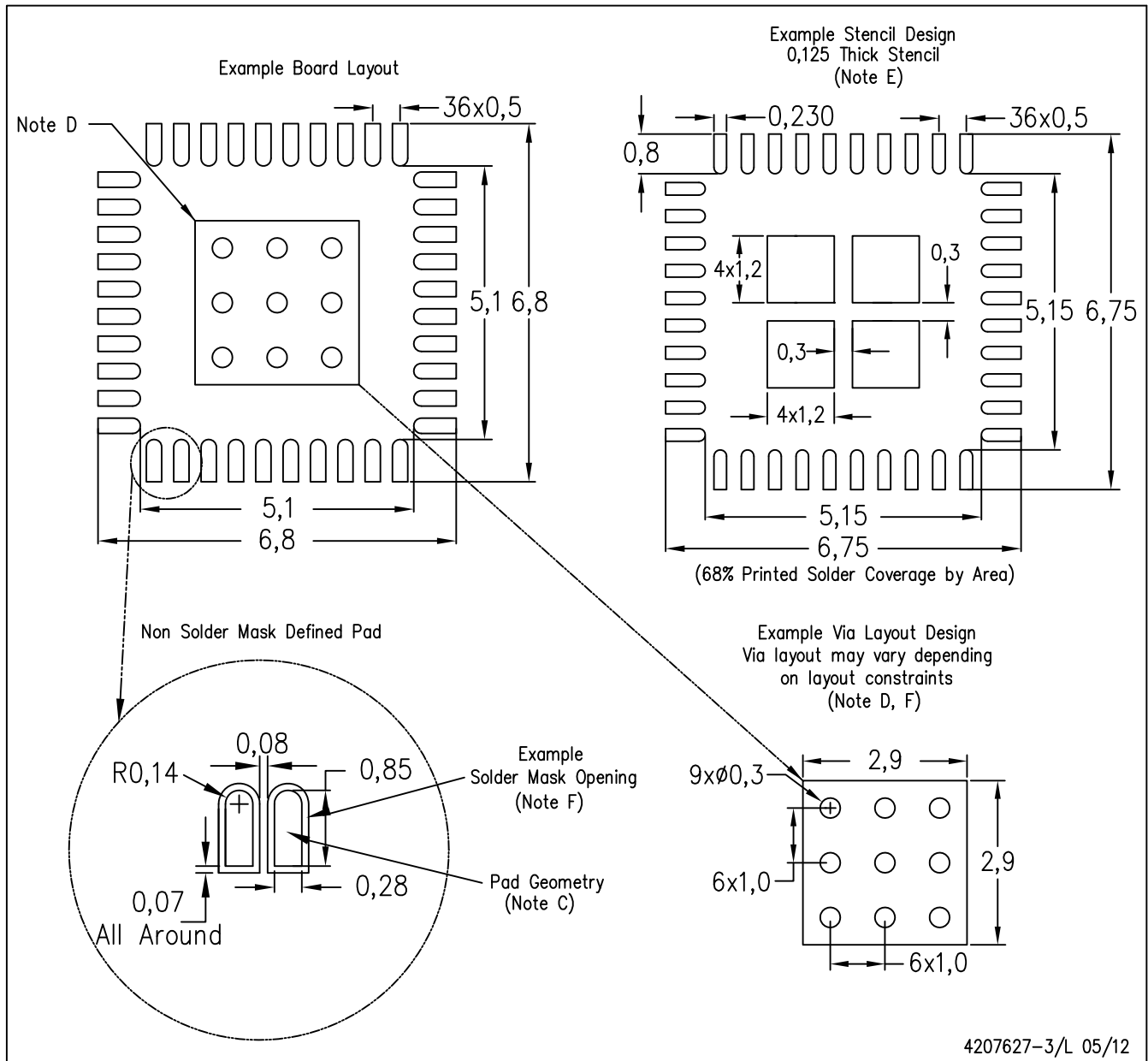
Exposed Thermal Pad Dimensions

4206355-3/Q 05/12

NOTES: A. All linear dimensions are in millimeters

RHA (S-PVQFN-N40)

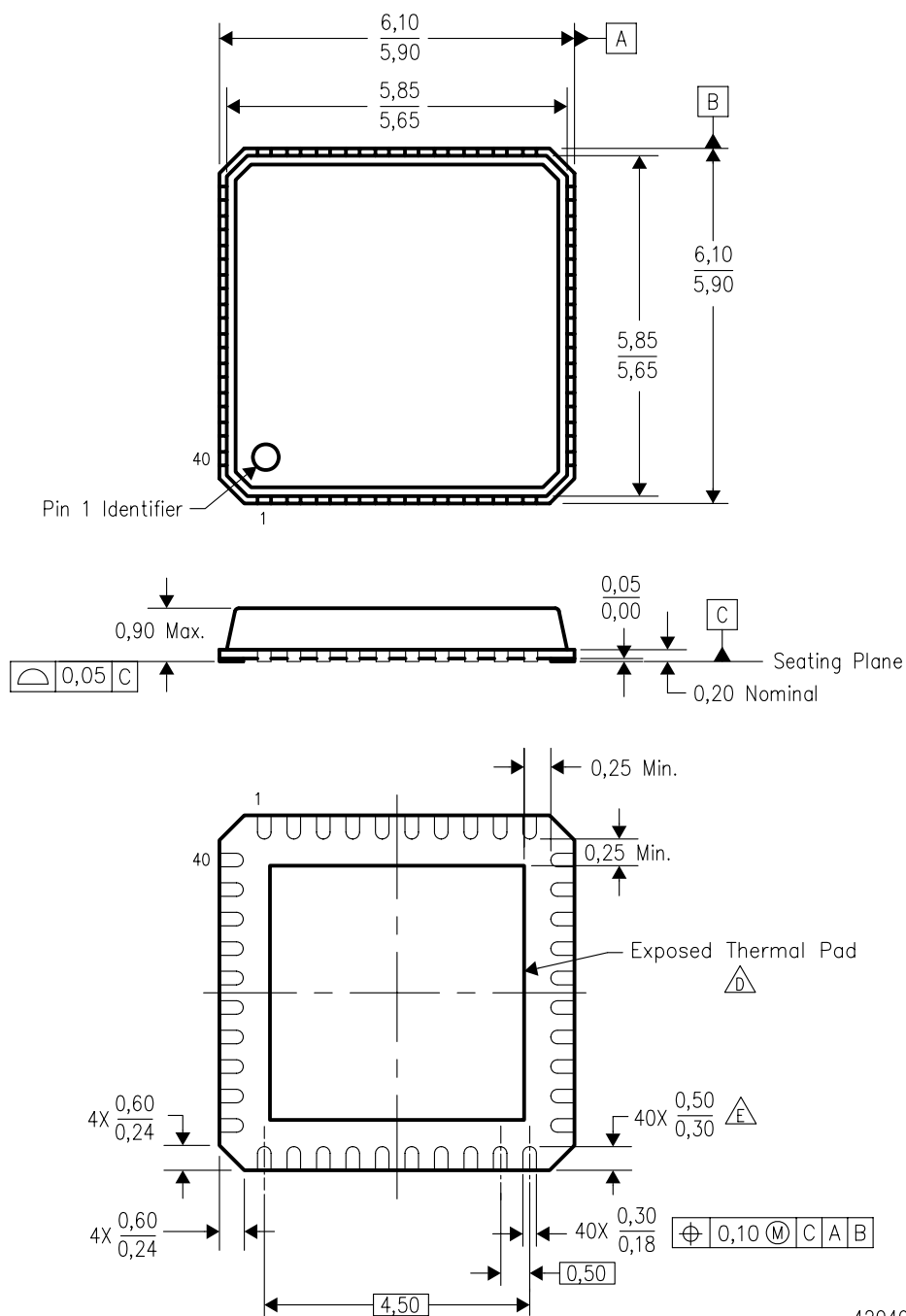
PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

RTB (S-PQFP-N40)

PLASTIC QUAD FLATPACK



4204967-2/E 05/07

- NOTES: A. All linear dimensions are in millimeters.
 Dimensioning and tolerancing per ASME Y14.5M-1994.
 B. This drawing is subject to change without notice.
 C. QFN (Quad Flatpack No-Lead) Package configuration.

The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
 Some products have selected lands extended past 0,50 length. See Product Data Sheet for details regarding specific land length exceptions.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46C and to discontinue any product or service per JESD48B. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components which meet ISO/TS16949 requirements, mainly for automotive use. Components which have not been so designated are neither designed nor intended for automotive use; and TI will not be responsible for any failure of such components to meet such requirements.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Mobile Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community e2e.ti.com