- **Phase-Lock Loop Clock Driver for Double Data-Rate Synchronous DRAM Applications**
- **Spread Spectrum Clock Compatible**
- **Operating Frequency: 60 to 140 MHz**
- **Low Jitter (cyc−cyc): ±75 ps**
- **Distributes One Differential Clock Input to Ten Differential Outputs**
- **Two-Line Serial Interface Provides Output Enable and Functional Control**
- **Outputs Are Put Into a High-Impedance State When the Input Differential Clocks Are <20 MHz**
- **48-Pin TSSOP Package**
- **Consumes <250-µA Quiescent Current**
- **External Feedback Pins (FBIN, $\overline{\text{FBIN}}$) Are Used to Synchronize the Outputs to the Input Clocks**

**DGG PACKAGE**
**(TOP VIEW)**

| | | | |
|---|---|---|---|
| GND | 1 | 48 | GND |
| $\overline{\text{Y0}}$ | 2 | 47 | $\overline{\text{Y5}}$ |
| Y0 | 3 | 46 | Y5 |
| $V_{DDQ}$ | 4 | 45 | $V_{DDQ}$ |
| Y1 | 5 | 44 | Y6 |
| $\overline{\text{Y1}}$ | 6 | 43 | $\overline{\text{Y6}}$ |
| GND | 7 | 42 | GND |
| GND | 8 | 41 | GND |
| $\overline{\text{Y2}}$ | 9 | 40 | $\overline{\text{Y7}}$ |
| Y2 | 10 | 39 | Y7 |
| $V_{DDQ}$ | 11 | 38 | $V_{DDQ}$ |
| SCLK | 12 | 37 | SDATA |
| CLK | 13 | 36 | $\overline{\text{FBIN}}$ |
| $\overline{\text{CLK}}$ | 14 | 35 | FBIN |
| $V_{DDI}$ | 15 | 34 | $V_{DDQ}$ |
| $AV_{DD}$ | 16 | 33 | FBOUT |
| AGND | 17 | 32 | $\overline{\text{FBOUT}}$ |
| GND | 18 | 31 | GND |
| $\overline{\text{Y3}}$ | 19 | 30 | $\overline{\text{Y8}}$ |
| Y3 | 20 | 29 | Y8 |
| $V_{DDQ}$ | 21 | 28 | $V_{DDQ}$ |
| Y4 | 22 | 27 | Y9 |
| $\overline{\text{Y4}}$ | 23 | 26 | $\overline{\text{Y9}}$ |
| GND | 24 | 25 | GND |

## description

The CDCV850 is a high-performance, low-skew, low-jitter zero delay buffer that distributes a differential clock input pair (CLK, $\overline{\text{CLK}}$) to ten differential pairs of clock outputs (Y[0:9], $\overline{\text{Y[0:9]}}$) and one differential pair of feedback clock outputs (FBOUT, $\overline{\text{FBOUT}}$). The clock outputs are controlled by the clock inputs (CLK, $\overline{\text{CLK}}$), the feedback clocks (FBIN, $\overline{\text{FBIN}}$), the 2-line serial interface (SDATA, SCLK), and the analog power input ($AV_{DD}$). A two-line serial interface can put the individual output clock pairs in a high-impedance state. When the $AV_{DD}$ terminal is tied to GND, the PLL is turned off and bypassed for test purposes.

The device provides a standard mode (100 Kbits/s) 2-line serial interface for device control. The implementation is as a slave/receiver. The device address is specified in the 2-line serial device address table. Both of the 2-line serial inputs (SDATA and SCLK) provide integrated pullup resistors (typically 100 kΩ).

Two 8-bit, 2-line serial registers provide individual enable control for each output pair. All outputs default to enabled at powerup. Each output pair can be placed in a high-impedance mode, when a low-level control bit is written to the control register. The registers must be accessed in sequential order (i.e., random access of the registers not supported). The serial interface circuit can be supplied with either 2.5 V or 3.3 V (at VDDI) in applications where this programming option is not required (after power up, all output pairs will then be enabled).

When the input frequency falls below a suggested detection frequency that is below 20 MHz (typically 10 MHz), the output pairs are put into a high-impedance condition, the PLL is shut down, and the device will enter a low power mode. The CDCV850 is also able to track spread spectrum clocking for reduced EMI.

Since the CDCV850 is based on PLL circuitry, it requires a stabilization time to achieve phase-lock of the PLL. This stabilization time is required following power up, as well as changes to various 2-line serial registers that affect the PLL. The CDCV850 is characterized for both commercial and industrial temperature ranges.

**AVAILABLE OPTIONS**

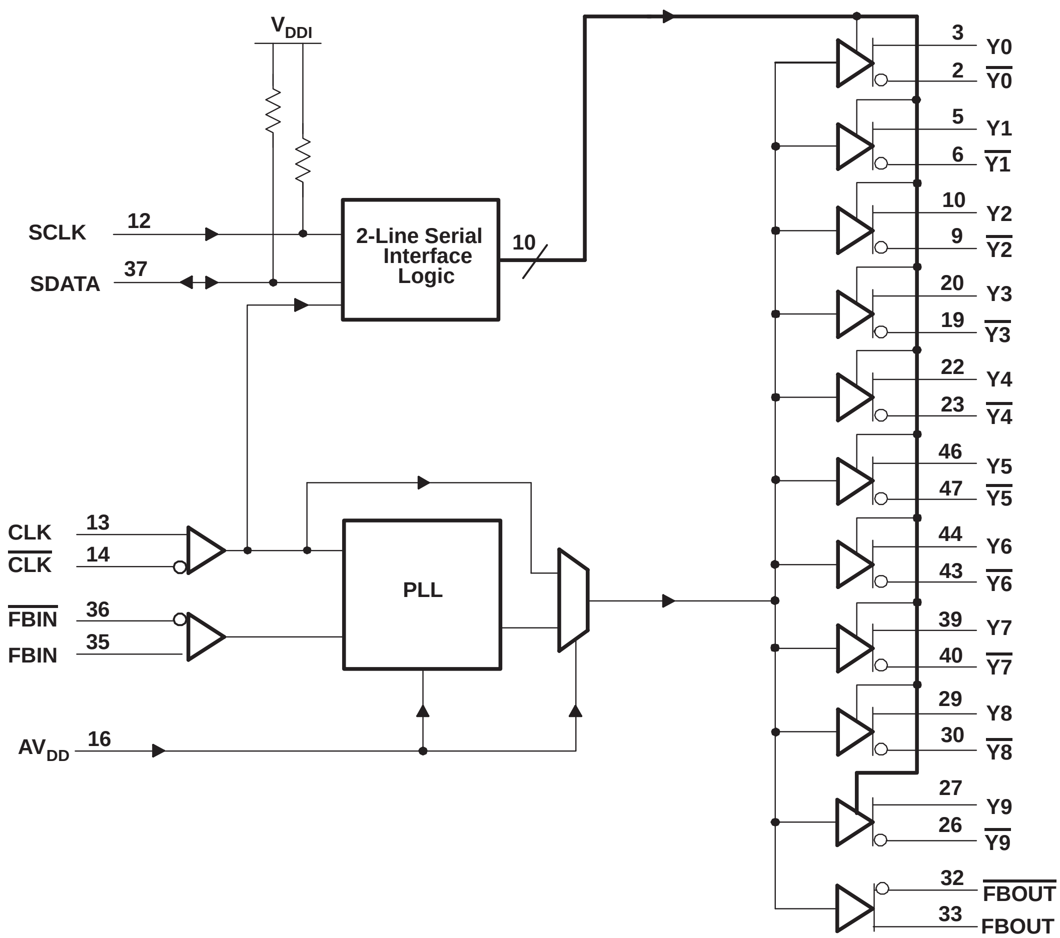
| $T_A$ | PACKAGED DEVICES |
|---|---|
| | TSSOP (DGG) |
| 0°C to 85°C | CDCV850DGG |
| −40°C to 85°C | CDCV850IDGG |

**FUNCTION TABLE**
**(Select Functions)**

| INPUTS | | | OUTPUTS† | | | | PLL |
|---|---|---|---|---|---|---|---|
| $AV_{DD}$ | CLK | $\overline{CLK}$ | Y[0:9] | $\overline{Y[0:9]}$ | FBOUT | $\overline{FBOUT}$ | |
| GND | L | H | L | H | L | H | Bypassed/Off |
| GND | H | L | H | L | H | L | Bypassed/Off |
| 2.5 V (nom) | L | H | L | H | L | H | On |
| 2.5 V (nom) | H | L | H | L | H | L | On |
| 2.5 V (nom) | <20 MHz | <20 MHz | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Off |

† Each output pair (except FBOUT, $\overline{FBOUT}$) can be put into a high-impedance state through the 2-line serial interface.

## functional block diagram



## Terminal Functions

| TERMINAL NAME | TERMINAL NO. | I/O | DESCRIPTION |
|---|---|---|---|
| AGND | 17 | | Ground for 2.5-V analog supply |
| $AV_{DD}$ | 16 | | 2.5-V analog supply |
| CLK, $\overline{\text{CLK}}$ | 13, 14 | I | Differential clock input |
| FBIN, $\overline{\text{FBIN}}$ | 35, 36 | I | Feedback differential clock input |
| $\overline{\text{FBOUT}}$, FBOUT | 32, 33 | O | Feedback differential clock output |
| GND | 1, 7, 8, 18, 24, 25, 31, 41, 42, 48 | | Ground |
| SCLK | 12 | I | Clock input for 2-line serial interface |
| SDATA | 37 | I/O | Data input/output for 2-line serial interface |
| $V_{DDQ}$ | 4, 11, 21, 28, 34, 38, 45 | | 2.5-V supply |
| $V_{DDI}$ | 15 | I | 2.5-V or 3.3-V supply for 2-line serial interface |
| Y[0:9] | 3, 5, 10, 20, 22, 27, 29, 39, 44, 46 | O | Buffered output copies of input clock, CLK |
| $\overline{\text{Y[0:9]}}$ | 2, 6, 9, 19, 23, 26, 30, 40, 43, 47 | O | Buffered output copies of input clock, $\overline{\text{CLK}}$ |

## absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range: $V_{DDQ}$, $AV_{DD}$ . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . −0.5 V to 3.6 V
$V_{DDI}$ . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . −0.5 V to 4.6 V
Input voltage range: $V_I$ (except SCLK and SDATA) (see Notes 1 and 2) . . . . . . . . –0.5 V to $V_{DDQ}$ + 0.5 V
$V_I$ (SCLK, SDATA) (see Notes 1 and 2) . . . . . . . . . . . . . . . . . . . –0.5 V to $V_{DDI}$ + 0.5 V
Output voltage range: $V_O$ (except SDATA) (see Notes 1 and 2) . . . . . . . . . . . . . . . . . –0.5 V to $V_{DDQ}$ + 0.5 V
$V_O$ (SDATA) (see Notes 1 and 2) . . . . . . . . . . . . . . . . . . . . . . –0.5 V to $V_{DDQ}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0 or $V_I$ > $V_{DDQ}$) . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . ±50 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{DDQ}$) . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . ±50 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{DDQ}$) . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DGG package . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 89°C/W
Storage temperature range $T_{stg}$ . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 3.6 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51.

## recommended operating conditions (see Note 4)

| | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Supply voltage | $V_{DDQ}$, $AV_{DD}$ | | 2.3 | | 2.7 | V |
| | $V_{DDI}$ (see Note 5) | | 2.3 | | 3.6 | |
| Low level input voltage, $V_{IL}$ | CLK, $\overline{CLK}$, HCSL Buffer only | | | 0 | 0.24 | V |
| | CLK, $\overline{CLK}$ | | −0.3 | | $V_{DDQ}$ − 0.4 | |
| | FBIN, $\overline{FBIN}$ | | | | $V_{DDQ}$/2 − 0.18 | |
| | SDATA, SCLK | | | | 0.3 × $V_{DDI}$ | |
| High level input voltage, $V_{IH}$ | CLK, $\overline{CLK}$, HCSL Buffer only | | 0.66 | 0.71 | | V |
| | CLK, $\overline{CLK}$ | | 0.4 | | $V_{DDQ}$ + 0.3 | |
| | FBIN, $\overline{FBIN}$ | | $V_{DDQ}$/2 + 0.18 | | | |
| | SDATA, SCLK | | 0.7 × $V_{DDI}$ | | | |
| DC input signal voltage (see Note 6) | | | –0.3 | | $V_{DDQ}$ + 0.3 | V |
| Differential input signal voltage, $V_{ID}$ (see Note 7) | DC | CLK, FBIN | 0.36 | | $V_{DDQ}$ + 0.6 | V |
| | AC | CLK, FBIN | 0.2 | | $V_{DDQ}$ + 0.6 | |
| Input differential pair cross-voltage, $V_{IX}$ (see Note 8) | | | 0.45×($V_{IH}$−$V_{IL}$) | | 0.55×($V_{IH}$−$V_{IL}$) | V |
| High-level output current, $I_{OH}$ | | | | | −12 | mA |
| Low-level output current, $I_{OL}$ | | | | | 12 | V |
| | SDATA | | | | 3 | mA |
| Input slew rate, SR (see Figure 8) | | | 1 | | 4 | V/ns |
| SSC modulation frequency | | | 30 | | 33.3 | kHz |
| SSC clock input frequency deviation | | | 0 | | −0.50 | kHz |
| Operating free-air temperature, $T_A$ | Commericial | | 0 | | 85 | °C |
| | Industrial | | −40 | | 85 | |

NOTES: 4. Unused inputs must be held high or low to prevent them from floating.
5. All devices on the serial interface bus, with input levels related to $V_{DDI}$, must have one common supply line to which the pullup resistor is connected to.
6. DC input signal voltage specifies the allowable dc execution of differential input.
7. Differential input signal voltage specifies the differential voltage |VTR − VCP| required for switching, where VTR is the true input level and VCP is the complementary input level.
8. Differential cross-point voltage is expected to track variations of VCC and is the voltage at which the differential signals must be crossing.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP[†] | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | Input voltage | All inputs | $V_{DDQ}$ = 2.3 V, $I_I$ = –18 mA | | | –1.2 | V |
| $V_{OH}$ | High-level output voltage | | $V_{DDQ}$ = min to max, $I_{OH}$ = –1 mA | $V_{DDQ}$ – 0.1 | | | V |
| | | | $V_{DDQ}$ = 2.3 V, $I_{OH}$ = –12 mA | 1.7 | | | |
| $V_{OL}$ | Low-level output voltage | | $V_{DDQ}$ = min to max, $I_{OL}$ = 1 mA | | | 0.1 | V |
| | | | $V_{DDQ}$ = 2.3 V, $I_{OL}$ = 12 mA | | | 0.6 | |
| | | SDATA | $V_{DDI}$ = 3.0 V, $I_{OL}$ = 3 mA | | | 0.4 | |
| $I_{OH}$ | High-level output current | | $V_{DDQ}$ = 2.3 V, $V_O$ = 1 V | –18 | –32 | | mA |
| $I_{OL}$ | Low-level output current | | $V_{DDQ}$ = 2.3 V, $V_O$ = 1.2 V | 26 | 35 | | mA |
| $V_O$ | Output voltage swing | | For load condition see Figure 3 | 1.1 | | $V_{DDQ}$ – 0.4 | V |
| $V_{OX}$ | Output differential cross voltage | | | $V_{DDQ}$/2 − 0.2 | $V_{DDQ}$/2 | $V_{DDQ}$/2 + 0.2 | V |
| $I_I$ | Input current | SDATA, SCLK | $V_{DDQ}$ = 3.6 V, $V_I$ = 0 V to 3.6 V | | | +10/−50 | µA |
| | | CLK, FBIN | $V_{DDQ}$ = 2.7 V, $V_I$ = 0 V to 2.7 V | | | ±10 | µA |
| $I_{OZ}$ | High-impedance-state output current | | $V_{DDQ}$ = 2.7 V, $V_O$ = $V_{DDQ}$ or GND | | | ±10 | µA |
| $I_{DDPD}$ | Power-down current on $V_{DDQ}$ + $AV_{DD}$ | | CLK at 0 MHz; Σ of $I_{DD}$ and $AI_{DD}$ | | 150 | 250 | µA |
| | Power down current on $V_{DDI}$ | | CLK at 0 MHz; $V_{DDQ}$ = 3.6 V | | 3 | 20 | µA |
| $I_{DD}$ | Dynamic current on $V_{DDQ}$ | | $V_{DDQ}$ = 2.7 V, $f_O$ = 100 MHz All differential output pairs are terminated with 120 Ω / $C_L$ = 4 pF | | 205 | 230 | mA |
| $AI_{(DD)}$ | Supply current on $AV_{DD}$ | | $AV_{DD}$ = 2.7 V, $f_O$ = 100 MHz | | 4 | 6 | mA |
| $I_{DDI}$ | Supply current on $V_{DDI}$ | | $V_{DDI}$ = 3.6 V; SCLK and SDATA = 3.6 V | | 1 | 2 | mA |
| $C_I$ | Input capacitance | | $V_{DDQ}$ = 2.5 V, $V_I$ = $V_{DDQ}$ or GND | 2 | 2.5 | 3 | pF |
| $C_O$ | Output capacitance | | $V_{DDQ}$ = 2.5 V, $V_O$ = $V_{DDQ}$ or GND | 2.5 | 3 | 3.5 | pF |

† All typical values are at respective nominal $V_{DDQ}$.
‡ The value of $V_{OC}$ is expected to be |VTR + VCP|/2. In case of each clock directly terminated by a 120-Ω resistor, where VTR is the true input signal voltage and VCP is the complementary input signal voltage (see Figure 3).

### timing requirements over recommended ranges of supply voltage and operating free-air temperature

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $f_{(CLK)}$ | Clock frequency | 60 | 140 | MHz |
| | Input clock duty cycle | 40% | 60% | |
| | Stabilization time† | | 10 | μs |

† Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLK. Until phase lock is obtained, the specifications for propagation delay, skew, and jitter parameters given in the switching characteristics table are not applicable. This parameter does not apply for input modulation under SSC application.

### timing requirements for the 2-line serial interface over recommended ranges of operating free-air temperature and VDDI from 3.3 V to 3.6 V (see Figure 10)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $f_{(SCLK)}$ | SCLK frequency | | 100 | kHz |
| $t_{(BUS)}$ | Bus free time | 4.7 | | μs |
| $t_{su(START)}$ | START setup time† | 4.7 | | μs |
| $t_{h(START)}$ | START hold time† | 4.0 | | μs |
| $t_{w(SCLL)}$ | SCLK low pulse duration | 4.7 | | μs |
| $t_{w(SCLH)}$ | SLCK high pulse duration | 4.0 | | μs |
| $t_{r(SDATA)}$ | SDATA input rise time | | 1000 | ns |
| $t_{f(SDATA)}$ | SDATA input fall time | | 300 | ns |
| $t_{su(SDATA)}$ | SDATA setup time | 250 | | ns |
| $t_{h(SDATA)}$ | SDATA hold time | 0 | | ns |
| $t_{su(STOP)}$ | STOP setup time | 4 | | μs |

† This conforms to I2C specification, version 2.1.

## switching characteristics over recommended ranges of operating free-air temperature (unless otherwisw noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{pd}$ | Propagation delay time | | Test mode/CLK to any output | | 4 | | ns |
| $t_{PHL}$ | High-to low-level propagation delay time | | SCLK to SDATA (acknowledge) | | 500[†] | | ns |
| $t_{en}$ | Output enable time | | Test mode/SDATA to Y-output | | 85 | | ns |
| $t_{dis}$ | Output disable time | | Test mode/SDATA to Y-output | | 35 | | ns |
| $t_{jit(per)}$ | Jitter (period), See Figure 6 | | 100/133 MHz | −30 | | 30 | ps |
| $t_{jit(cc)}$ | Jitter (cycle-to-cycle), See Figure 3 | | 100/133 MHz | −30 | | 30 | ps |
| $t_{jit(hper)}$ | Half-period jitter, See Figure 7 | | 100/133 MHz | −75 | | 75 | ps |
| $t_{(\varnothing)}$ | Static phase offset, See Figure 4a | 0°C to 85°C | 100 MHz/VID on CLK = 0.71 V[‡] | −120 | | 120 | ps |
| | | | 100 MHz/VID on CLK = 0.59 V[§] | −50 | | 160 | |
| | | | 100 MHz/VID on CLK = 0.82 V[¶] | −170 | | 70 | |
| | | | 133 MHz/VID on CLK = 0.71 V[¶] | −50 | | 180 | |
| | | −40°C to 85°C | 100 MHz/VID on CLK = 0.71 V[‡] | −160 | | 80 | ps |
| | | | 100 MHz/VID on CLK = 0.59 V[§] | −90 | | 120 | |
| | | | 100 MHz/VID on CLK = 0.82 V[¶] | −210 | | 30 | |
| | | | 133 MHz/VID on CLK = 0.71 V[¶] | −80 | | 150 | |
| $td_{(\varnothing)}$[#] | Dynamic phase offset, SSC on, See Figure 4b and Figure 9 | | 100 MHz/VID on CLK = 0.71 V[‡] | −190 | | 190 | ps |
| | | | 133 MHz/VID on CLK = 0.71 V[‡] | −140 | | 140 | ps |
| | Dynamic phase offset, SSC off, See Figure 4b | | 100 MHz/VID on CLK = 0.71 V[‡] | −160 | | 160 | ps |
| | | | 133 MHz/VID on CLK = 0.71 V[‡] | −130 | | 130 | ps |
| $t_{slr(o)}$ | Output clock slew rate, terminated with 120 Ω/14 pF, See Figures 1 and 8 | | | 1 | | 2 | V/ns |
| $t_{slr(o)}$ | Output clock slew rate, terminated with 120 Ω/4 pF, See Figures 1 and 8 | | | 1 | | 3 | V/ns |
| $t_{sk(o)}$[‖] | Output skew, See Figure 5 | | | | | 75 | ps |
| | SSC modulation frequency | | | 30 | | 33.3 | kHz |
| | SSC clock input frequency deviation | | | 0.00 | | −0.50 | % |

[†] This time is for a PLL frequency of 100 MHz.
[‡] According CK00 spec: 6 x $I_{ref}$ at 50 Ω and $R_{ref}$ = 475 Ω
[§] According CK00 spec: 5 x $I_{ref}$ at 50 Ω and $R_{ref}$ = 475 Ω
[¶] According CK00 spec: 7 x $I_{ref}$ at 50 Ω and $R_{ref}$ = 475 Ω
[#] The parameter is assured by design but cannot be 100% production tested.
[‖] All differential output pins are terminated with 120 Ω/4 pF

## 2-line serial interface

### 2-line serial interface slave address

| A7 | A6 | A5 | A4 | A3 | A2 | A1 | R/$\overline{W}$ |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 |

Writing to the device is accomplished by sequentially sending the device address $D2_H$, the dummy bytes (command code and the number of bytes), and the data bytes. This sequence is illustrated in the following tables:

| 1 bit | 7 bits | 1 bit | 1 bit | 8 bits | 1 bit | 8 bits |
|---|---|---|---|---|---|---|
| Start Bit | Slave Address | R/W | Ack | Command Code | Ack | Byte Count = N |

| Ack | Data Byte 0 | Ack | Data Byte 1 | Ack | ••••• | Data Byte N | Ack | Stop |
|---|---|---|---|---|---|---|---|---|
| 1 bit | 8 bits | 1 bit | 8 bits | 1 bit | | 8 bits | 1 bit | 1 bit |

### 2-line serial interface configuration command bitmap

The 2-line serial command bytes are used to control the output clock pairs (Y[0:9], $\overline{Y[0:9]}$). The output clock pairs are enabled after power up. During normal operation, the clock pairs can be disabled (set Hi-Z) or enabled (running) by writing the corresponding bit to the data bytes in the following tables:

**Byte 0: Enable/Disable Register**
**(H = Enable, L = Disable)**

| BIT | PINS | INITIAL VALUE | DESCRIPTION |
|---|---|---|---|
| 7 | 3, 2 | H | Y0, $\overline{Y0}$ |
| 6 | 5, 6 | H | Y1, $\overline{Y1}$ |
| 5 | 10, 9 | H | Y2, $\overline{Y2}$ |
| 4 | 20, 19 | H | Y3, $\overline{Y3}$ |
| 3 | 22, 23 | H | Y4, $\overline{Y4}$ |
| 2 | 46, 47 | H | Y5, $\overline{Y5}$ |
| 1 | 44, 43 | H | Y6, $\overline{Y6}$ |
| 0 | 39, 40 | H | Y7, $\overline{Y7}$ |

**Byte 1: Enable/Disable Register**
**(H = Enable, L = Disable)**

| BIT | PINS | INITIAL VALUE | DESCRIPTION |
|---|---|---|---|
| 7 | 29, 30 | H | Y8, $\overline{Y8}$ |
| 6 | 27, 26 | H | Y9, $\overline{Y9}$ |
| 5 | − | L | Reserved |
| 4 | − | L | Reserved |
| 3 | − | L | Reserved |
| 2 | − | L | Reserved |
| 1 | − | L | Reserved |
| 0 | − | L | Reserved |

## PARAMETER MEASUREMENT INFORMATION

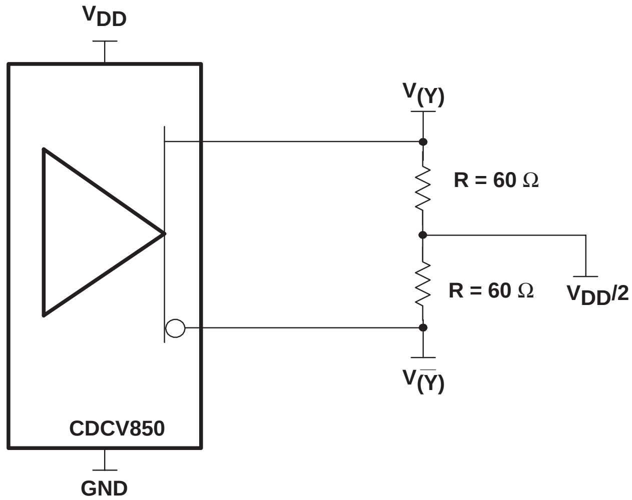



**Figure 1. IBIS Model Output Load (used for slew rate measurement)**

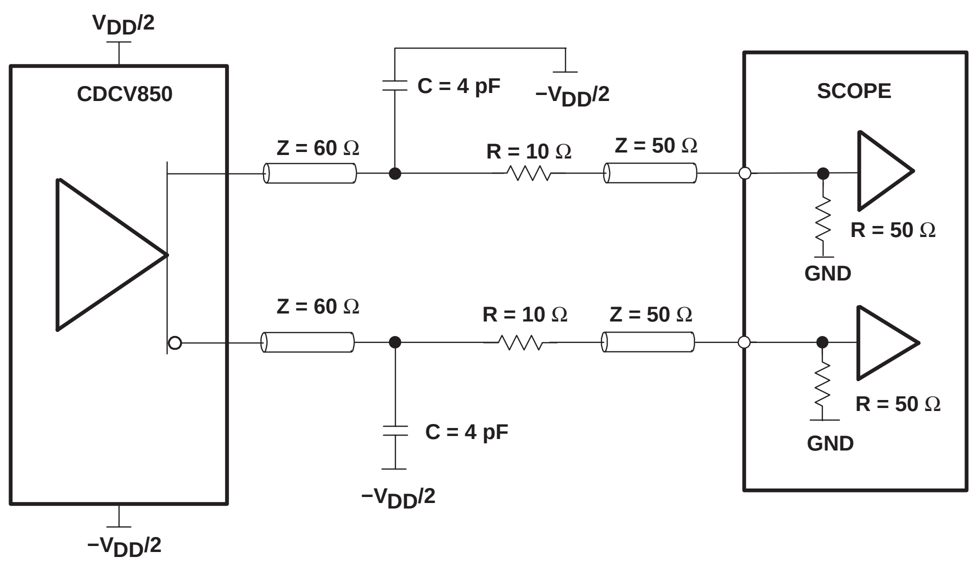
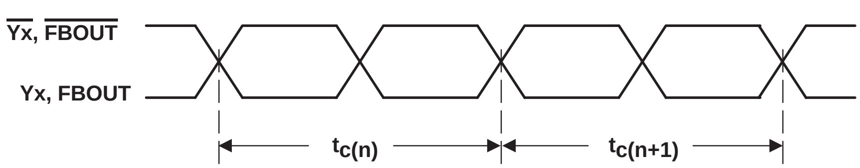


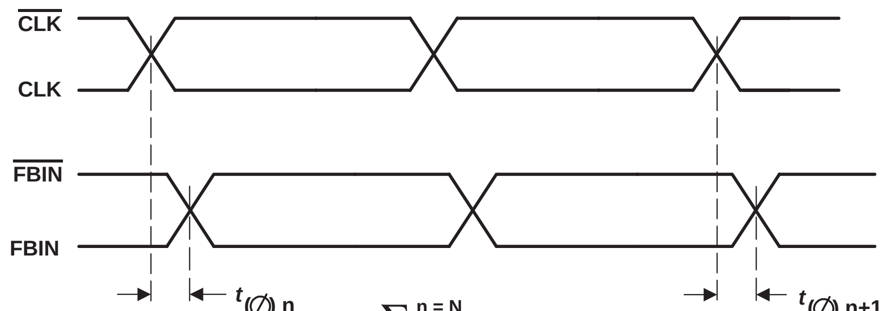

**Figure 2. Output Load Test Circuit**




$$t_{jit(cc)} = t_{c(n)} - t_{c(n+1)}$$

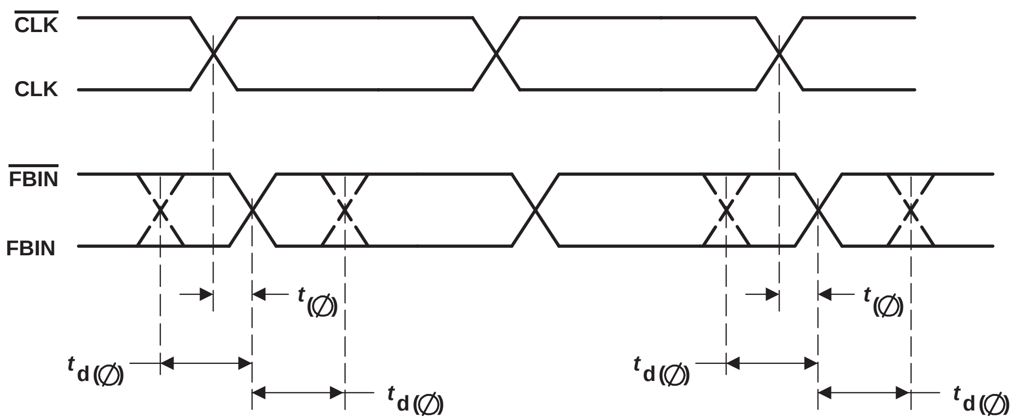
**Figure 3. Cycle-to-Cycle Jitter**

## PARAMETER MEASUREMENT INFORMATION




$$t_{(\varnothing)} = \frac{\sum_{1}^{n=N} t_{(\varnothing)n}}{N}$$ **(N is a large number of samples)**

**(a) Static Phase Offset**




**(b) Dynamic Phase Offset**

**Figure 4. Static Phase Offset**

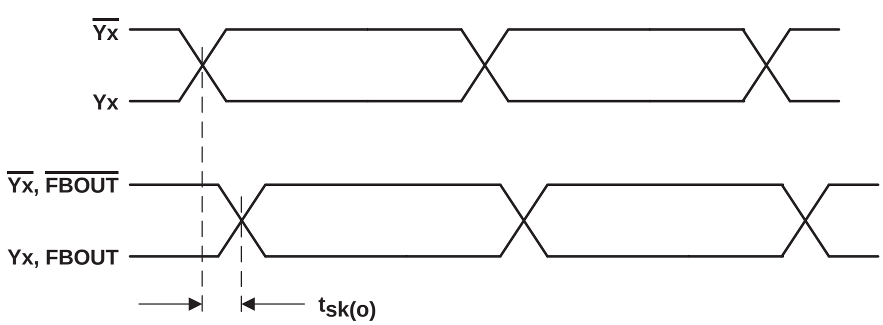
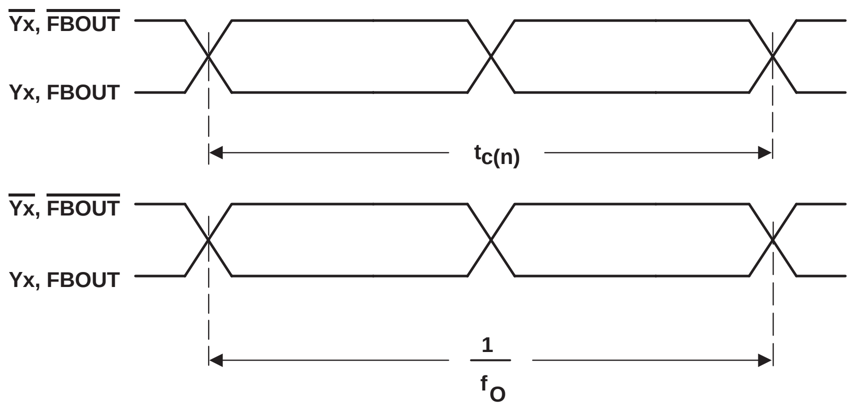


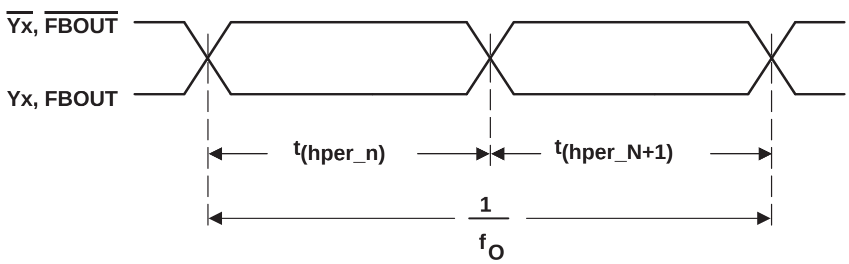

**Figure 5. Output Skew**

## PARAMETER MEASUREMENT INFORMATION




$$t_{jit(per)} = t_{c(n)} - \frac{1}{f_O}$$

**Figure 6. Period Jitter**




$$t_{jit(hper)} = t_{(hper\_n)} - \frac{1}{2xf_O}$$

**Figure 7. Half-Period Jitter**

## PARAMETER MEASUREMENT INFORMATION

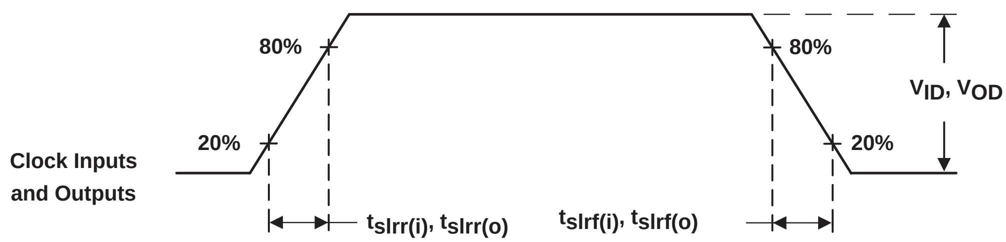



Figure 8. Input and Output Slew Rates

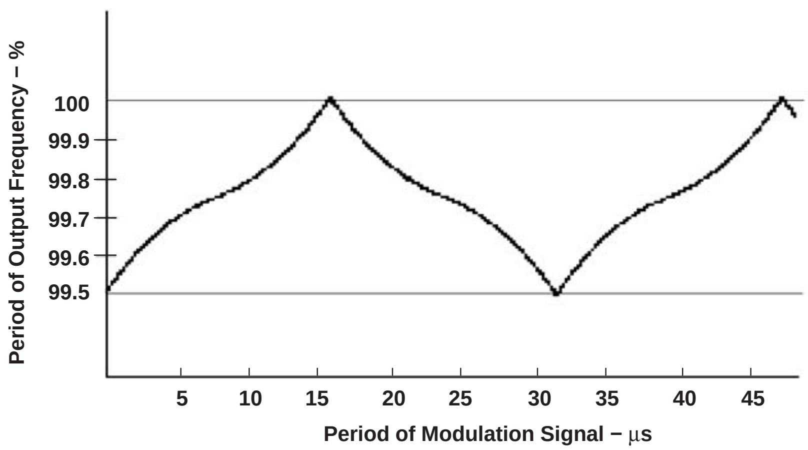
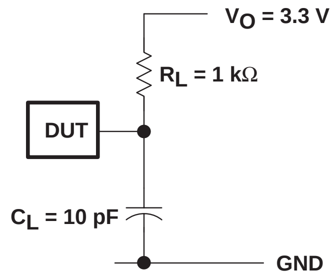
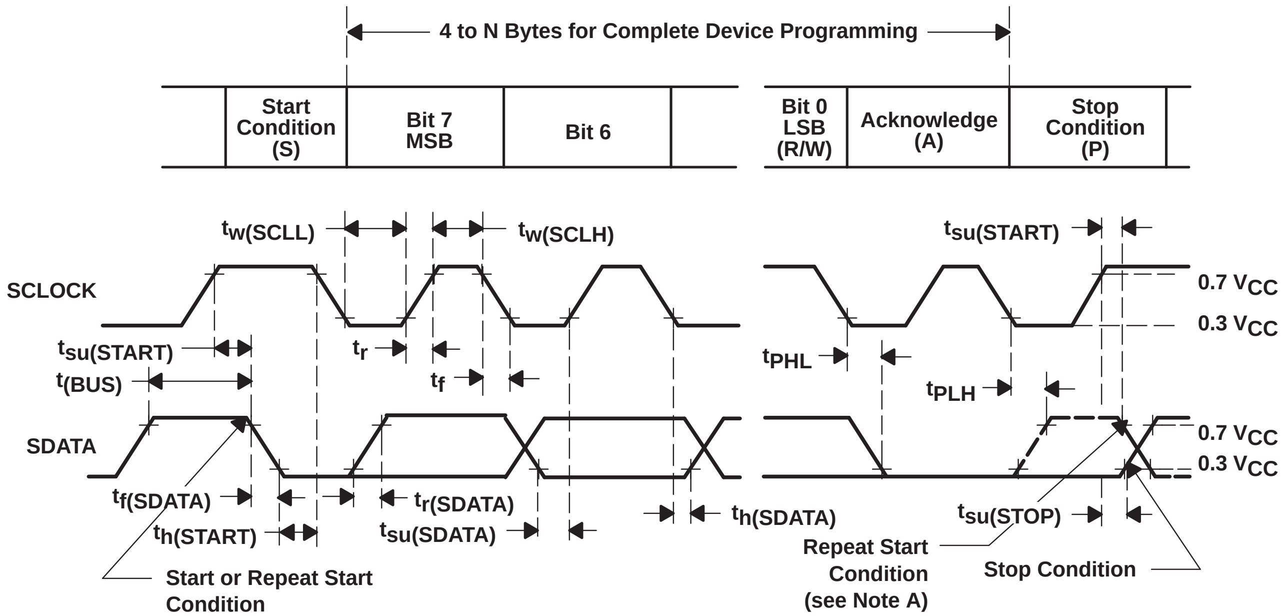



Figure 9. SSC Modulation Profile




TEST CIRCUIT




VOLTAGE WAVEFORMS

| BYTE | DESCRIPTION |
|---|---|
| 1 | Slave Address |
| 2 | Common (Dummy Value, Ignored) |
| 3 | Byte Count = N |
| 4 | Data Byte 0 |
| 5 − N | Data Byte 1 − N |

NOTE A: The repeat start condition is supported. If PWRDWN# is asserted SDATA will be set to off-state, high impedance.

**Figure 10. Propagation Delay Times, $t_r$ and $t_f$**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/ Ball Finish | MSL Peak Temp (3) | Samples (Requires Login) |
|---|---|---|---|---|---|---|---|---|---|
| CDCV850DGG | ACTIVE | TSSOP | DGG | 48 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| CDCV850DGGG4 | ACTIVE | TSSOP | DGG | 48 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| CDCV850DGGR | ACTIVE | TSSOP | DGG | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| CDCV850DGGRG4 | ACTIVE | TSSOP | DGG | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| CDCV850IDGG | ACTIVE | TSSOP | DGG | 48 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| CDCV850IDGGG4 | ACTIVE | TSSOP | DGG | 48 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| CDCV850IDGGR | OBSOLETE | TSSOP | DGG | 48 | | TBD | Call TI | Call TI | |
| CDCV850IDGGRG4 | OBSOLETE | TSSOP | DGG | 48 | | TBD | Call TI | Call TI | |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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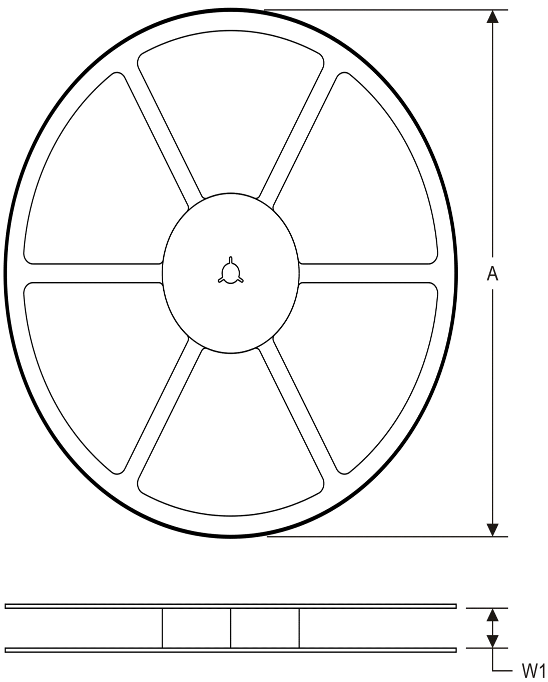
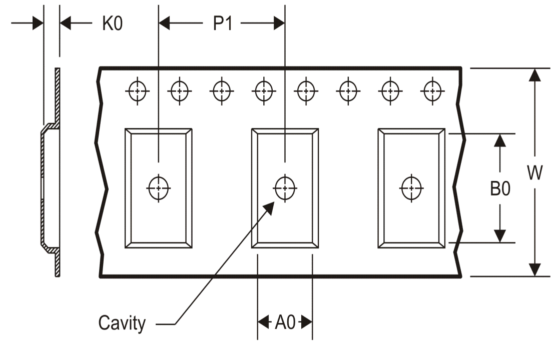
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**




**TAPE DIMENSIONS**



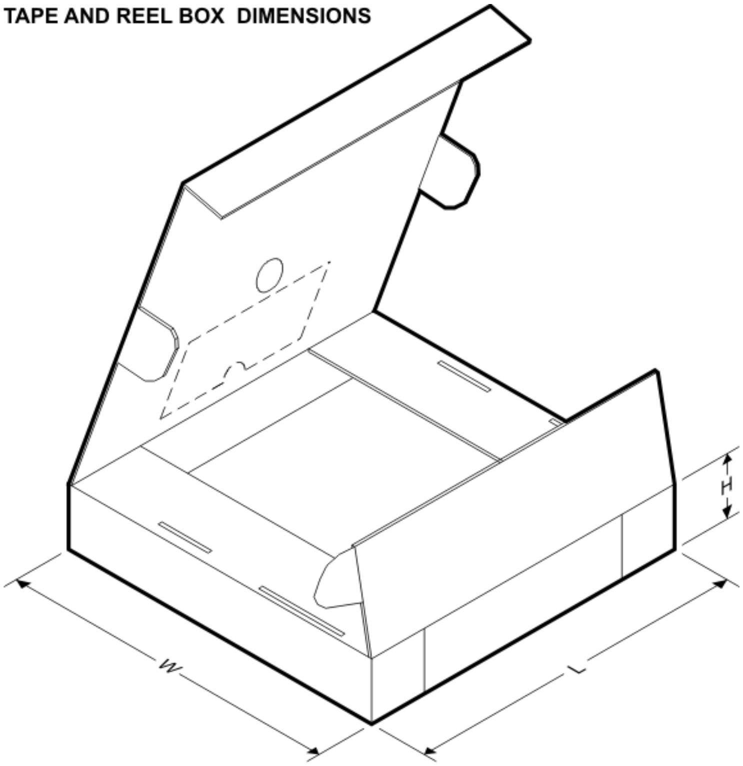

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**TAPE AND REEL INFORMATION**

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CDCV850DGGR | TSSOP | DGG | 48 | 2000 | 330.0 | 24.4 | 8.6 | 15.8 | 1.8 | 12.0 | 24.0 | Q1 |

## TAPE AND REEL BOX DIMENSIONS

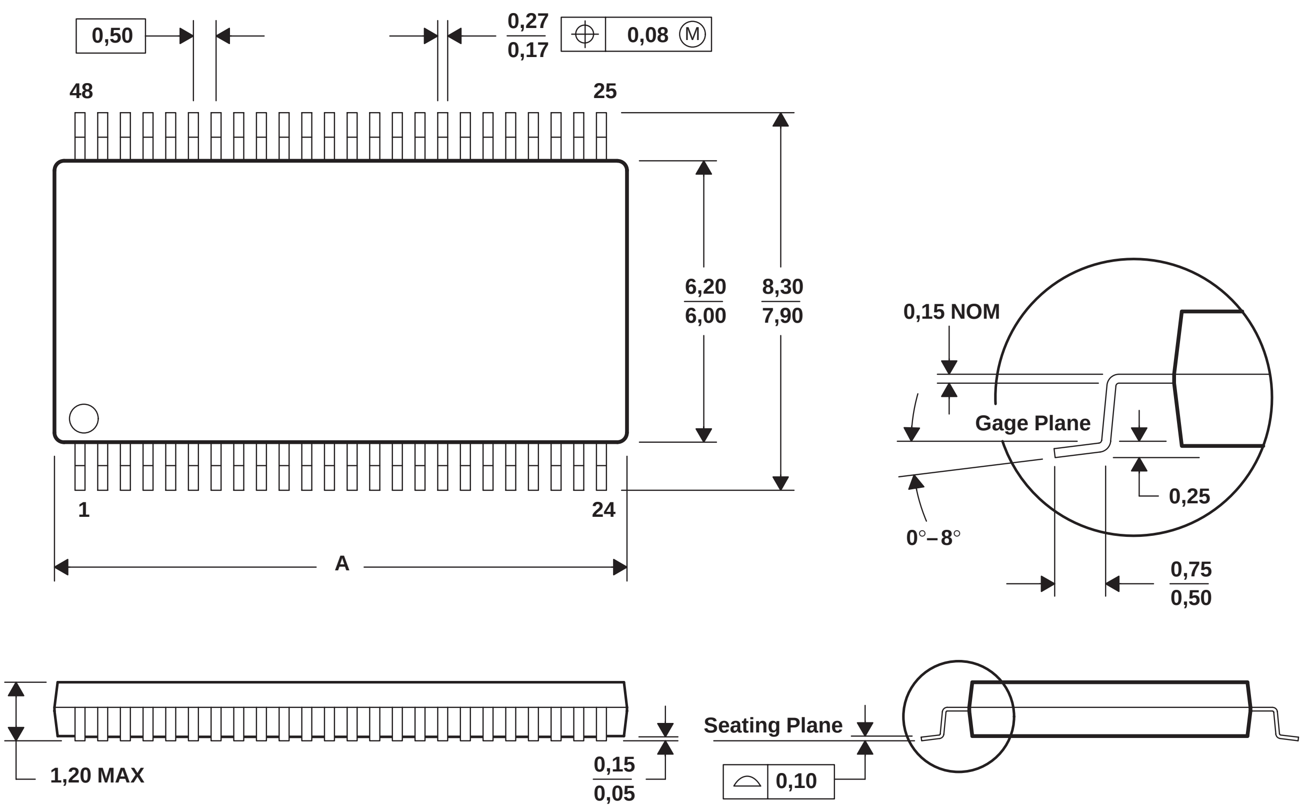



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CDCV850DGGR | TSSOP | DGG | 48 | 2000 | 367.0 | 367.0 | 45.0 |

**DGG (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**48 PINS SHOWN**




| DIM \ PINS ** | 48 | 56 | 64 |
|---|---|---|---|
| A MAX | 12,60 | 14,10 | 17,10 |
| A MIN | 12,40 | 13,90 | 16,90 |

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NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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