

Quad, Serial Input, 12-Bit, Voltage Output DIGITAL-TO-ANALOG CONVERTER

FEATURES

- **LOW POWER:** 3mW
- **SETTLING TIME:** 10 μ s to 0.012%
- **12-BIT LINEARITY AND MONOTONICITY:** -40°C to +85°C
- **DOUBLE-BUFFERED DATA INPUTS**
- **SO-16 or SSOP-20 PACKAGES**
- **SINGLE-SUPPLY +3V OPERATION**

APPLICATIONS

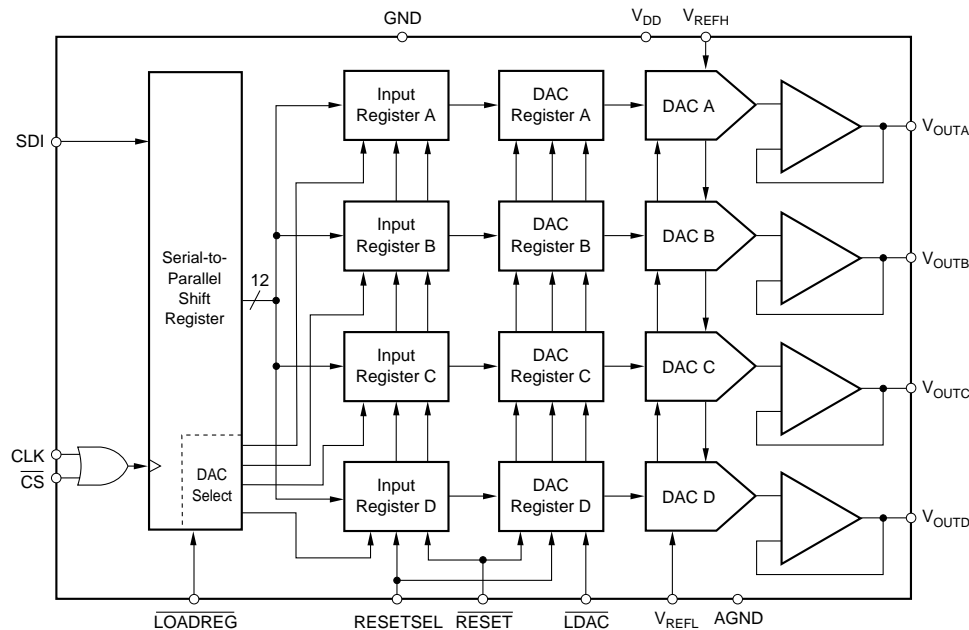
- **PROCESS CONTROL**
- **ATE PIN ELECTRONICS**
- **CLOSED-LOOP SERVO-CONTROL**
- **MOTOR CONTROL**
- **DATA ACQUISITION SYSTEMS**
- **DAC-PER-PIN PROGRAMMERS**

DESCRIPTION

The DAC7617 is a quad, serial input, 12-bit, voltage output Digital-to-Analog Converter (DAC) with guaranteed 12-bit monotonic performance over the -40°C to +85°C temperature range. An asynchronous reset clears all registers to either mid-scale (800_H) or zero-scale (000_H), selectable via the RESETSEL pin. The individual DAC inputs are double buffered to allow

for simultaneous update of all DAC outputs. The device is powered from a single +3V supply.

Low power and small size makes the DAC7617 ideal for automatic test equipment, DAC-per-pin programmers, data acquisition systems, and closed-loop servo-control. The device is available in SO-16 and SSOP-20 packages and is guaranteed over the -40°C to +85°C temperature range.



SPECIFICATIONS

At $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{DD} = +3\text{V}$, $V_{REFH} = +1.25\text{V}$, and $V_{REFL} = 0\text{V}$, unless otherwise noted.

PARAMETER	CONDITIONS	DAC7617E, U			DAC7617EB, UB			UNITS	
		MIN	TYP	MAX	MIN	TYP	MAX		
ACCURACY									
Linearity Error ⁽¹⁾	Code = 00A _H	12		±2	*		±1	LSB ⁽²⁾	
Linearity Matching ⁽³⁾				±2			±1	LSB	
Differential Linearity Error				±1			±1	LSB	
Monotonicity								Bits	
Zero-Scale Error				±2.4			*	mV	
Zero-Scale Drift			5	10		*	*	ppm/°C	
Zero-Scale Matching ⁽³⁾			±1	±2		*	±1.2	mV	
Full-Scale Error	Code = FFF _H			±2.4			*	mV	
Full-Scale Matching ⁽³⁾			±1	±2		*	±1.2	mV	
Power Supply Rejection			30			*		ppm/V	
ANALOG OUTPUT									
Voltage Output ⁽⁴⁾	No Oscillation	V_{REFL} -625		V_{REFH} +625	*		*	V	
Output Current					*		*	μA	
Load Capacitance			100			*			pF
Short-Circuit Current			+8, -2			*			mA
Short-Circuit Duration			Indefinite			*			
REFERENCE INPUT									
V_{REFH} Input Range		0		+1.25	*		*	V	
V_{REFL} Input Range		0			*		*	V	
DYNAMIC PERFORMANCE									
Settling Time	To ±0.012%		5	10		*	*	μs	
Channel-to-Channel Crosstalk	Full-Scale Step On Any Other DAC		0.1			*		LSB	
Output Noise Voltage	Bandwidth: 0Hz to 1MHz		65			*		nV/√Hz	
DIGITAL INPUT/OUTPUT									
Logic Family			CMOS			*			
Logic Levels	$ I_{IH} \leq 10\mu\text{A}$ $ I_{IL} \leq 10\mu\text{A}$	$V_{DD} \cdot 0.7$ -0.3		V_{DD} $V_{DD} \cdot 0.3$	*		*	V	
V_{IH}					*		*	V	
V_{IL}					*		*	V	
Data Format			Straight Binary			*			
POWER SUPPLY REQUIREMENTS									
V_{DD}		3.0	3.3	3.6	*	*	*	V	
I_{DD}			0.8	1		*	*	mA	
Power Dissipation			2.4	3		*	*	mW	
TEMPERATURE RANGE									
Specified Performance		-40		+85	*		*	°C	

* Specification same as DAC7617E, U.

NOTES: (1) Specification applies at code 00A_H and above. (2) LSB means Least Significant Bit, with V_{REFH} equal to +1.25V and V_{REFL} equal to 0V, one LSB is 0.305mV. (3) All DAC outputs will match within the specified error band. (4) Ideal output voltage does not take into account zero or full-scale error.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

V _{DD} to GND	-0.3V to +5.5V
V _{REFL} to GND	-0.3V to (V _{DD} + 0.3V)
V _{DD} to V _{REFH}	-0.3V to V _{DD}
V _{REFH} to V _{REFL}	-0.3V to V _{DD}
Digital Input Voltage to GND	-0.3V to V _{DD} + 0.3V
Maximum Junction Temperature	+150°C
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

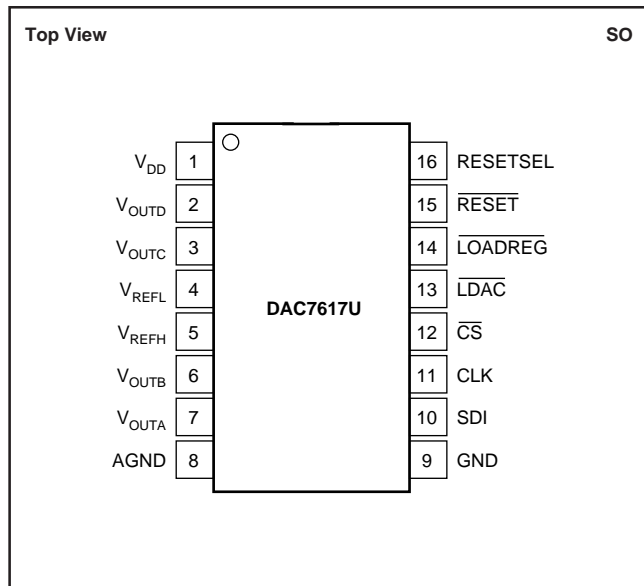
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

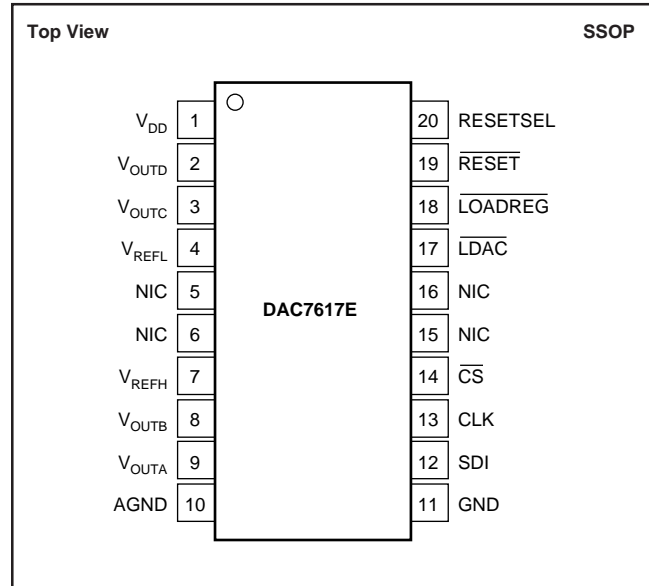
PRODUCT	MAXIMUM LINEARITY ERROR (LSB)	MAXIMUM DIFFERENTIAL LINEARITY (LSB)	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFICATION TEMPERATURE RANGE	ORDERING NUMBER ⁽¹⁾	TRANSPORT MEDIA
DAC7617U "	±2 "	±1 "	SO-16 "	211 "	-40°C to +85°C "	DAC7617U DAC7617U/1K	Rails Tape and Reel
DAC7617UB "	±1 "	±1 "	SO-16 "	211 "	-40°C to +85°C "	DAC7617UB DAC7617UB/1K	Rails Tape and Reel
DAC7617E "	±2 "	±1 "	SSOP-20 "	334 "	-40°C to +85°C "	DAC7617E DAC7617E/1K	Rails Tape and Reel
DAC7617EB "	±1 "	±1 "	SSOP-20 "	334 "	-40°C to +85°C "	DAC7617EB DAC7617EB/1K	Rails Tape and Reel

NOTE: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /1K indicates 1000 devices per reel). Ordering 1000 pieces of "DAC7617EB/1K" will get a single 1000-piece Tape and Reel.

PIN CONFIGURATION—U Package



PIN CONFIGURATION—E Package



PIN DESCRIPTIONS—U Package

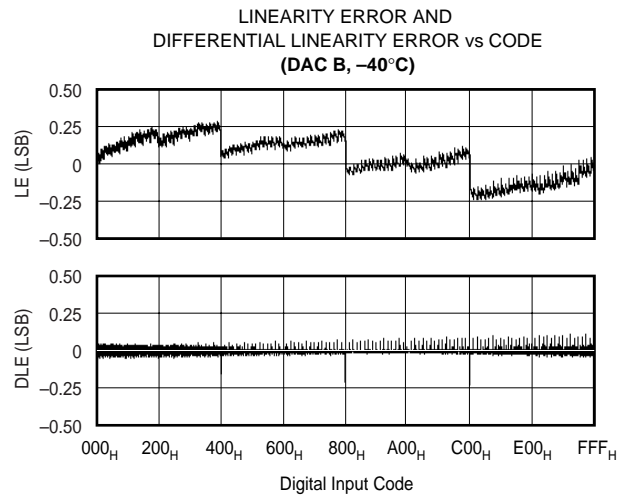
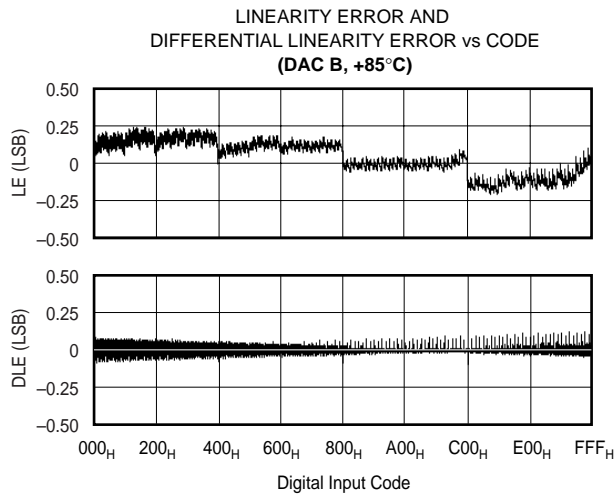
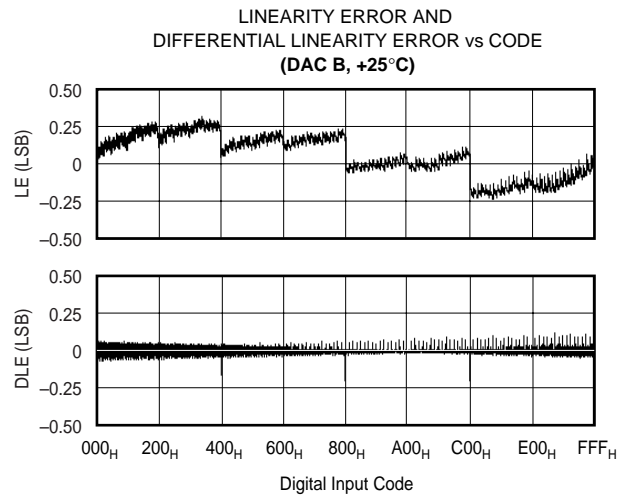
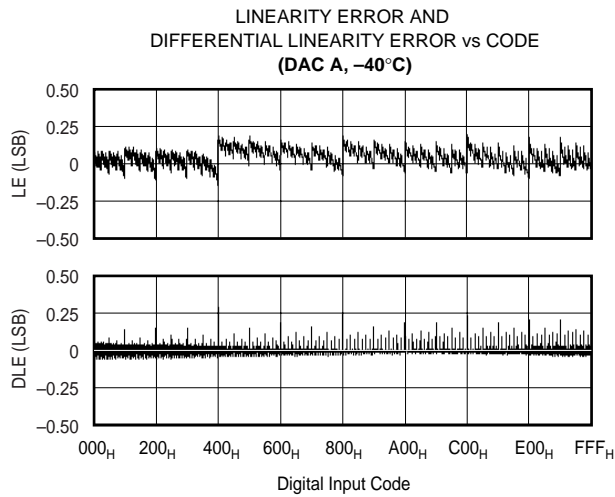
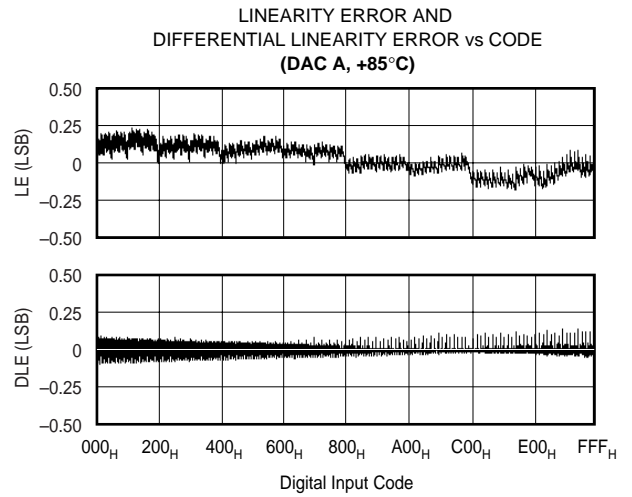
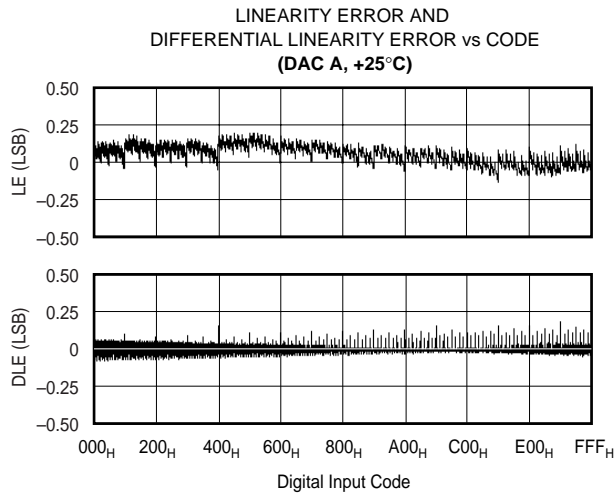
PIN	LABEL	DESCRIPTION
1	V _{DD}	Positive Analog Supply Voltage, +3V nominal.
2	V _{OUTD}	DAC D Voltage Output
3	V _{OUTC}	DAC C Voltage Output
4	V _{REFL}	Reference Input Voltage Low. Sets minimum output voltage for all DACs.
5	V _{REFH}	Reference Input Voltage High. Sets maximum output voltage for all DACs.
6	V _{OUTB}	DAC B Voltage Output
7	V _{OUTA}	DAC A Voltage Output
8	AGND	Analog Ground
9	GND	Ground
10	SDI	Serial Data Input
11	CLK	Serial Data Clock
12	$\overline{\text{CS}}$	Chip Select Input
13	$\overline{\text{LDAC}}$	All DAC registers become transparent when $\overline{\text{LDAC}}$ is LOW. They are in the latched state when $\overline{\text{LDAC}}$ is HIGH.
14	$\overline{\text{LOADREG}}$	The selected input register becomes transparent when $\overline{\text{LOADREG}}$ is LOW. It is in the latched state when $\overline{\text{LOADREG}}$ is HIGH.
15	$\overline{\text{RESET}}$	Asynchronous Reset Input. Sets DAC and input registers to either zero-scale (000 _H) or mid-scale (800 _H) when LOW. RESETSEL determines which code is active.
16	RESETSEL	When LOW, a LOW on $\overline{\text{RESET}}$ will cause the DAC and input registers to be set to code 000 _H . When RESETSEL is HIGH, a LOW on $\overline{\text{RESET}}$ will set the registers to code 800 _H .

PIN DESCRIPTIONS—E Package

PIN	LABEL	DESCRIPTION
1	V _{DD}	Positive Analog Supply Voltage, +3V nominal.
2	V _{OUTD}	DAC D Voltage Output
3	V _{OUTC}	DAC C Voltage Output
4	V _{REFL}	Reference Input Voltage Low. Sets minimum output voltage for all DACs.
5	NIC	Not Internally Connected.
6	NIC	Not Internally Connected.
7	V _{REFH}	Reference Input Voltage High. Sets maximum output voltage for all DACs.
8	V _{OUTB}	DAC B Voltage Output
9	V _{OUTA}	DAC A Voltage Output
10	AGND	Analog Ground
11	GND	Ground
12	SDI	Serial Data Input
13	CLK	Serial Data Clock
14	$\overline{\text{CS}}$	Chip Select Input
15	NIC	Not Internally Connected.
16	NIC	Not Internally Connected.
17	$\overline{\text{LDAC}}$	All DAC registers becomes transparent when $\overline{\text{LDAC}}$ is LOW. They are in the latched state when $\overline{\text{LDAC}}$ is HIGH.
18	$\overline{\text{LOADREG}}$	The selected input register becomes transparent when $\overline{\text{LOADREG}}$ is LOW. It is in the latched state when $\overline{\text{LOADREG}}$ is HIGH.
19	$\overline{\text{RESET}}$	Asynchronous Reset Input. Sets all DAC registers to either zero-scale (000 _H) or mid-scale (800 _H) when LOW. RESETSEL determines which code is active.
20	RESETSEL	When LOW, a LOW on $\overline{\text{RESET}}$ will cause all DAC registers to be set to code 000 _H . When RESETSEL is HIGH, a LOW on $\overline{\text{RESET}}$ will set the registers to code 800 _H .

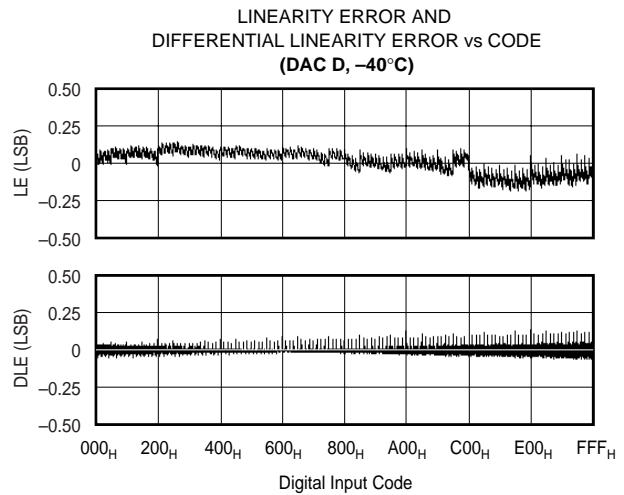
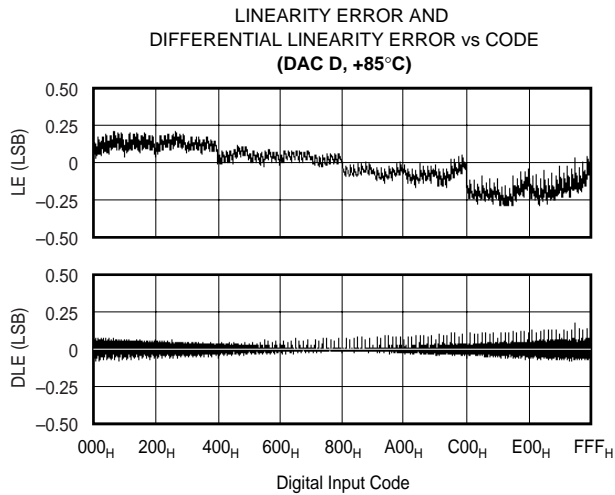
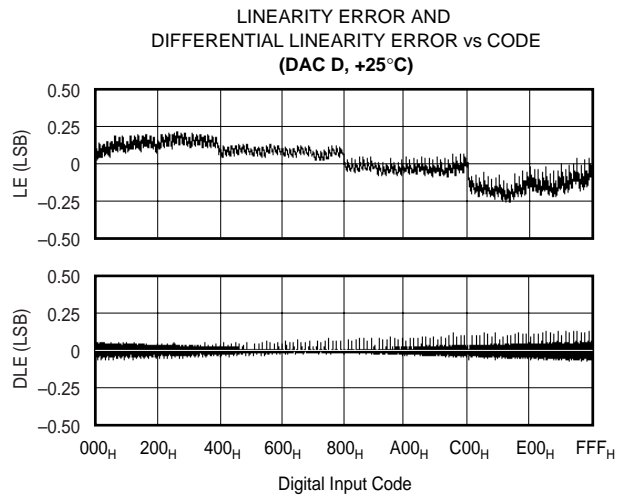
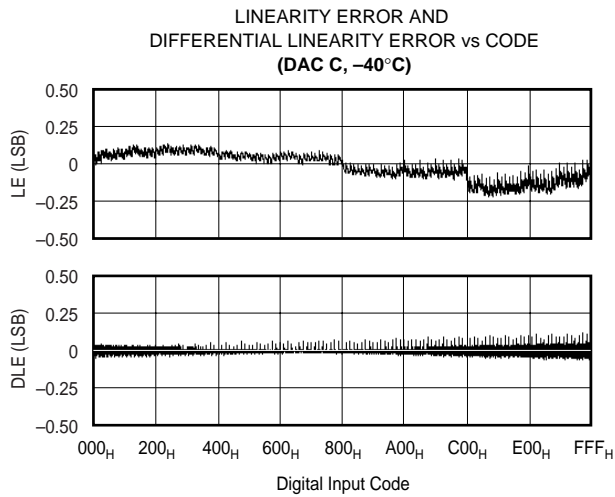
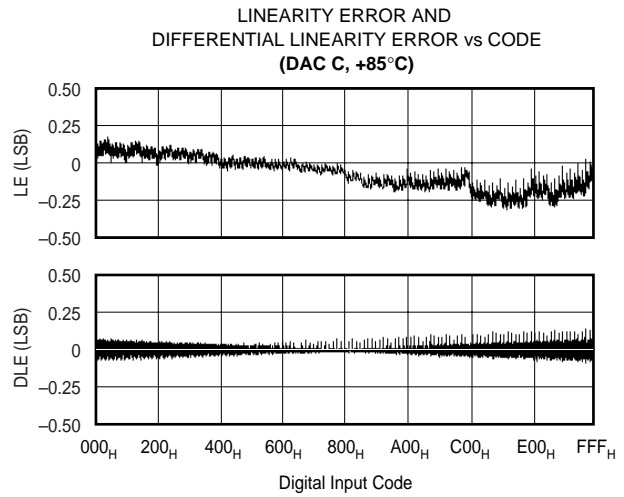
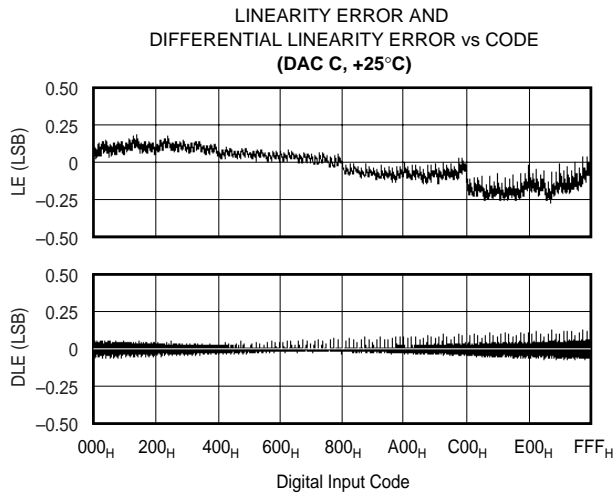
TYPICAL PERFORMANCE CURVES

At $T_A = +25^\circ\text{C}$, $V_{DD} = +3\text{V}$, $V_{REFH} = +1.25\text{V}$, and $V_{REFL} = 0\text{V}$, representative unit, unless otherwise specified.



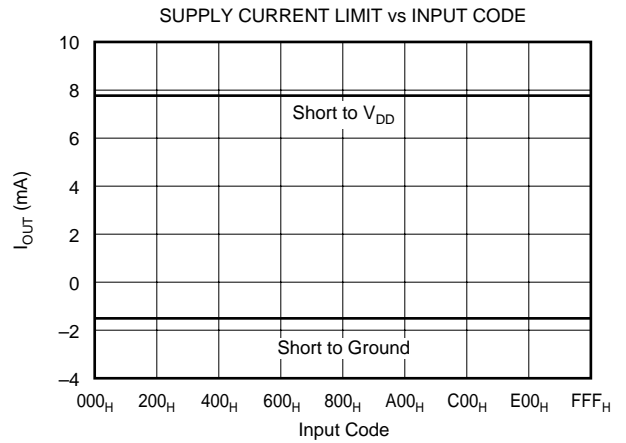
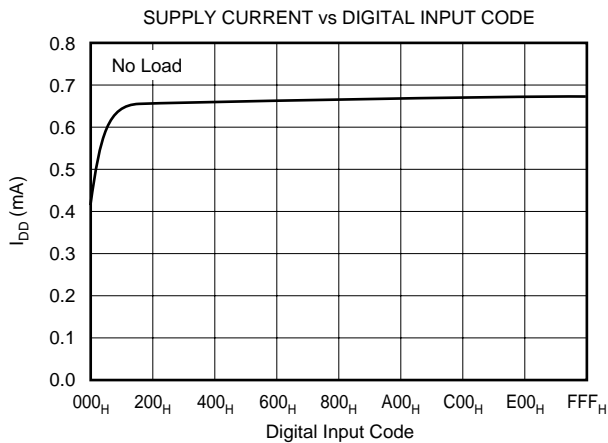
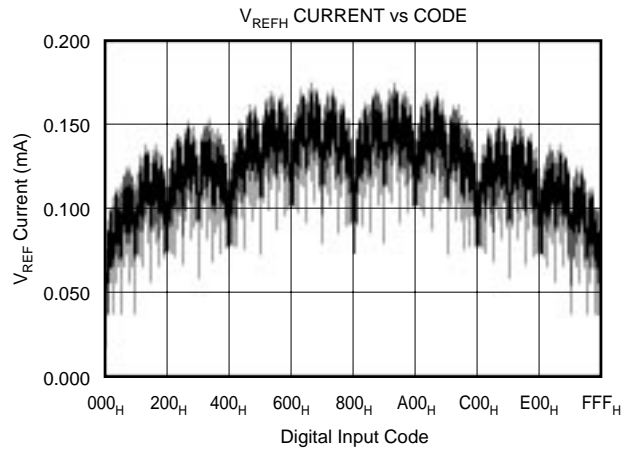
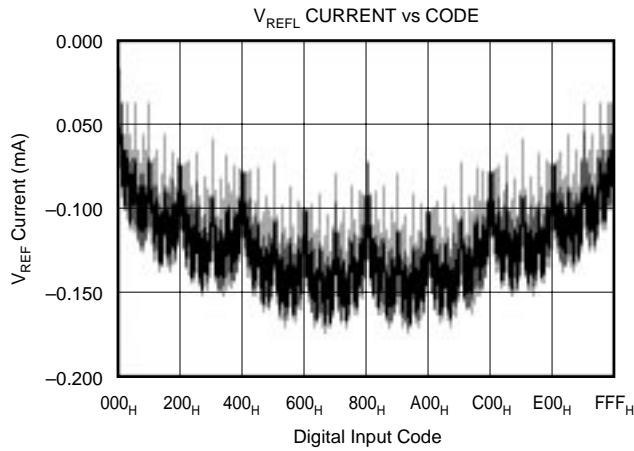
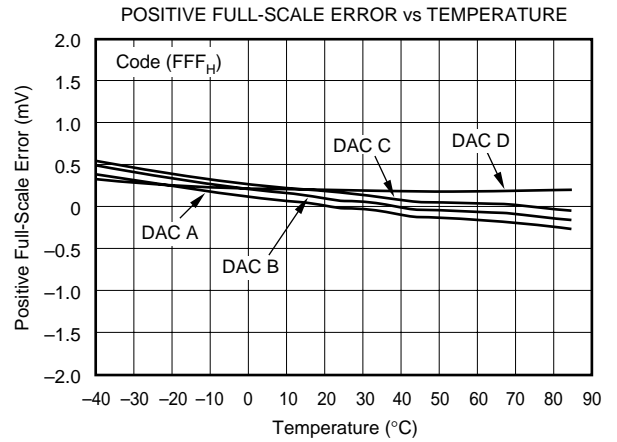
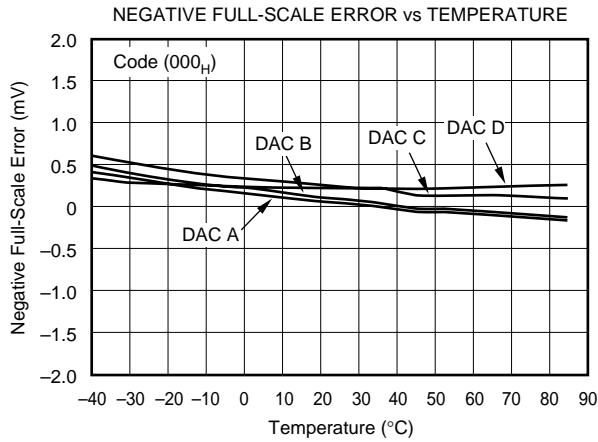
TYPICAL PERFORMANCE CURVES

At $T_A = +25^\circ\text{C}$, $V_{DD} = +3\text{V}$, $V_{REFH} = +1.25\text{V}$, and $V_{REFL} = 0\text{V}$, representative unit, unless otherwise specified.



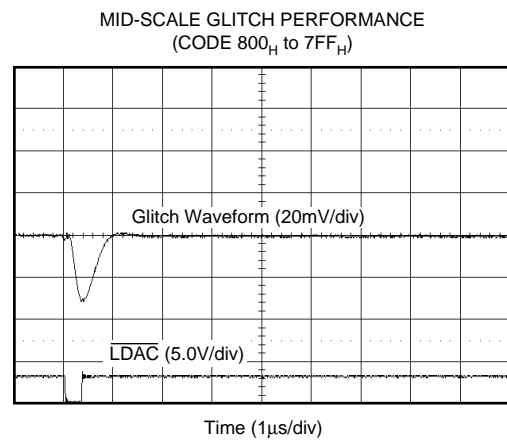
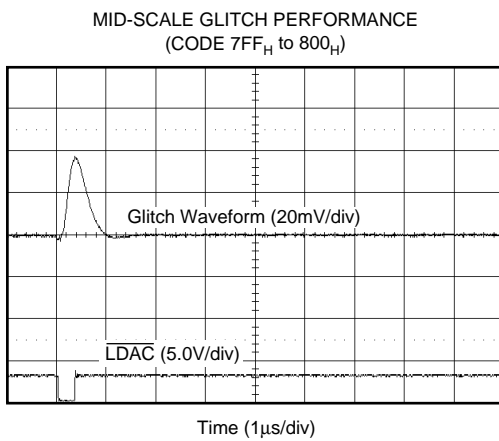
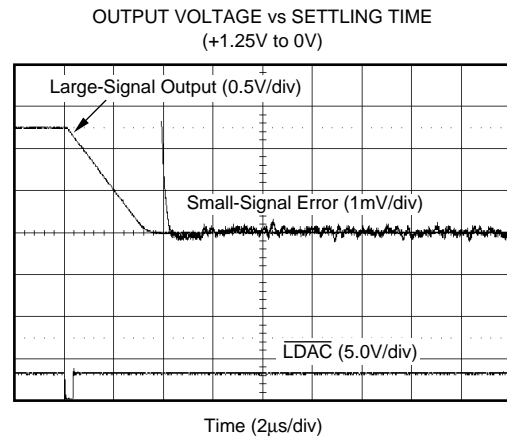
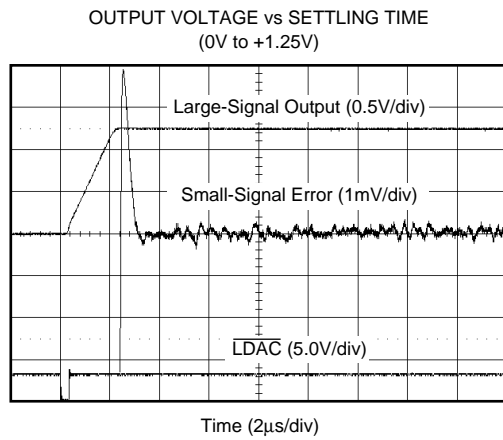
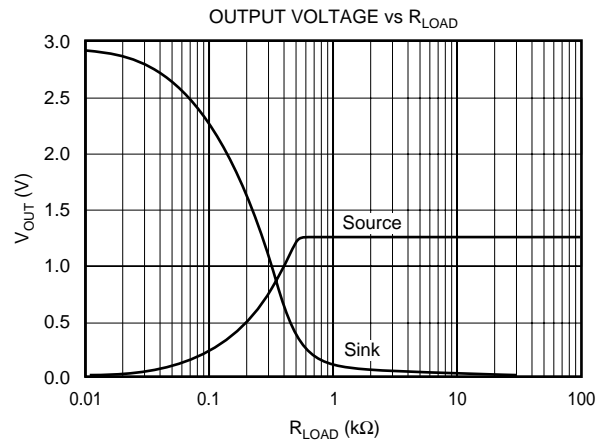
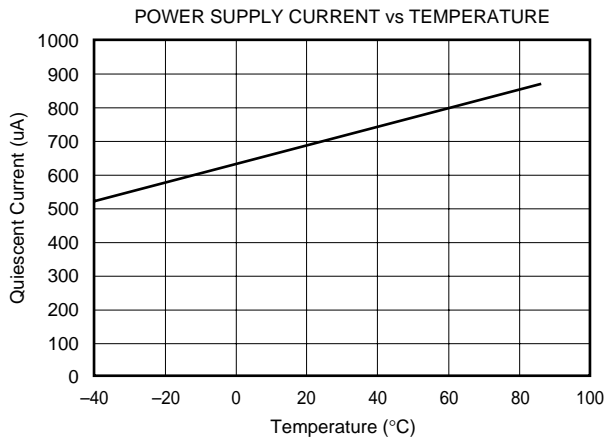
TYPICAL PERFORMANCE CURVES

At $T_A = +25^\circ\text{C}$, $V_{DD} = +3\text{V}$, $V_{REFH} = +1.25\text{V}$, and $V_{REFL} = 0\text{V}$, representative unit, unless otherwise specified.



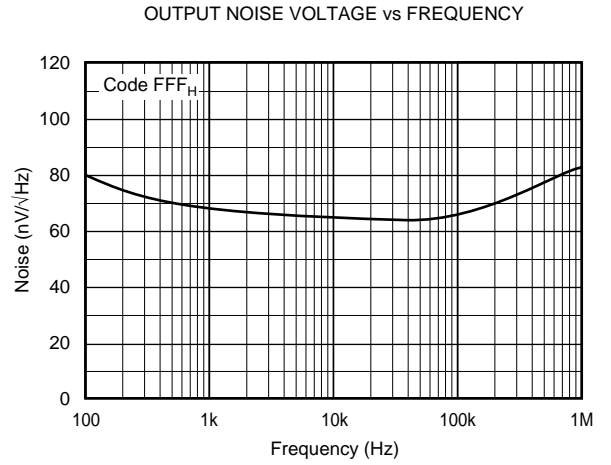
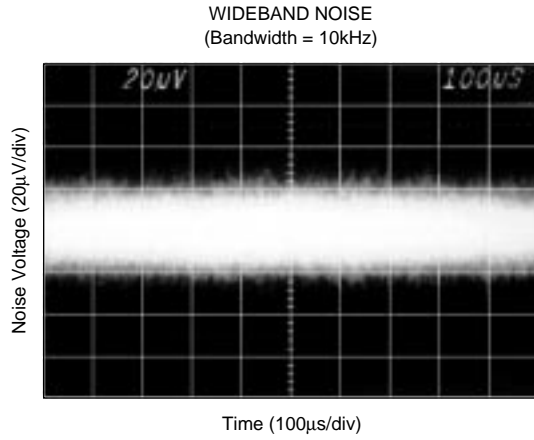
TYPICAL PERFORMANCE CURVES

At $T_A = +25^\circ\text{C}$, $V_{DD} = +3\text{V}$, $V_{REFH} = +1.25\text{V}$, and $V_{REFL} = 0\text{V}$, representative unit, unless otherwise specified.



TYPICAL PERFORMANCE CURVES

At $T_A = +25^\circ\text{C}$, $V_{DD} = +3\text{V}$, $V_{REFH} = +1.25\text{V}$, and $V_{REFL} = 0\text{V}$, representative unit, unless otherwise specified.



THEORY OF OPERATION

The DAC7617 is a quad, serial input, 12-bit, voltage output DAC. The architecture is a classic R-2R ladder configuration followed by an operational amplifier that serves as a buffer. Each DAC has its own R-2R ladder network and output op amp, but all share the reference voltage inputs. The minimum voltage output (“zero-scale”) and maximum voltage output (“full-scale”) are set by external voltage references (V_{REFL} and V_{REFH} , respectively). The digital input is a 16-bit serial word that contains the 12-bit DAC code and a 2-bit address code that selects one of the four DACs (the two remaining bits are unused). The converter can be powered from a single +3V supply. Each device offers a reset function which immediately sets all DAC output voltages and internal registers to either zero-scale (code 000_H) or mid-scale (code 800_H). The reset code is selected by the state of the RESETSEL pin (LOW = 000_H, HIGH = 800_H). See Figure 1 for the basic operation of the DAC7617.

ANALOG OUTPUTS

The output of the DAC7617 can swing to ground. Note that the settling time of the output op amp will be longer with voltages very near ground. Additionally, care must be taken when measuring the zero-scale error. If the output amplifier has a negative offset, the output voltage may not change for the first few digital input codes (000_H, 001_H, 002_H, etc.) since the output voltage cannot swing below ground.

The behavior of the output amplifier can be critical in some applications. Under short-circuit conditions (DAC output shorted to V_{DD}), the output amplifier can sink a great deal more current than it can source. See the Specifications Table for more details concerning short-circuit current.

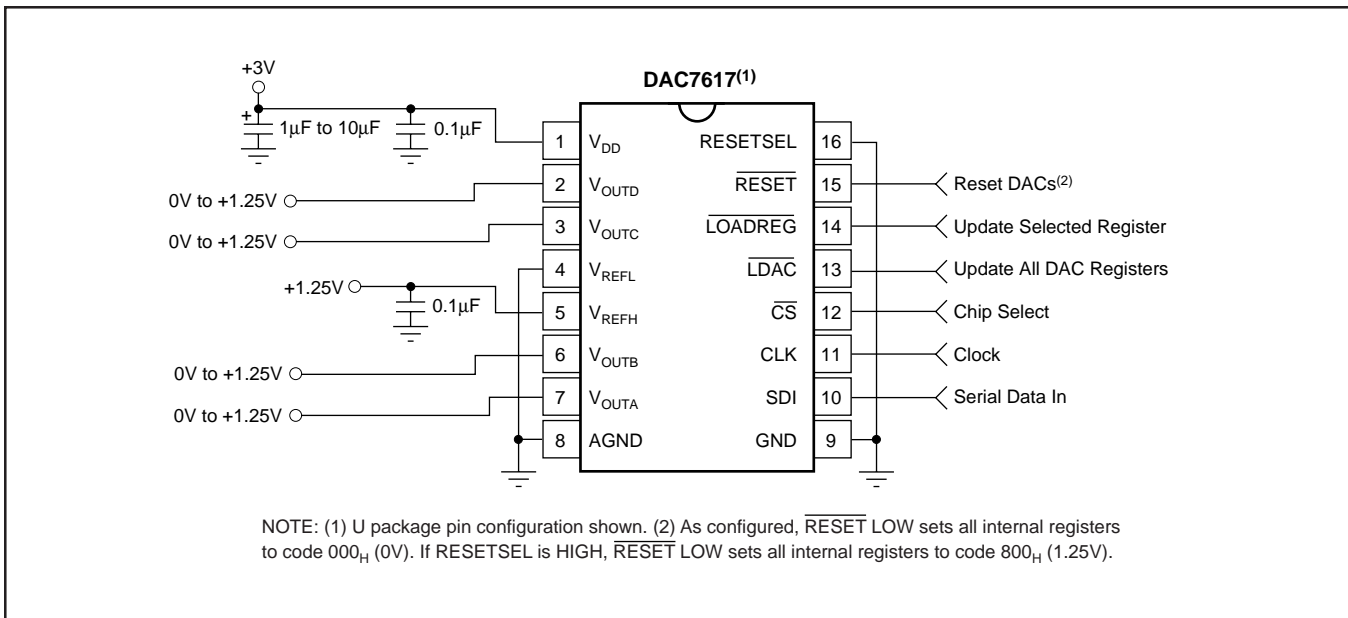


FIGURE 1. Basic Single-Supply Operation of the DAC7617.

REFERENCE INPUTS

The minimum output of each DAC is equal to V_{REFL} plus a small offset voltage (essentially, the offset of the output op amp). The maximum output is equal to $V_{REFH} - 1LSB$ plus a similar offset voltage.

The current into the reference inputs depends on the DAC output voltages and can vary from a few microamps to approximately 0.4 milliamp. Bypassing the reference voltage or voltages with a $0.1\mu F$ capacitor placed as close as possible to the DAC7617 package is strongly recommended.

DIGITAL INTERFACE

Figure 2 and Table I provide the basic timing for the DAC7617. The interface consists of a serial clock (CLK), serial data (SDI), a load register signal ($\overline{LOADREG}$), and a “load all DAC registers” signal (\overline{LDAC}). In addition, a chip select (\overline{CS}) input is available to enable serial communication when there are multiple serial devices. An asynchronous reset input (\overline{RESET}) is provided to simplify start-up conditions, periodic resets, or emergency resets to a known state.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{DS}	Data Valid to CLK Rising	25			ns
t_{DH}	Data Held Valid after CLK Rises	20			ns
t_{CH}	CLK HIGH	30			ns
t_{CL}	CLK LOW	50			ns
t_{CSS}	\overline{CS} LOW to CLK Rising	55			ns
t_{CSH}	CLK HIGH to \overline{CS} Rising	15			ns
t_{LD1}	$\overline{LOADREG}$ HIGH to CLK Rising	40			ns
t_{LD2}	CLK Rising to $\overline{LOADREG}$ LOW	15			ns
t_{LDRW}	$\overline{LOADREG}$ LOW Time	45			ns
t_{LDDW}	\overline{LDAC} LOW Time	45			ns
t_{RSSH}	RESETSEL Valid to \overline{RESET} LOW	25			ns
t_{RSTW}	\overline{RESET} LOW Time	70			ns
t_S	Settling Time	10			μs

TABLE I. Timing Specifications ($T_A = -40^\circ C$ to $+85^\circ C$).

The DAC code and address are provided via a 16-bit serial interface, as shown in Figure 2. The first two bits select the input register that will be updated when $\overline{LOADREG}$ goes LOW (see Table II). The next two bits are not used. The last 12 bits are the DAC code which is provided, most significant bit first.

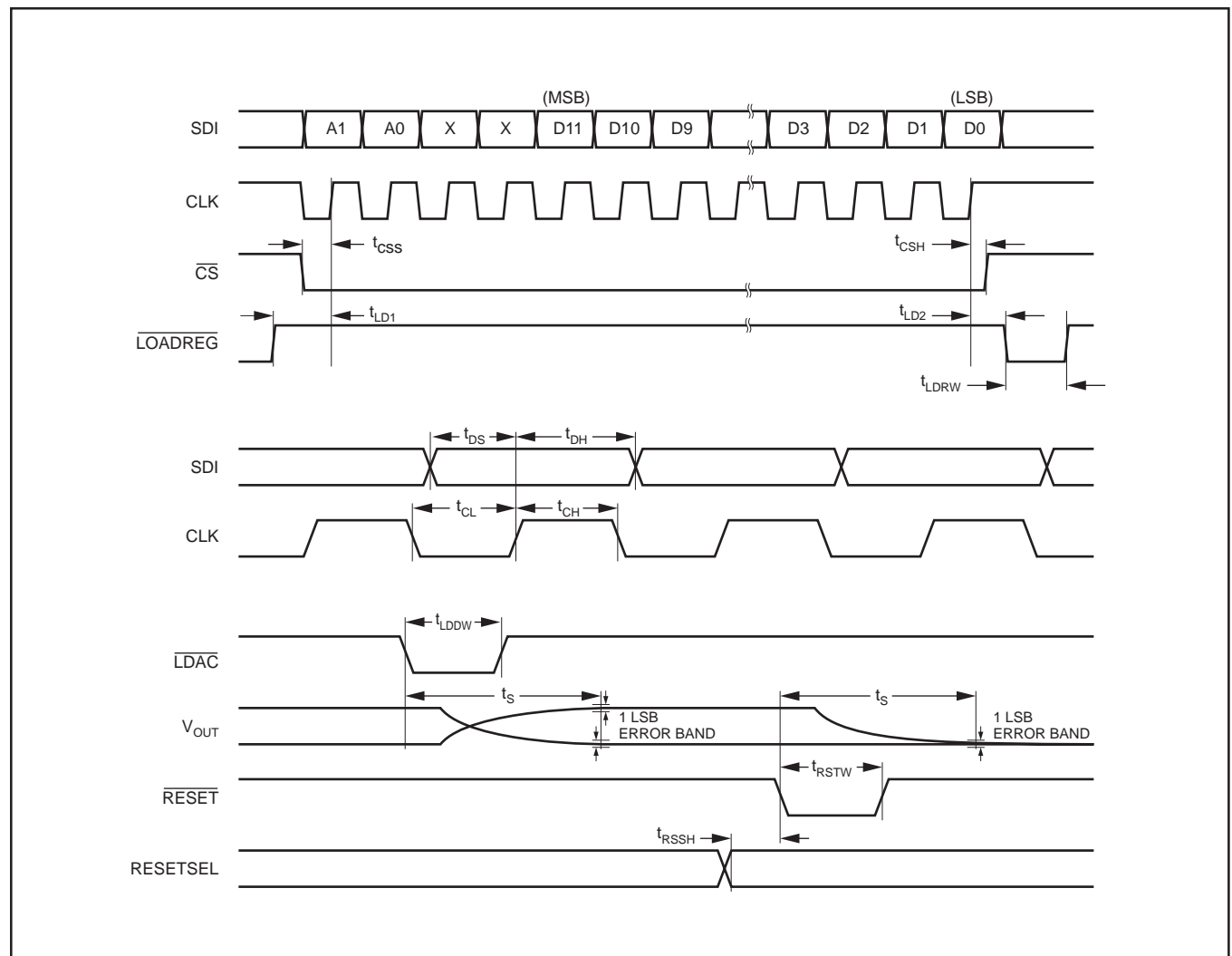


FIGURE 2. DAC7617 Timing.

A1	A0	$\overline{\text{LOADREG}}$	$\overline{\text{LDAC}}$	$\overline{\text{RESET}}$	SELECTED INPUT REGISTER	STATE OF SELECTED INPUT REGISTER	STATE OF ALL DAC REGISTERS
L ⁽¹⁾	L	L	H ⁽²⁾	H	A	Transparent	Latched
L	H	L	H	H	B	Transparent	Latched
H	L	L	H	H	C	Transparent	Latched
H	H	L	H	H	D	Transparent	Latched
X ⁽³⁾	X	H	L	H	NONE	(All Latched)	Transparent
X	X	H	H	H	NONE	(All Latched)	Latched
X	X	X	X	L	ALL	Reset ⁽⁴⁾	Reset ⁽⁴⁾

NOTES: (1) L = Logic LOW. (2) H = Logic HIGH. (3) X = Don't Care. (4) Resets to either 000H or 800_H, per the RESETSEL state (LOW = 000_H, HIGH = 800_H). When $\overline{\text{RESET}}$ rises, all registers that are in their latched state retain the reset value.

TABLE II. Control Logic Truth Table.

$\overline{\text{CS}}^{(1)}$	CLK ⁽¹⁾	$\overline{\text{LOADREG}}$	$\overline{\text{RESET}}$	SERIAL SHIFT REGISTER
H ⁽²⁾	X ⁽³⁾	H	H	No Change
L ⁽⁴⁾	L	H	H	No Change
L	↑ ⁽⁵⁾	H	H	Advanced One Bit
↑	L	H	H	Advanced One Bit
H ⁽⁶⁾	X	L ⁽⁷⁾	H	No Change
H ⁽⁶⁾	X	H	L ⁽⁸⁾	No Change

NOTES: (1) $\overline{\text{CS}}$ and CLK are interchangeable. (2) H = Logic HIGH. (3) X = Don't Care. (4) L = Logic LOW (5) = Positive Logic Transition. (6) A HIGH value is suggested in order to avoid a "false clock" from advancing the shift register and changing the shift register. (7) If data is clocked into the serial register while $\overline{\text{LOADREG}}$ is LOW, the selected input register will change as the shift register bits "flow" through A1 and A0. This will corrupt the data in each input register that has been erroneously selected. (8) $\overline{\text{RESET}}$ LOW causes no change in the contents of the serial shift register.

TABLE III. Serial Shift Register Truth Table.

Note that $\overline{\text{CS}}$ and CLK are combined with an OR gate and the output controls the serial-to-parallel shift register internal to the DAC7617 (see the block diagram on the front of this data sheet). These two inputs are completely interchangeable. In addition, care must be taken with the state of CLK when $\overline{\text{CS}}$ rises at the end of a serial transfer. If CLK is LOW when $\overline{\text{CS}}$ rises, the OR gate will provide a rising edge to the shift register, shifting the internal data one additional bit. The result will be incorrect data and possible selection of the wrong input register.

If both $\overline{\text{CS}}$ and CLK are used, then $\overline{\text{CS}}$ should rise only when CLK is HIGH. If not, then either $\overline{\text{CS}}$ or CLK can be used to operate the shift register. See Table III for more information.

The digital data into the DAC7617 is double-buffered. This allows new data to be entered for each DAC without disturbing the analog outputs. When the new settings have been entered into the device, all of the DAC outputs can be updated simultaneously. The transfer from the input registers to the DAC registers is accomplished with a HIGH to LOW transition on the $\overline{\text{LDAC}}$ input. It is possible to keep this pin LOW and update each DAC via $\overline{\text{LOADREG}}$ because the DAC registers become transparent when $\overline{\text{LDAC}}$ is LOW. However, as each new data word is entered into the device, the corresponding output will update immediately when $\overline{\text{LOADREG}}$ is taken LOW.

Digital Input Coding

The DAC7617 input data is in Straight Binary format. The output voltage is given by the following equation:

$$V_{\text{OUT}} = V_{\text{REFL}} + \frac{(V_{\text{REFH}} - V_{\text{REFL}}) \cdot N}{4096}$$

where N is the digital input code (in decimal). This equation does not include the effects of offset (zero-scale) or gain (full-scale) errors.

LAYOUT

A precision analog component requires careful layout, adequate bypassing, and clean, well-regulated power supplies. As the DAC7617 offers single-supply operation, it will often be used in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it will be to keep digital noise from appearing at the converter output.

Due to the DAC7617's single ground pin, all return currents, including digital and analog return currents, must flow through the GND pin. Ideally, GND would be connected directly to an analog ground plane. This plane would be separate from the ground connection for the digital components until they were connected at the power entry point of the system (see Figure 3).

The power applied to V_{DD} should be well regulated and low noise. Switching power supplies and DC/DC converters will often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes as their internal logic switches states. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output.

As with the GND connection, V_{DD} should be connected to a +3V power supply plane or trace that is separate from the connection for digital logic until they are connected at the power entry point. In addition, the 1 μ F to 10 μ F and 0.1 μ F capacitors shown in Figure 3 are strongly recommended. In some situations, additional bypassing may be required, such as a 100 μ F electrolytic capacitor or even a π filter made up of inductors and capacitors—all designed to essentially low-pass filter the +3V supply, removing the high-frequency noise (see Figure 3).

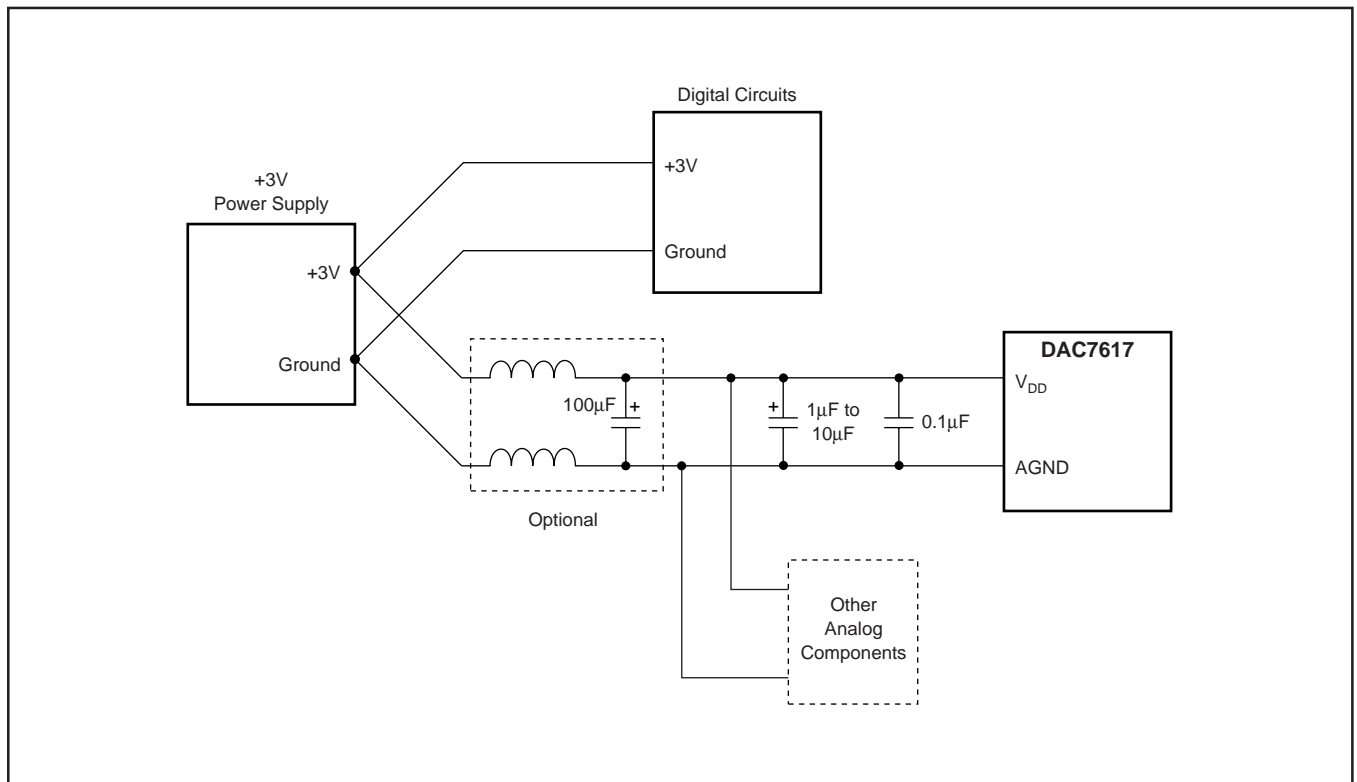


FIGURE 3. Suggested Power and Ground Connections for a DAC7617 Sharing a +3V Supply with a Digital System.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
DAC7617E	ACTIVE	SSOP	DB	20	68	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7617E/1K	ACTIVE	SSOP	DB	20	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7617E/1KG4	ACTIVE	SSOP	DB	20	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7617EB	ACTIVE	SSOP	DB	20	68	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7617EB/1K	ACTIVE	SSOP	DB	20	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7617EB/1KG4	ACTIVE	SSOP	DB	20	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7617EBG4	ACTIVE	SSOP	DB	20	68	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7617EG4	ACTIVE	SSOP	DB	20	68	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7617U	ACTIVE	SOIC	DW	16	48	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7617U/1K	ACTIVE	SOIC	DW	16	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7617U/1KG4	ACTIVE	SOIC	DW	16	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7617UB	ACTIVE	SOIC	DW	16	48	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7617UB/1K	ACTIVE	SOIC	DW	16	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7617UB/1KG4	ACTIVE	SOIC	DW	16	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7617UBG4	ACTIVE	SOIC	DW	16	48	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7617UG4	ACTIVE	SOIC	DW	16	48	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

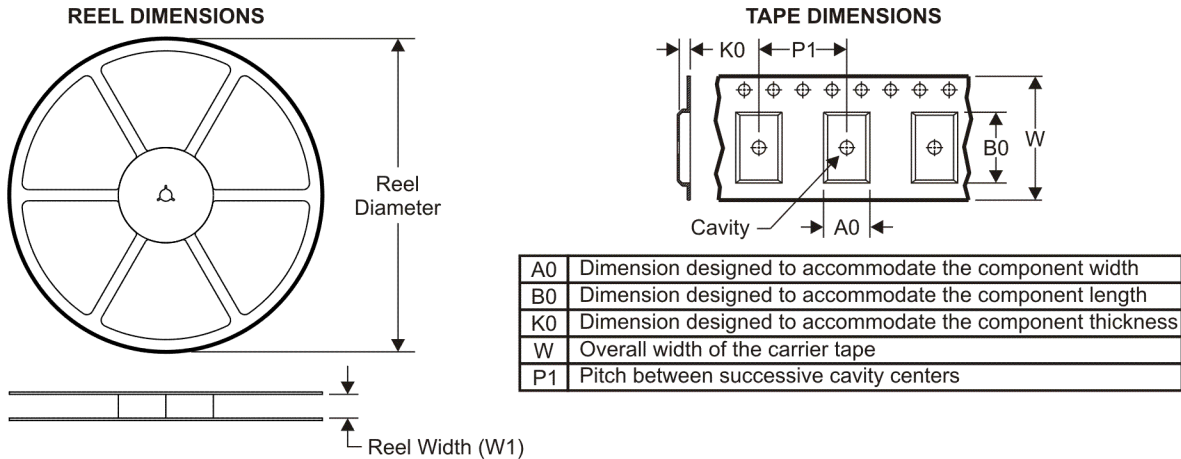
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

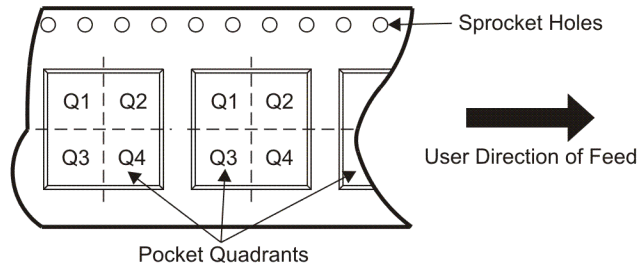
Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC7617E/1K	SSOP	DB	20	1000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
DAC7617EB/1K	SSOP	DB	20	1000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
DAC7617U/1K	SOIC	DW	16	1000	330.0	16.4	10.85	10.8	2.7	12.0	16.0	Q1
DAC7617UB/1K	SOIC	DW	16	1000	330.0	16.4	10.85	10.8	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC7617E/1K	SSOP	DB	20	1000	346.0	346.0	33.0
DAC7617EB/1K	SSOP	DB	20	1000	346.0	346.0	33.0
DAC7617U/1K	SOIC	DW	16	1000	346.0	346.0	33.0
DAC7617UB/1K	SOIC	DW	16	1000	346.0	346.0	33.0

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
RF/IF and ZigBee® Solutions	www.ti.com/lprf

Applications

Audio	www.ti.com/audio
Automotive	www.ti.com/automotive
Broadband	www.ti.com/broadband
Digital Control	www.ti.com/digitalcontrol
Medical	www.ti.com/medical
Military	www.ti.com/military
Optical Networking	www.ti.com/opticalnetwork
Security	www.ti.com/security
Telephony	www.ti.com/telephony
Video & Imaging	www.ti.com/video
Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2008, Texas Instruments Incorporated