

# Precision, Low Power INSTRUMENTATION AMPLIFIERS

## FEATURES

- **LOW OFFSET VOLTAGE:** 50µV max
- **LOW DRIFT:** 0.5µV/°C max
- **LOW INPUT BIAS CURRENT:** 5nA max
- **HIGH CMR:** 120dB min
- **INPUTS PROTECTED TO ±40V**
- **WIDE SUPPLY RANGE:** ±2.25V to ±18V
- **LOW QUIESCENT CURRENT:** 700µA
- **8-PIN PLASTIC DIP, SO-8**

## APPLICATIONS

- BRIDGE AMPLIFIER
- THERMOCOUPLE AMPLIFIER
- RTD SENSOR AMPLIFIER
- MEDICAL INSTRUMENTATION
- DATA ACQUISITION

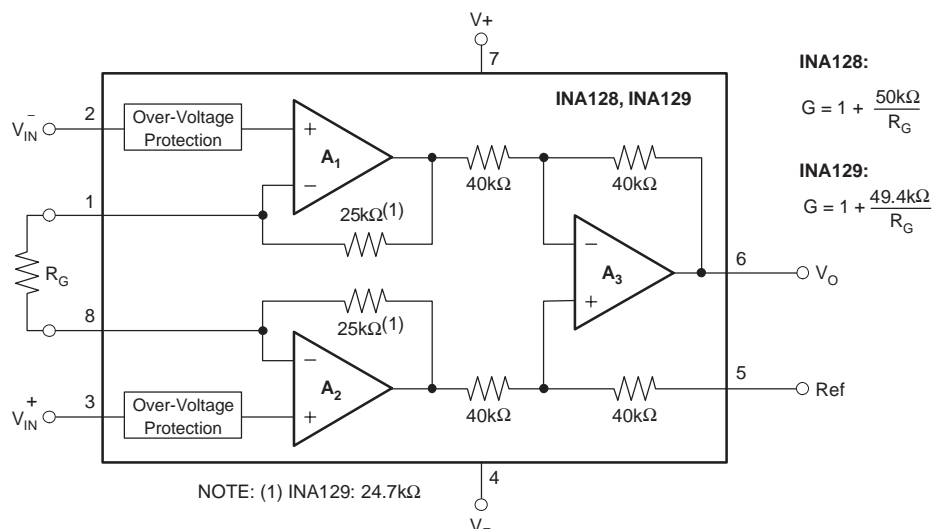
## DESCRIPTION

The INA128 and INA129 are low power, general purpose instrumentation amplifiers offering excellent accuracy. The versatile 3-op amp design and small size make them ideal for a wide range of applications. Current-feedback input circuitry provides wide bandwidth even at high gain (200kHz at G = 100).

A single external resistor sets any gain from 1 to 10,000. The INA128 provides an industry-standard gain equation; the INA129 gain equation is compatible with the AD620.

The INA128/INA129 is laser trimmed for very low offset voltage (50µV), drift (0.5µV/°C) and high common-mode rejection (120dB at G ≥ 100). It operates with power supplies as low as ±2.25V, and quiescent current is only 700µA—ideal for battery-operated systems. Internal input protection can withstand up to ±40V without damage.

The INA128/INA129 is available in 8-pin plastic DIP and SO-8 surface-mount packages, specified for the –40°C to +85°C temperature range. The INA128 is also available in a dual configuration, the INA2128.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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**ABSOLUTE MAXIMUM RATINGS(1)**

Supply Voltage	±18V
Analog Input Voltage Range	±40V
Output Short-Circuit (to ground)	Continuous
Operating Temperature	-40°C to +125°C
Storage Temperature Range	-55°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

**ELECTROSTATIC DISCHARGE SENSITIVITY**



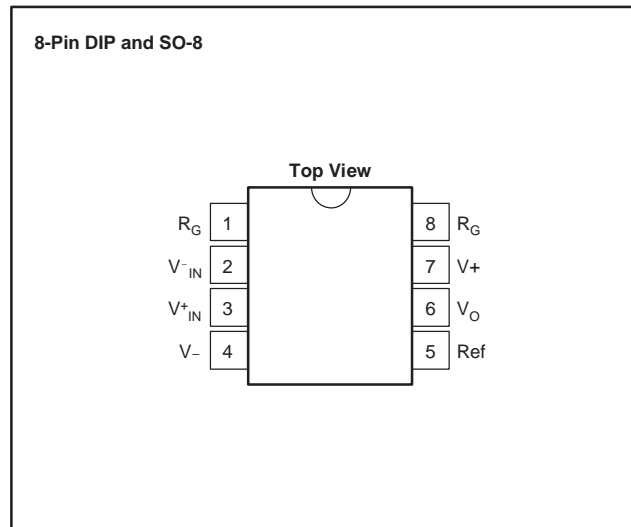
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

**ORDERING INFORMATION**

For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet.

**PIN CONFIGURATION**



**ELECTRICAL CHARACTERISTICS**

 At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ ,  $R_L = 10\text{k}\Omega$ , unless otherwise noted.

PARAMETER	CONDITIONS	INA128P, U INA129P, U			INA128PA, UA INA129PA, UA			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>INPUT</b>								
Offset Voltage, RTI								
Initial	$T_A = +25^\circ\text{C}$		$\pm 10 \pm 100/\text{G}$	$\pm 50 \pm 500/\text{G}$		$\pm 25 \pm 100/\text{G}$	$\pm 125 \pm 1000/\text{G}$	$\mu\text{V}$
vs Temperature	$T_A = T_{\text{MIN}}$ to $T_{\text{MAX}}$		$\pm 0.2 \pm 2/\text{G}$	$\pm 0.5 \pm 20/\text{G}$		$\pm 0.2 \pm 5/\text{G}$	$\pm 1 \pm 20/\text{G}$	$\mu\text{V}/^\circ\text{C}$
vs Power Supply	$V_S = \pm 2.25\text{V}$ to $\pm 18\text{V}$		$\pm 0.2 \pm 20/\text{G}$	$\pm 1 \pm 100/\text{G}$		*	$\pm 2 \pm 200/\text{G}$	$\mu\text{V}/\text{V}$
Long-Term Stability			$\pm 0.1 \pm 3/\text{G}$			*		$\mu\text{V}/\text{mo}$
Impedance, Differential			$10^{10} \parallel 2$			*		$\Omega \parallel \text{pF}$
Common-Mode			$10^{11} \parallel 9$			*		$\Omega \parallel \text{pF}$
Common-Mode Voltage Range <sup>(1)</sup>	$V_O = 0\text{V}$	$(V+) - 2$ $(V-) + 2$	$(V+) - 1.4$ $(V-) + 1.7$		*	*		V
Safe Input Voltage				$\pm 40$		*	*	V
Common-Mode Rejection	$V_{\text{CM}} = \pm 13\text{V}$ , $\Delta R_S = 1\text{k}\Omega$						*	
	$G = 1$	80	86		73	*		dB
	$G = 10$	100	106		93	*		dB
	$G = 100$	120	125		110	*		dB
	$G = 1000$	120	130		110	*		dB
<b>BIAS CURRENT</b>								
vs Temperature			$\pm 2$	$\pm 5$		*	$\pm 10$	nA
Offset Current			$\pm 30$			*		$\text{pA}/^\circ\text{C}$
vs Temperature			$\pm 1$	$\pm 5$		*	$\pm 10$	nA
			$\pm 30$			*		$\text{pA}/^\circ\text{C}$
<b>NOISE VOLTAGE, RTI</b>								
	$G = 1000$ , $R_S = 0\Omega$							
$f = 10\text{Hz}$			10			*		$\text{nV}/\sqrt{\text{Hz}}$
$f = 100\text{Hz}$			8			*		$\text{nV}/\sqrt{\text{Hz}}$
$f = 1\text{kHz}$			8			*		$\text{nV}/\sqrt{\text{Hz}}$
$f_B = 0.1\text{Hz}$ to $10\text{Hz}$			0.2			*		$\mu\text{V}_{\text{pp}}$
Noise Current								
$f = 10\text{Hz}$			0.9			*		$\text{pA}/\sqrt{\text{Hz}}$
$f = 1\text{kHz}$			0.3			*		$\text{pA}/\sqrt{\text{Hz}}$
$f_B = 0.1\text{Hz}$ to $10\text{Hz}$			30			*		$\text{pA}_{\text{pp}}$
<b>GAIN</b>								
Gain Equation, INA128			$1 + (50\text{k}\Omega/R_G)$			*		V/V
INA129			$1 + (49.4\text{k}\Omega/R_G)$			*		V/V
Range of Gain		1		10000	*		*	V/V
Gain Error	$G = 1$		$\pm 0.01$	$\pm 0.024$		*	$\pm 0.1$	%
	$G = 10$		$\pm 0.02$	$\pm 0.4$		*	$\pm 0.5$	%
	$G = 100$		$\pm 0.05$	$\pm 0.5$		*	$\pm 0.7$	%
	$G = 1000$		$\pm 0.5$	$\pm 1$		*	$\pm 2$	%
Gain vs Temperature <sup>(2)</sup>	$G = 1$		$\pm 1$	$\pm 10$		*	*	$\text{ppm}/^\circ\text{C}$
$50\text{k}\Omega$ (or $49.4\text{k}\Omega$ ) Resistance <sup>(2)(3)</sup>			$\pm 25$	$\pm 100$		*	*	$\text{ppm}/^\circ\text{C}$
Nonlinearity	$V_O = \pm 13.6\text{V}$ , $G = 1$		$\pm 0.0001$	$\pm 0.001$		*	$\pm 0.002$	% of FSR
	$G = 10$		$\pm 0.0003$	$\pm 0.002$		*	$\pm 0.004$	% of FSR
	$G = 100$		$\pm 0.0005$	$\pm 0.002$		*	$\pm 0.004$	% of FSR
	$G = 1000$		$\pm 0.001$	(4)		*	*	% of FSR

NOTE: \* Specification is same as INA128P, U or INA129P, U.

(1) Input common-mode range varies with output voltage — see typical curves.

(2) Specified by wafer test.

 (3) Temperature coefficient of the  $50\text{k}\Omega$  (or  $49.4\text{k}\Omega$ ) term in the gain equation.

 (4) Nonlinearity measurements in  $G = 1000$  are dominated by noise. Typical nonlinearity is  $\pm 0.001\%$ .

**ELECTRICAL CHARACTERISTICS (continued)**

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ ,  $R_L = 10\text{k}\Omega$ , unless otherwise noted.

PARAMETER	CONDITIONS	INA128P, U INA129P, U			INA128PA, UA INA129PA, UA			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>OUTPUT</b>								
Voltage: Positive	$R_L = 10\text{k}\Omega$	$(V+) - 1.4$	$(V+) - 0.9$		*	*		V
Negative	$R_L = 10\text{k}\Omega$	$(V-) + 1.4$	$(V-) + 0.8$		*	*		V
Load Capacitance Stability			1000			*		pF
Short-Circuit Current			+6/-15			*		mA
<b>FREQUENCY RESPONSE</b>								
Bandwidth, -3dB	$G = 1$		1.3			*		MHz
	$G = 10$		700			*		kHz
	$G = 100$		200			*		kHz
	$G = 1000$		20			*		kHz
Slew Rate	$V_O = \pm 10\text{V}$ , $G = 10$		4			*		V/ $\mu\text{s}$
Settling Time, 0.01%	$G = 1$		7			*		$\mu\text{s}$
	$G = 10$		7			*		$\mu\text{s}$
	$G = 100$		9			*		$\mu\text{s}$
	$G = 1000$		80			*		$\mu\text{s}$
Overload Recovery	50% Overdrive		4			*		$\mu\text{s}$
<b>POWER SUPPLY</b>								
Voltage Range		$\pm 2.25$	$\pm 15$	$\pm 18$	*	*	*	V
Current, Total	$V_{IN} = 0\text{V}$		$\pm 700$	$\pm 750$		*	*	$\mu\text{A}$
<b>TEMPERATURE RANGE</b>								
Specification		-40		+85	*		*	$^\circ\text{C}$
Operating		-40		+125	*		*	$^\circ\text{C}$
$\theta_{JA}$	8-Pin DIP		80			*		$^\circ\text{C/W}$
	SO-8 SOIC		150			*		$^\circ\text{C/W}$

NOTE: \* Specification is same as INA128P, U or INA129P, U.

(1) Input common-mode range varies with output voltage — see typical curves.

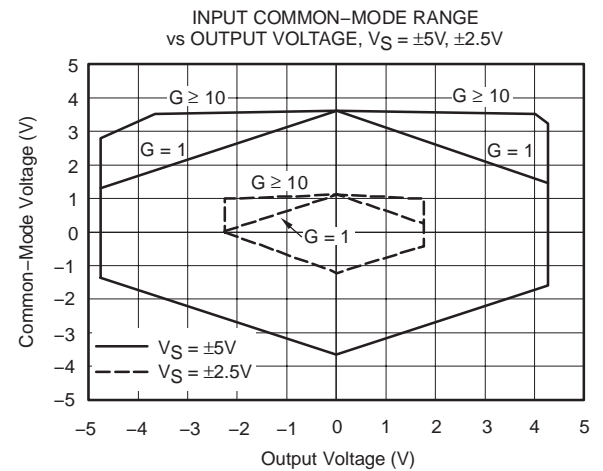
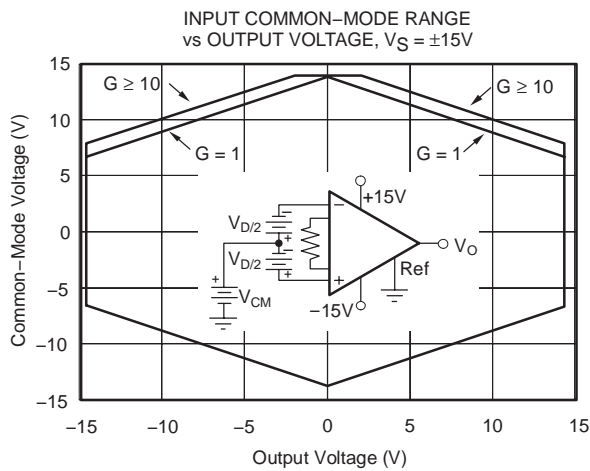
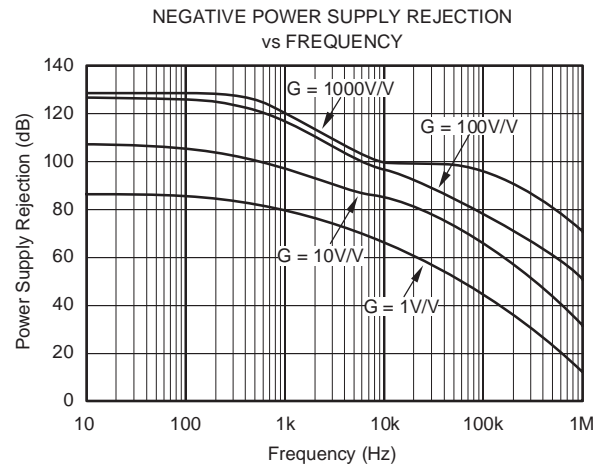
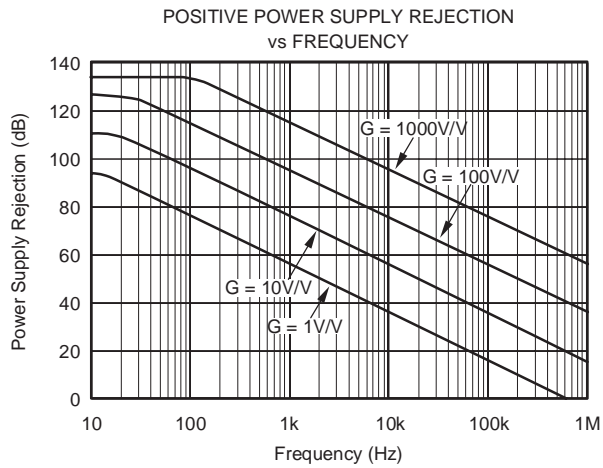
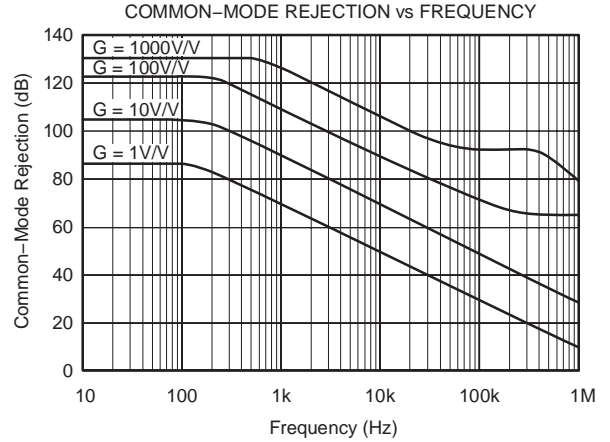
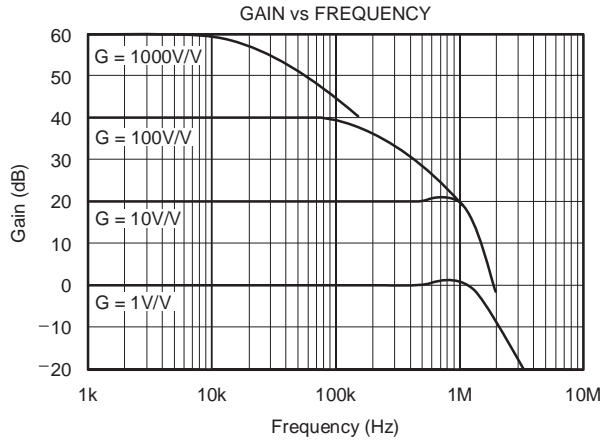
(2) Specified by wafer test.

(3) Temperature coefficient of the  $50\text{k}\Omega$  (or  $49.4\text{k}\Omega$ ) term in the gain equation.

(4) Nonlinearity measurements in  $G = 1000$  are dominated by noise. Typical nonlinearity is  $\pm 0.001\%$ .

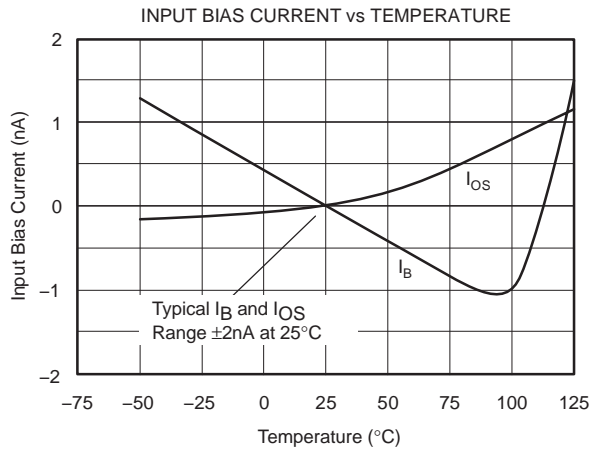
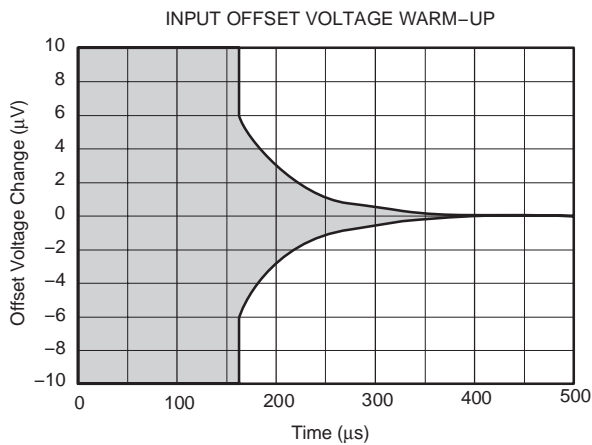
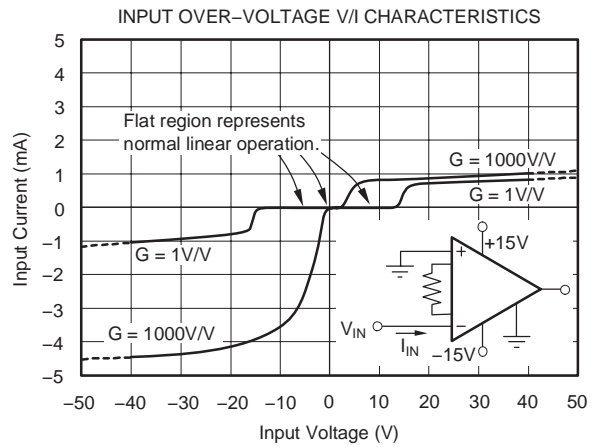
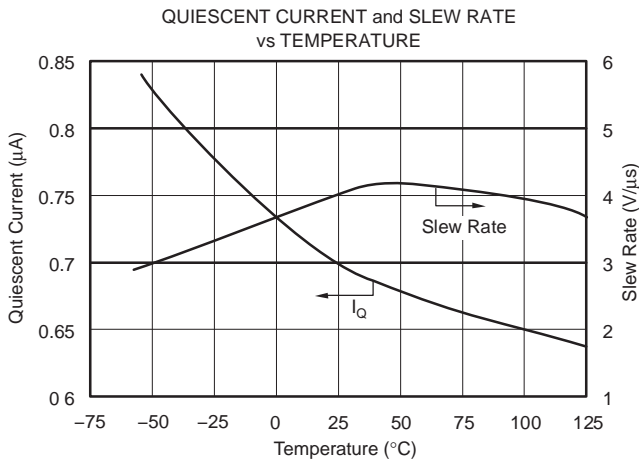
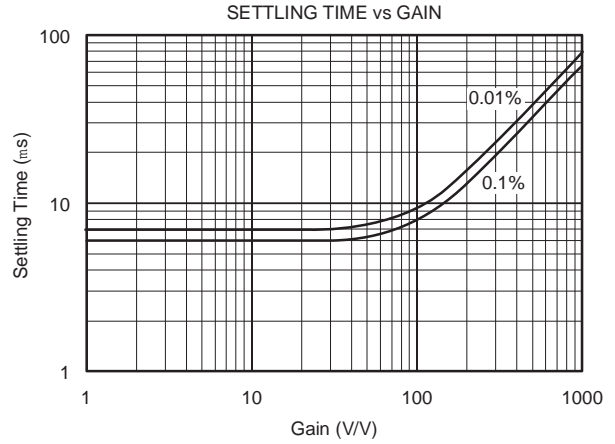
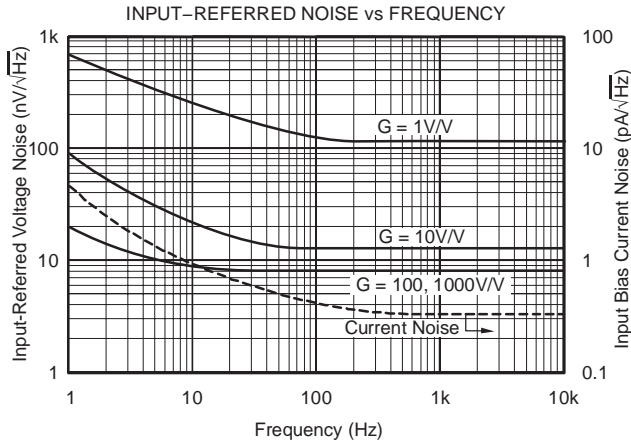
## TYPICAL CHARACTERISTICS

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ , unless otherwise noted.



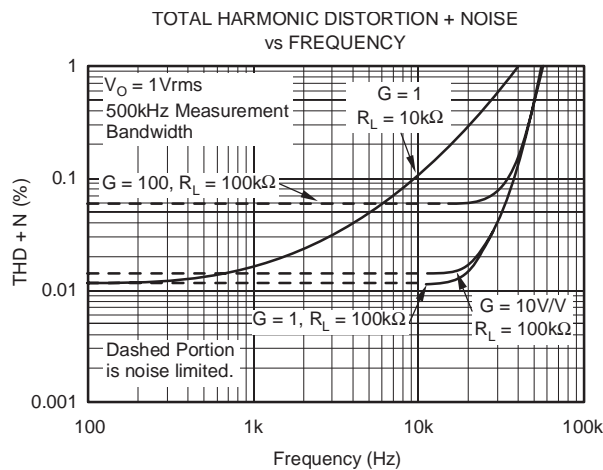
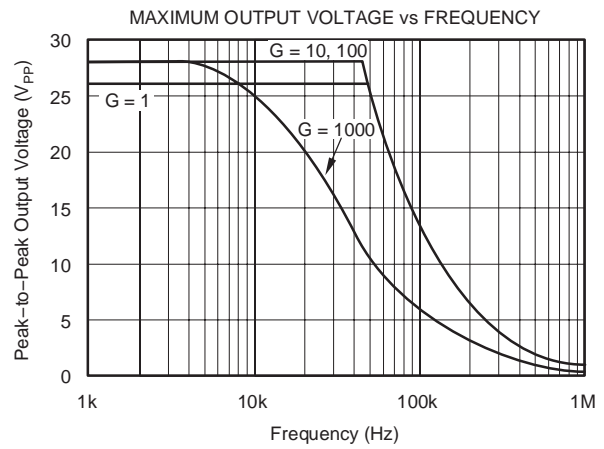
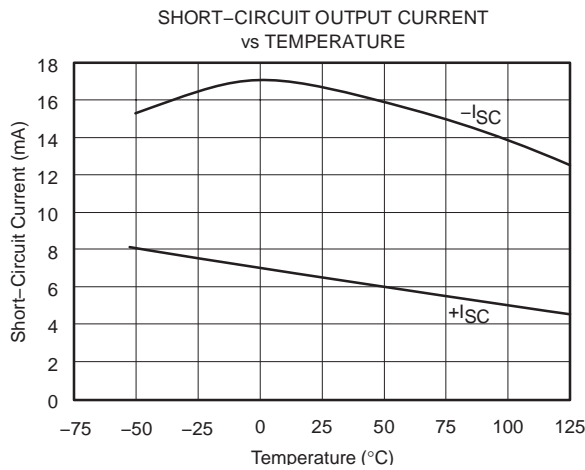
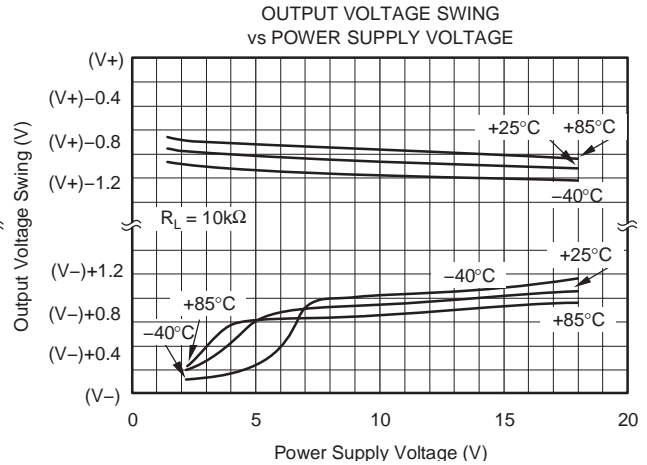
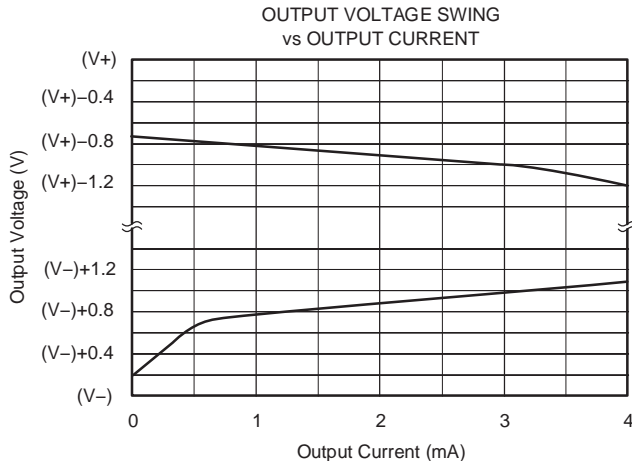
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**TYPICAL CHARACTERISTICS (continued)**

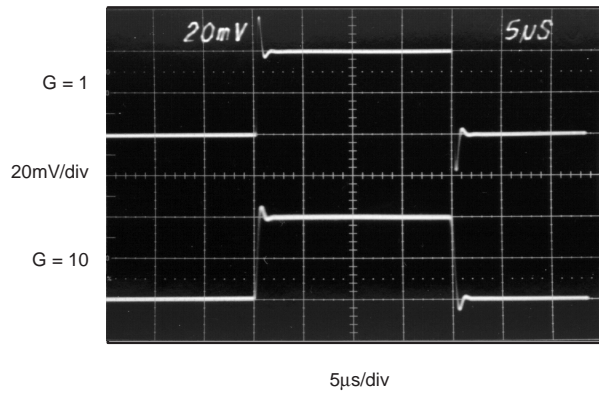
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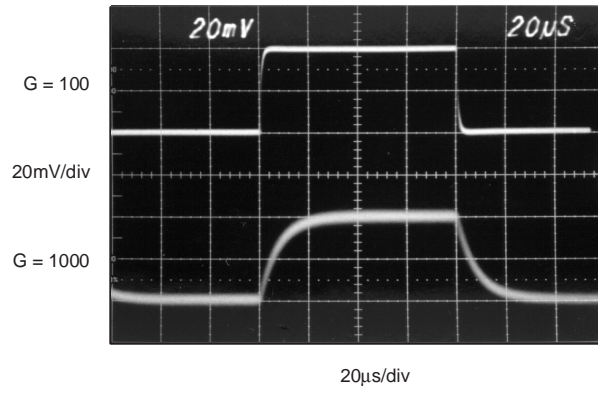
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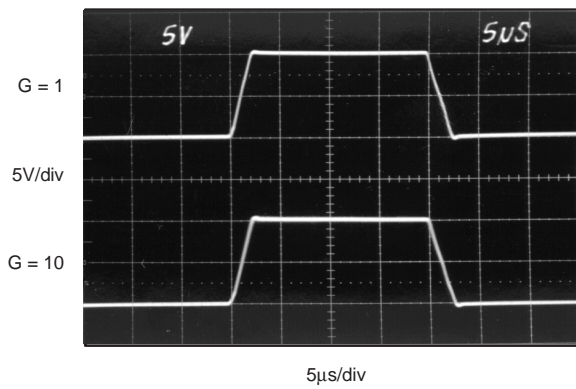
SMALL SIGNAL  
(G = 1, 10)



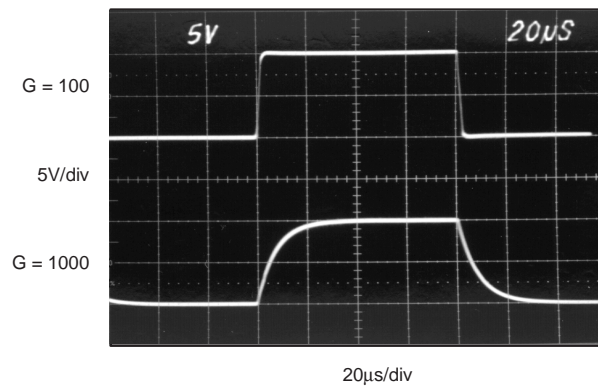
SMALL SIGNAL  
(G = 100, 1000)



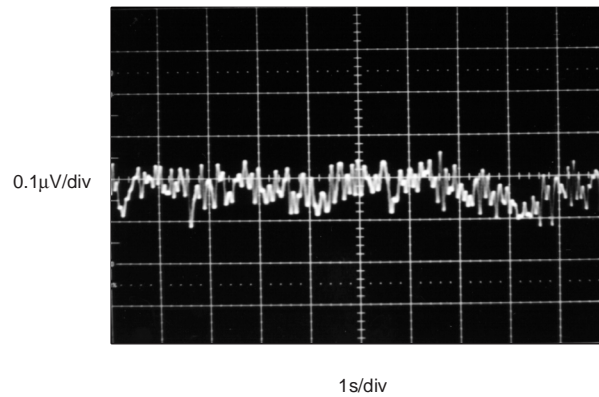
LARGE SIGNAL  
(G = 1, 10)



LARGE SIGNAL  
(G = 100, 1000)



VOLTAGE NOISE 0.1 to 10Hz  
INPUT-REFERRED, G ≥ 100



## APPLICATIONS INFORMATION

Figure 1 shows the basic connections required for operation of the INA128/INA129. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

The output is referred to the output reference (Ref) terminal which is normally grounded. This must be a low-impedance connection to assure good common-mode rejection. A resistance of 8Ω in series with the Ref pin will cause a typical device to degrade to approximately 80dB CMR ( $G = 1$ ).

### SETTING THE GAIN

Gain is set by connecting a single external resistor,  $R_G$ , connected between pins 1 and 8:

INA128:

$$G = 1 + \frac{50k\Omega}{R_G} \quad (1)$$

INA129:

$$G = 1 + \frac{49.4k\Omega}{R_G} \quad (2)$$

Commonly used gains and resistor values are shown in Figure 1.

The 50kΩ term in Equation 1 (49.4kΩ in Equation 2) comes from the sum of the two internal feedback resistors of  $A_1$  and  $A_2$ . These on-chip metal film

resistors are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of these internal resistors are included in the gain accuracy and drift specifications of the INA128/INA129.

The stability and temperature drift of the external gain setting resistor,  $R_G$ , also affects gain.  $R_G$ 's contribution to gain accuracy and drift can be directly inferred from the gain equation (1). Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance which will contribute additional gain error (possibly an unstable gain error) in gains of approximately 100 or greater.

### DYNAMIC PERFORMANCE

The typical performance curve *Gain vs Frequency* shows that, despite its low quiescent current, the INA128/INA129 achieves wide bandwidth, even at high gain. This is due to the current-feedback topology of the input stage circuitry. Settling time also remains excellent at high gain.

### NOISE PERFORMANCE

The INA128/INA129 provides very low noise in most applications. Low frequency noise is approximately  $0.2\mu V_{PP}$  measured from 0.1 to 10Hz ( $G \geq 100$ ). This provides dramatically improved noise when compared to state-of-the-art chopper-stabilized amplifiers.

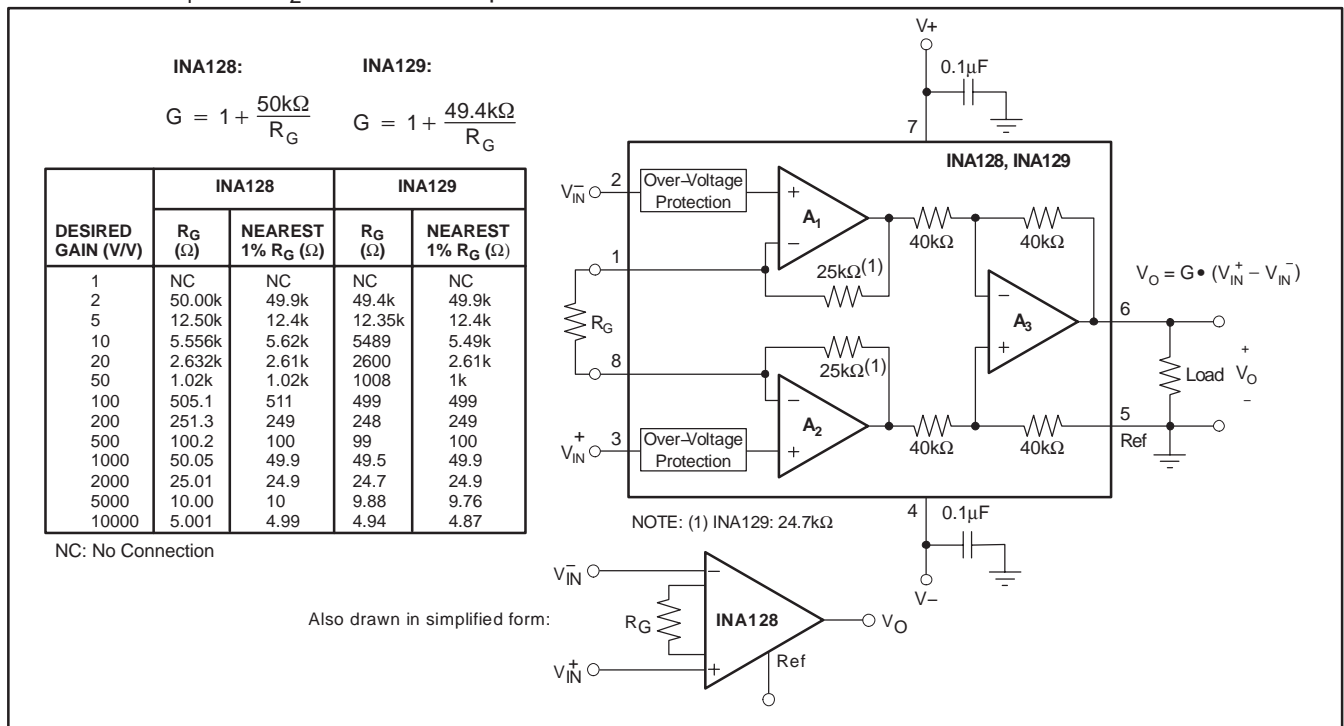


Figure 1. Basic Connections

## OFFSET TRIMMING

The INA128/INA129 is laser trimmed for low offset voltage and offset voltage drift. Most applications require no external offset adjustment. Figure 2 shows an optional circuit for trimming the output offset voltage. The voltage applied to Ref terminal is summed with the output. The op amp buffer provides low impedance at the Ref terminal to preserve good common-mode rejection.

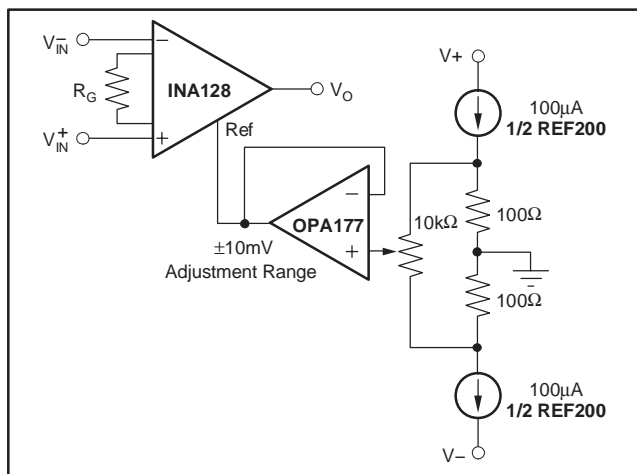


Figure 2. Optional Trimming of Output Offset Voltage

## INPUT BIAS CURRENT RETURN PATH

The input impedance of the INA128/INA129 is extremely high—approximately  $10^{10}\Omega$ . However, a path must be provided for the input bias current of both inputs. This input bias current is approximately  $\pm 2\text{nA}$ . High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. Figure 3 shows various provisions for an input bias current path. Without a bias current path, the inputs will float to a potential which exceeds the common-mode range, and the input amplifiers will saturate.

If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in Figure 3). With higher source impedance, using two equal resistors provides a balanced input with possible advantages of lower input offset voltage due to bias current and better high-frequency common-mode rejection.

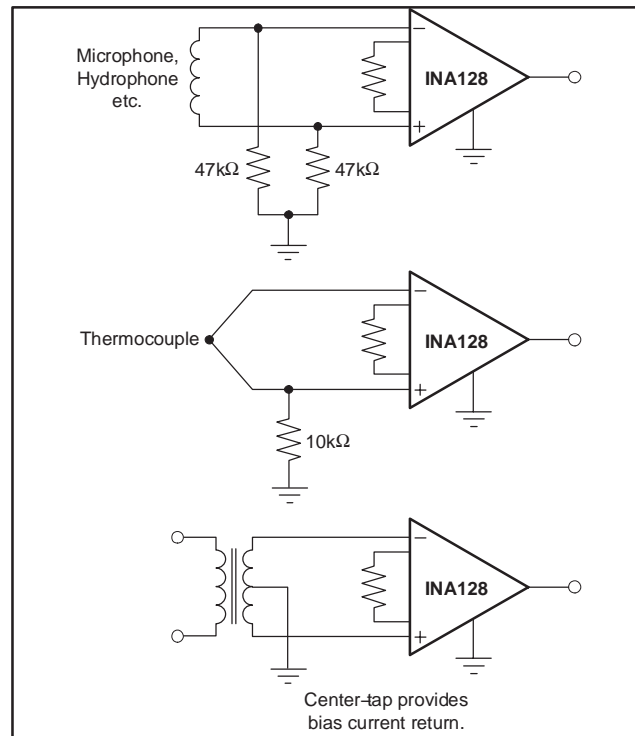


Figure 3. Providing an Input Common-Mode Current Path

## INPUT COMMON-MODE RANGE

The linear input voltage range of the input circuitry of the INA128/INA129 is from approximately 1.4V below the positive supply voltage to 1.7V above the negative supply. As a differential input voltage causes the output voltage increase, however, the linear input range will be limited by the output voltage swing of amplifiers  $A_1$  and  $A_2$ . So the linear common-mode input range is related to the output voltage of the complete amplifier. This behavior also depends on supply voltage—see performance curves, *Input Common-Mode Range vs Output Voltage*.

Input-overload can produce an output voltage that appears normal. For example, if an input overload condition drives both input amplifiers to their positive output swing limit, the difference voltage measured by the output amplifier will be near zero. The output of  $A_3$  will be near 0V even though both inputs are overloaded.

## LOW VOLTAGE OPERATION

The INA128/INA129 can be operated on power supplies as low as  $\pm 2.25\text{V}$ . Performance remains excellent with power supplies ranging from  $\pm 2.25\text{V}$  to  $\pm 18\text{V}$ . Most parameters vary only slightly throughout this supply voltage range—see typical performance curves.

Operation at very low supply voltage requires careful attention to assure that the input voltages remain within their linear range. Voltage swing requirements of internal nodes limit the input common-mode range with low power supply voltage. Typical performance curves, "Input Common-Mode Range vs Output Voltage" show the range of linear operation for  $\pm 15V$ ,  $\pm 5V$ , and  $\pm 2.5V$  supplies.

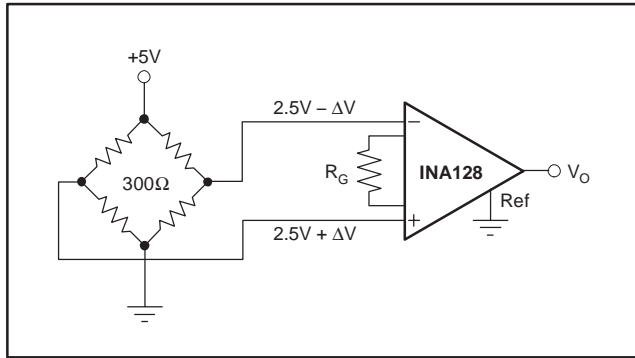


Figure 4. Bridge Amplifier

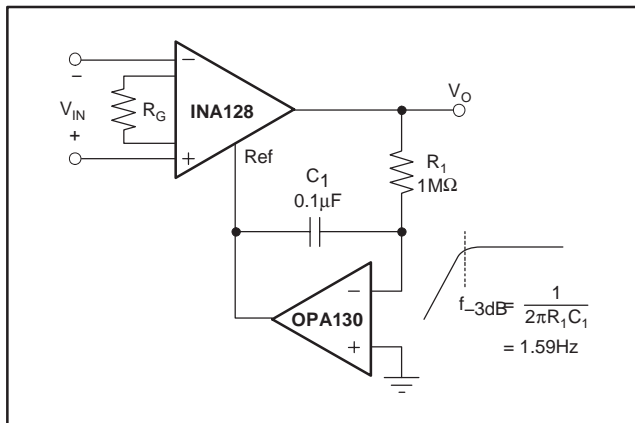


Figure 5. AC-Coupled Instrumentation Amplifier

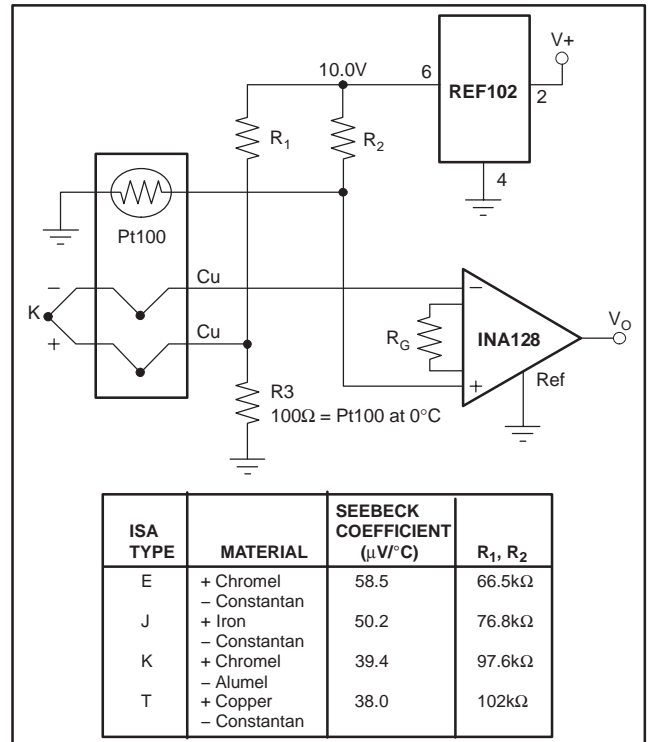


Figure 6. Thermocouple Amplifier with RTD Cold-Junction Compensation

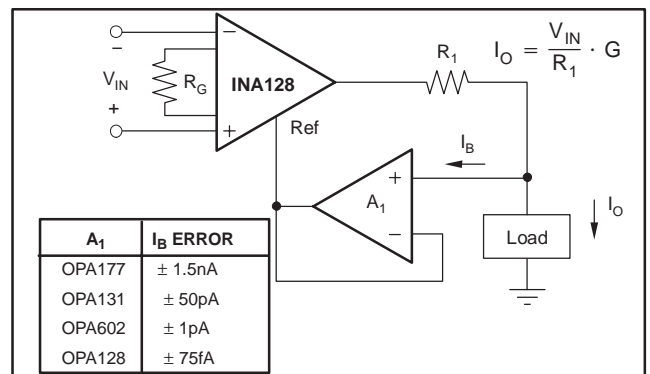


Figure 7. Differential Voltage to Current Converter

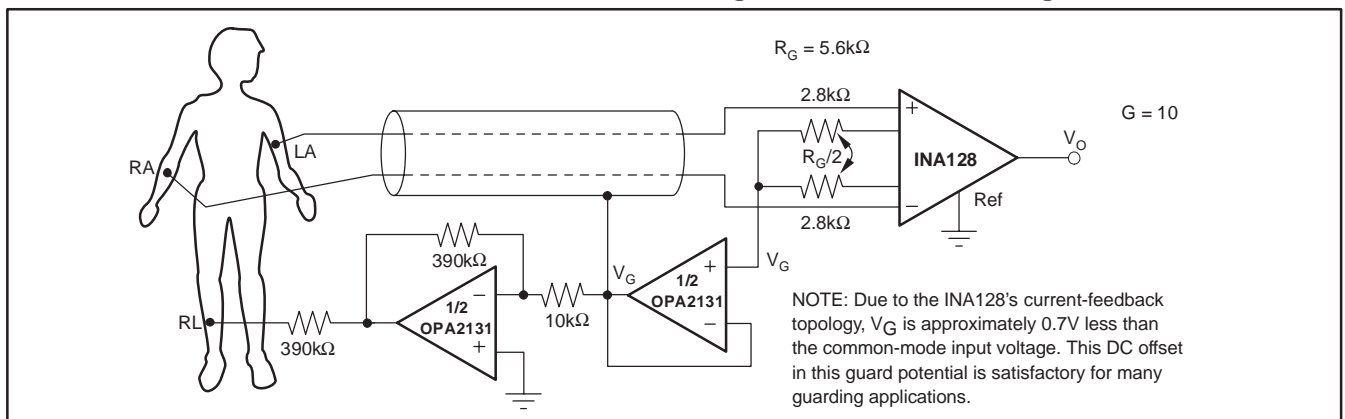


Figure 8. ECG Amplifier with Right-Leg Drive

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
INA128P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
INA128PA	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
INA128PAG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
INA128PG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
INA128U	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA128U/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA128U/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA128UA	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA128UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA128UA/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA128UA/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA128UAE4	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA128UAG4	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA128UG4	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA129P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
INA129PA	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
INA129PAG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
INA129U	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA129U/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA129U/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA129UA	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA129UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA129UA/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA129UA/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA129UAE4	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
INA129UG4	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
SN412014DRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

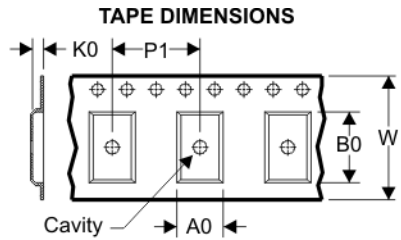
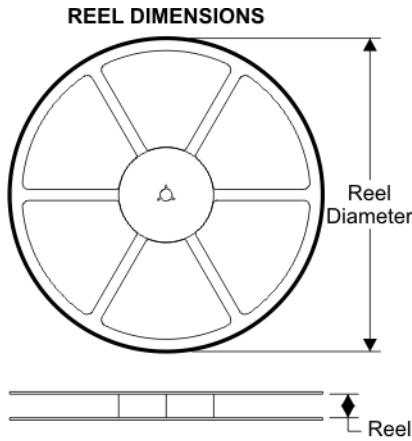
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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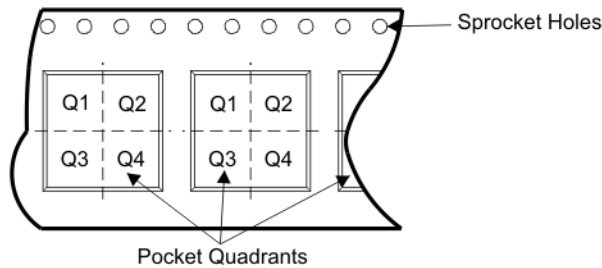
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**TAPE AND REEL BOX INFORMATION**



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA128U/2K5	D	8	SITE 41	330	12	6.4	5.2	2.1	8	12	Q1
INA128UA/2K5	D	8	SITE 41	330	12	6.4	5.2	2.1	8	12	Q1
INA129U/2K5	D	8	SITE 41	330	12	6.4	5.2	2.1	8	12	Q1
INA129UA/2K5	D	8	SITE 41	330	12	6.4	5.2	2.1	8	12	Q1
INA129UA/2K5G4	D	8	SITE 41	330	12	6.4	5.2	2.1	8	12	Q1

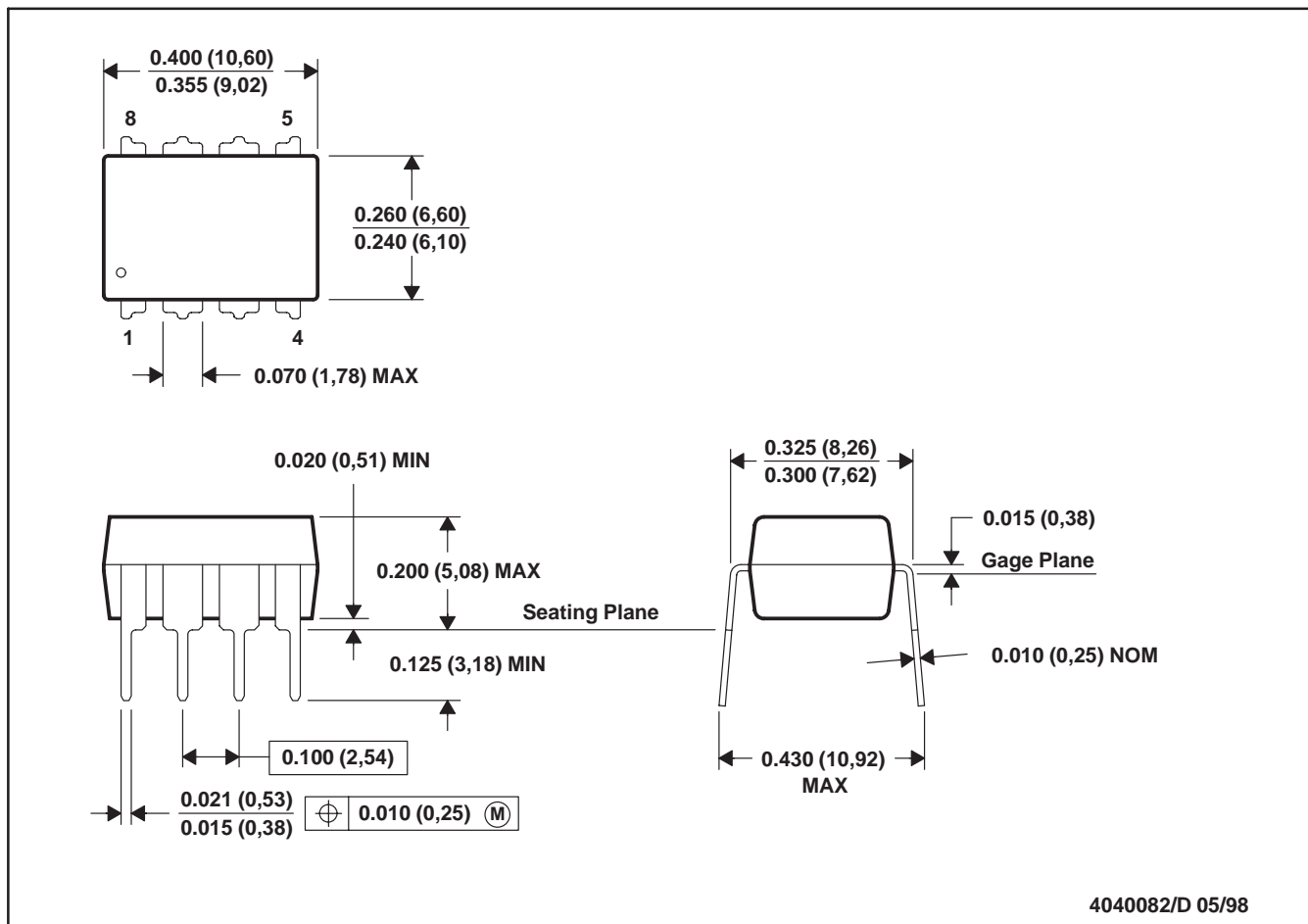
**TAPE AND REEL BOX DIMENSIONS**



Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
INA128U/2K5	D	8	SITE 41	346.0	346.0	29.0
INA128UA/2K5	D	8	SITE 41	346.0	346.0	29.0
INA129U/2K5	D	8	SITE 41	346.0	346.0	29.0
INA129UA/2K5	D	8	SITE 41	346.0	346.0	29.0
INA129UA/2K5G4	D	8	SITE 41	346.0	346.0	29.0

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE



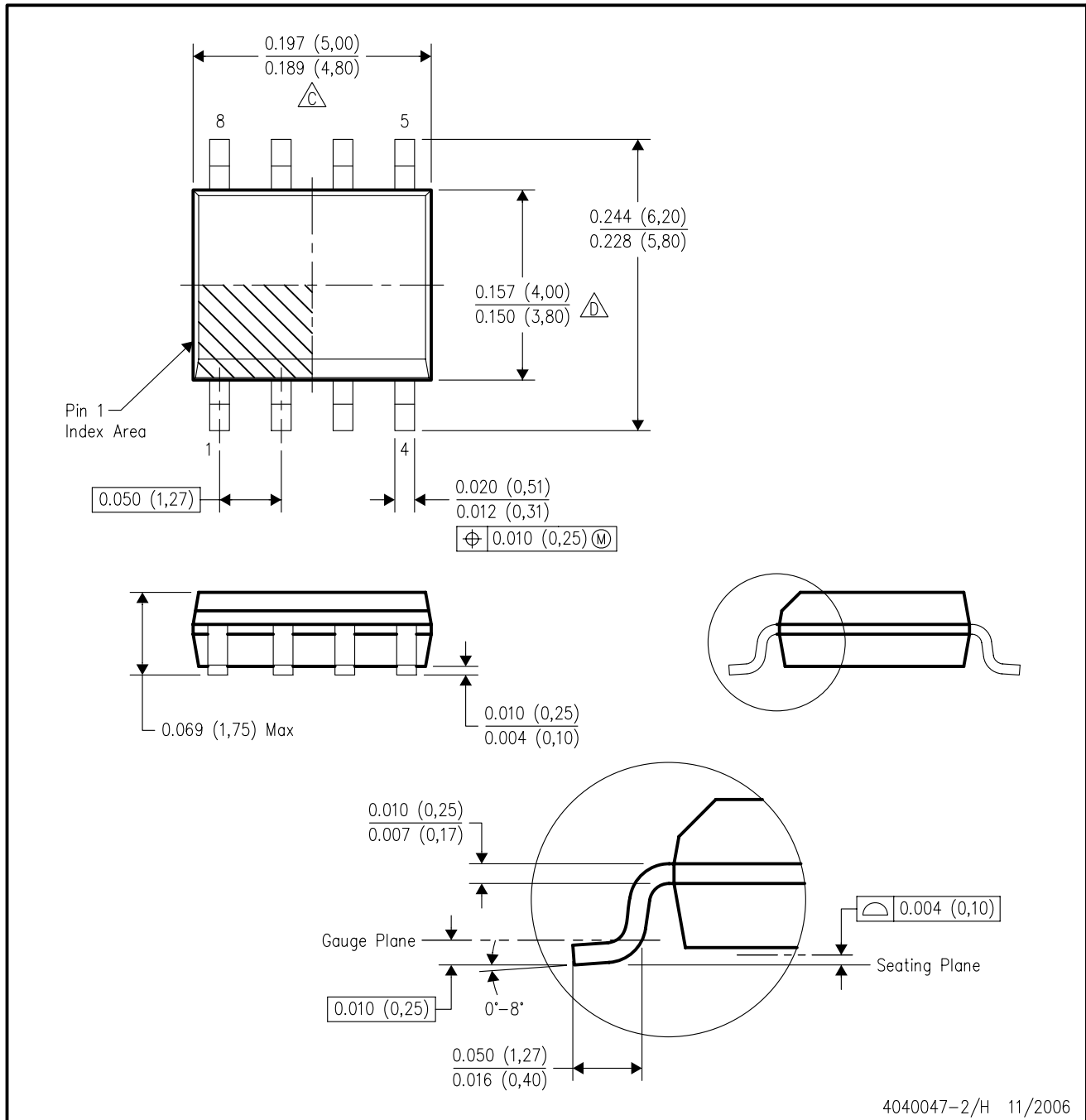
- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-001

For the latest package information, go to [http://www.ti.com/sc/docs/package/pkg\\_info.htm](http://www.ti.com/sc/docs/package/pkg_info.htm)



D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
  - E. Reference JEDEC MS-012 variation AA.

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