### LF444QML

LF444QML Quad Low Power JFET Input Operational Amplifier



Literature Number: SNOSAO9



### LF444QML

## **Quad Low Power JFET Input Operational Amplifier**

### **General Description**

The LF444 quad low power operational amplifier provides many of the same AC characteristics as the industry standard LM148 while greatly improving the DC characteristics of the LM148. The amplifier has the same bandwidth, slew rate, and gain (10 k $\Omega$  load) as the LM148 and only draws one fourth the supply current of the LM148. In addition the well matched high voltage JFET input devices of the LF444 reduce the input bias and offset currents by a factor of 10,000 over the LM148. The LF444 also has a very low equivalent input noise voltage for a low power amplifier.

The LF444 is pin compatible with the LM148 allowing an immediate 4 times reduction in power drain in many applications. The LF444 should be used wherever low power dissipation and good electrical characteristics are the major considerations.

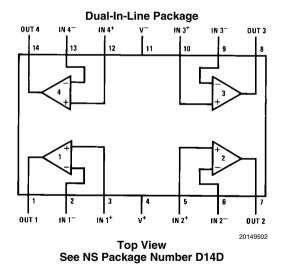
#### **Features**

- ¼ supply current of a LM148: 250 µA/Amplifier (max)
- Low input bias current: 100 pA (max)
- High gain bandwidth: 1 MHz
- High slew rate: 1 V/µs
- Low noise voltage for low power 35 nV/√Hz
- Low input noise current 0.01 pA/√Hz
- High input impedance: 10<sup>12</sup>Ω
- High gain,  $V_{\Omega} = \pm 10V$ ,  $R_{I} = 10K\Omega$ : 25K (min)

### **Ordering Information**

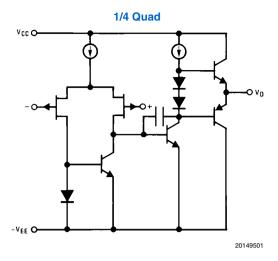
NS Part Number	SMD Part Number	NS Package Number	Package Description
LF444MD/883		D14D	14LD Sidebraze Ceramic Dip

### **Connection Diagram**

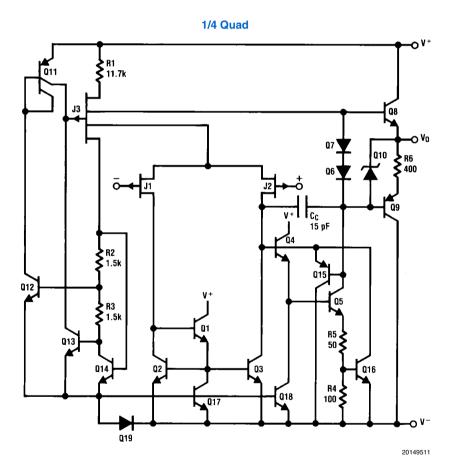


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# **Simplified Schematic**



### **Detailed Schematic**



### **Absolute Maximum Ratings** (Note 1)

Supply Voltage
Differential Input Voltage
Input Voltage Range (*Note 4*)
Output Short Circuit Duration (*Note 5*)

Power Dissipation (*Note 2*), (*Note 3*)

 $\mathsf{T}_{\mathsf{Jmax}}$ 

 $\theta_{JA} \ (Typical)$ 

Operating Temperature Range

Storage Temperature Range

ESD Tolerance (Note 6)

±18V ±30V ±15V Continuous 900 mW 150°C 100°C/W

 $-55^{\circ}\text{C} \le \text{T}_{\text{A}} \le 125^{\circ}\text{C}$  $-65^{\circ}\text{C} \le \text{T}_{\text{A}} \le 150^{\circ}\text{C}$ Rating to be determined

### **Quality Conformance Inspection**

Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55
12	Settling time at	+25
13	Settling time at	+125
14	Settling time at	-55

#### **LF444 Electrical Characteristics**

#### **DC Parameters**

The following conditions apply, unless otherwise specified.  $V_S = \pm 15V$ ,  $V_{CM} = 0V$ ,  $R_S = 0\Omega$ ,  $R_L = 0\Omega$ 

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub- groups
V	Input Offset Voltage	B 10KO		-10	10	mV	1
V <sub>IO</sub>	Input Onset voltage	$R_S = 10K\Omega$		-14	14	mV	2, 3
I <sub>IO</sub>	Input Offset Current	$R_L = 10K\Omega$		-0.05	0.05	nA	1
-10	Imput Oncot Current			-10	10	nA	2
+l <sub>IB</sub>	Input Bias Current	$R_1 = 10K\Omega$		-0.10	0.10	nA	1
	input Blas Sallsill	11[ - 10.22	<u> </u>	-20	20	nA	2
-I <sub>IB</sub>	Input Bias Current	$R_1 = 10K\Omega$		-0.10	0.10	nA	1
		_		-20	20	nA	2
+A <sub>VS</sub>	Large Signal Voltage Gain	$V_{O} = 0 \text{ to } +10V,$	(Note 8)	25		V/mV	1
TAVS	Large Signal Voltage Cam	$R_L = 10K\Omega, R_S = 10K\Omega$	(Note of	15		V/mV	2, 3
Λ	Larga Signal Voltage Gein	$V_{O} = 0 \text{ to } -10V,$	(Note 9)	25		V/mV	1
-A <sub>VS</sub>	Large Signal Voltage Gain	$R_L = 10K\Omega$ , $R_S = 10K\Omega$	(Note 8)	15		V/mV	2, 3
+V <sub>O</sub>	Output Voltage Swing	$R_L = 10K\Omega, V_I = +1V$		12		V	1, 2, 3
-V <sub>O</sub>	Output Voltage Swing	$R_L = 10K\Omega$ , $V_I = -1V$			-12	V	1, 2, 3
V <sub>CM</sub>	Input Common Mode Voltage Range		(Note 7)	9	-9	V	1, 2, 3
CMRR	Common Mode Rejection Ratio	$R_S = 10K\Omega$ , $V_{CM} = \pm 9V$		70		dB	1, 2, 3
PSRR+	Power Supply Rejection Ratio	$V_{S} = \pm 15V \text{ to } V_{S} = \pm 6V$		70		dB	1, 2, 3
PSRR-	Power Supply Rejection Ratio	$V_S = \pm 15V$ to $V_S = \pm 6V$		70		dB	1, 2, 3
I <sub>S</sub>	Supply Current				1.0	mA	1, 2, 3
	Output Short Circuit Current	V <sub>1</sub> = 1V		-3.0	-20	mA	1
	Output Short Circuit Current			-3.0	-40	mA	2, 3
	Output Short Circuit Current	V <sub>I</sub> = -1V		3.0	20	mA	1
-l <sub>os</sub>	Catput Short Shoult Guilent			3.0	40	mA	2, 3

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by  $T_{Jmax}$  (maximum junction temperature),  $\theta_{JA}$  (package junction to ambient thermal resistance), and  $T_A$  (ambient temperature). The maximum allowable power dissipation at any temperature is  $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$  or the number given in the Absolute Maximum Ratings, whichever is lower.

**Note 3:** Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

Note 4: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

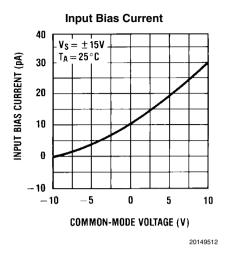
Note 5: Any of the amplifier outputs can be shorted to ground indefinitely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

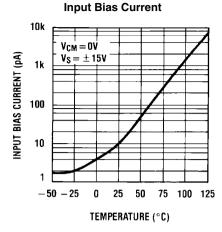
Note 6: Human body model, 1.5  $k\Omega$  in series with 100 pF.

Note 7: Parameter tested go-no-go only. Guaranteed by the CMRR test.

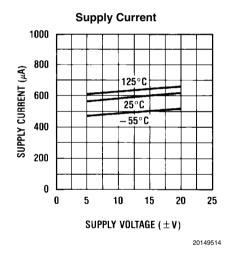
Note 8: Datalog in K = V/mV.

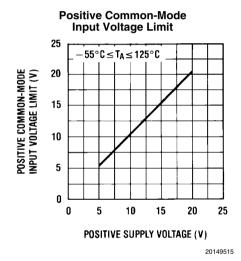
### **Typical Performance Characteristics**





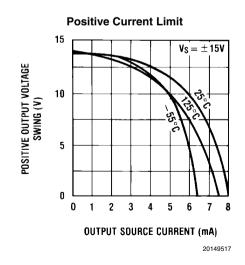
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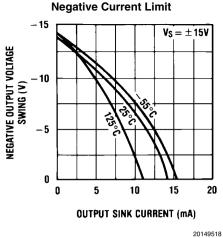


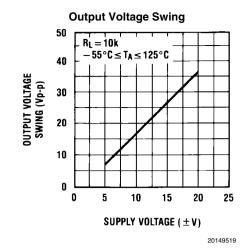


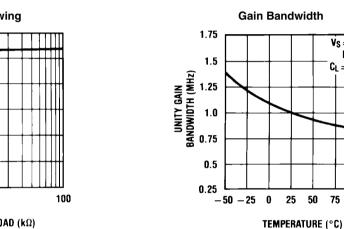
Negative Common-Mode Input Voltage Limit  $-25 \\ -55^{\circ}\text{C} \leq \text{T}_{A} \leq 125^{\circ}\text{C}$   $-10 \\ 0 \\ -5 \\ -10 \\ -15 \\ 0 \\ 0 \\ -5 \\ -10 \\ -15 \\ -20 \\ -25$ NEGATIVE SUPPLY VOLTAGE (V)

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**Output Voltage Swing**  $V_S = \pm 15V$ T<sub>A</sub> = 25°C 25 OUTPUT VOLTAGE SWING (Vp-p) 20 15 10 5 0 1 10  $R_L$ -OUTPUT LOAD  $(k\Omega)$ 

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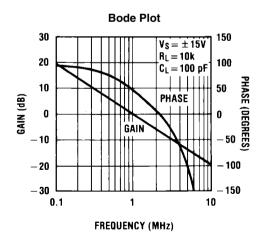
100 125

50 75

 $\dot{V}_S = \pm 15V$ 

 $C_L = 100 \text{ pF}$ 

 $R_L = 10k$ 

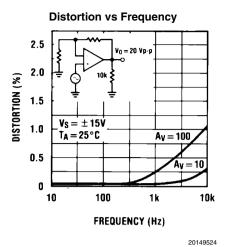


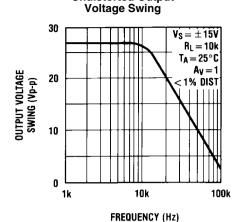
**Slew Rate** 2.0  $V_S = \pm 15V$ R<sub>L</sub> = 10k  $A_{V} = 1$ 1.5 SLEW RATE (V/µs) **FALLING** RISING 1.0 0.5 -50 - 250 25 50 75 100 125 TEMPERATURE (°C)

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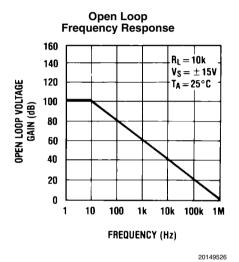
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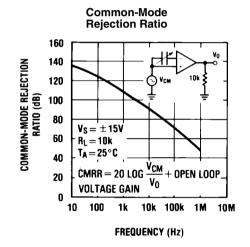




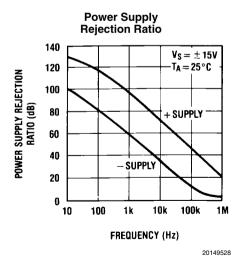
**Undistorted Output** 

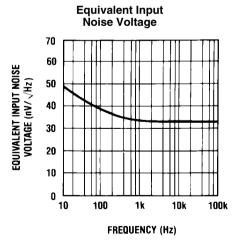
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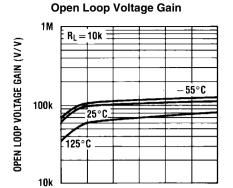
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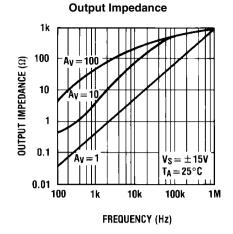


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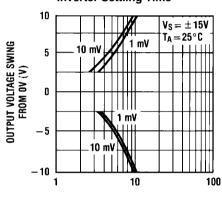
SUPPLY VOLTAGE (  $\pm$  V)



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#### **Inverter Settling Time**

10



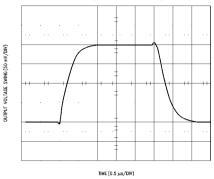
SETTLING TIME ( $\mu$ s)

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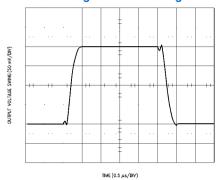
### **Pulse Response**

 $R_{L} = 10 \text{ k}\Omega, C_{L} = 10 \text{ pF}$ 

#### **Small Signal Inverting**



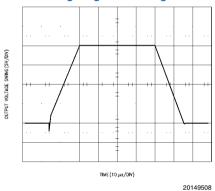
#### **Small Signal Non-Inverting**



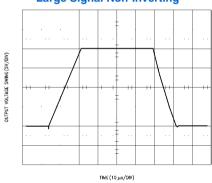
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#### **Large Signal Inverting**

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**Large Signal Non-Inverting** 



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#### **Application Hints**

This device is a quad low power op amp with JFET input devices (BI-FET®). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode. Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased to allow normal circuit operation with power supplies of ±3.0V. Supply voltages less than these may degrade the common-mode rejection and restrict the output voltage swing.

The amplifiers will drive a 10 k $\Omega$  load resistance to  $\pm 10V$  over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

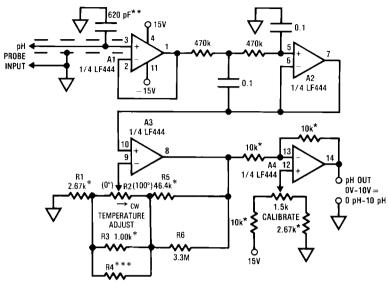
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

### **Typical Application**

#### pH Probe Amplifier/Temperature Compensator



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\*\*\*For R2 =  $50k\Omega$ , R4 = 330k ±1%

For R2 = 100k, R4 =  $75k \pm 1\%$ 

For R2 = 200k, R4 =  $56k \pm 1\%$ 

\*\*Polystyrene

\*Film resistor type RN60C

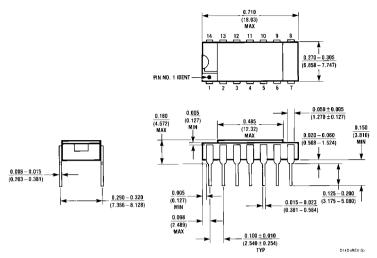
To calibrate, insert probe in pH =7 solution. Set the "TEMPERATURE ADJUST" pot, R2, to correspond to the solution temperature: full clockwise for  $0^{\circ}$ C, and proportionately for intermediate temperatures, using a turns-counting dial. Then set "CALIBRATE" pot so output reads 7V.

Typical probe = Ingold Electrodes #465-35

# **Revision History**

Date Released	Revision	Section	Changes
12/16/2010	Α	New release to corporate format	1 MDS datasheet converted to standard corporate format, MDS MNLF444M-X Rev 0AL will be
			archived.

### Physical Dimensions inches (millimeters) unless otherwise noted



See NS Package Number D14D

#### **Notes**

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