Stellaris® LM3S6911 RevA2 Errata

This document contains known errata at the time of publication for the Stellaris LM3S6911 microcontroller. The table below summarizes the errata and lists the affected revisions. See the data sheet for more details.

See also the ARM® Cortex™-M3 errata, ARM publication number PR326-PRDC-009450 v2.0.

Table 1. Revision History

Date	Revision	Description
August 2011	3.0	■ Added issue “Standard R-C network cannot be used on $\overline{\text{RST}}$ to extend POR timing” on page 5. ■ Clarified issue “General-purpose timer 16-bit Edge Count or Edge Time mode does not load reload value” on page 8 to include Edge-Time mode.
September 2010	2.10	■ Added issue “Hibernation module does not operate correctly” on page 5, replacing previous Hibernation module errata items. ■ Minor edits and clarifications.
July 2010	2.9	■ Added issue “The RTRIS bit in the UARTRIS register is only set when the interrupt is enabled” on page 8.
June 2010	2.8	■ Added issue “External reset does not reset the XTAL to PLL Translation (PLLCFG) register” on page 5.
May 2010	2.7	■ Removed issue "Hibernation Module 4.194304-MHz oscillator supports a limited range of crystal load capacitance values" as it does not apply to this part. ■ Minor edits and clarifications.
April 2010	2.6	■ Removed issue "Writes to Hibernation module registers sometimes fail" as it does not apply to this part. ■ Added issue "Hibernation Module 4.194304-MHz oscillator supports a limited range of crystal load capacitance values." ■ Minor edits and clarifications.
April 2010	2.5	■ Removed issue "Setting Bit 7 in I2C Master Timer Period (I2CMTPR) register may have unexpected results". The data sheet description has changed such that this is no longer necessary. ■ Minor edits and clarifications.
February 2010	2.4	■ Added issue “The General-Purpose Timer match register does not function correctly in 32-bit mode” on page 8. ■ Added issue "Setting Bit 7 in I2C Master Timer Period (I2CMTPR) register may have unexpected results".
Jan 2010	2.3	■ "Hard Fault possible when waking from Sleep or Deep-Sleep modes and Cortex-M3 Debug Access Port (DAP) is enabled" has been removed and the content added to the LM3S6911 data sheet. ■ "Ethernet number of Packets decremented early" has been removed and the content added to the LM3S6911 data sheet.
Dec 2009	2.2	Started tracking revision history.

Table 2. List of Errata

Erratum Number	Erratum Title	Module Affected	Revision(s) Affected
1.1	JTAG pins do not have internal pull-ups enabled at power-on reset	JTAG and Serial Wire Debug	A2
1.2	JTAG INTEST instruction does not work	JTAG and Serial Wire Debug	A2
2.1	Clock source incorrect when waking up from Deep-Sleep mode in some configurations	System Control	A2
2.2	PLL may not function properly at default LDO setting	System Control	A2
2.3	I/O buffer 5-V tolerance issue	System Control	A2
2.4	PLL Runs Fast When Using a 3.6864-MHz Crystal	System Control	A2
2.5	External reset does not reset the XTAL to PLL Translation (PLLCFG) register	System Control	A2
2.6	Standard R-C network cannot be used on $\overline{\text{RST}}$ to extend POR timing	System Control	A2
3.1	Hibernation module does not operate correctly	Hibernation Module	A2
4.1	MERASE bit of the FMC register does not erase the entire Flash array	Flash Controller	A2
5.1	GPIO input pin latches in the Low state if pad type is open drain	GPIO	A2
5.2	GPIO pins may glitch during power supply ramp up	GPIO	A2
6.1	General-purpose timer Edge Count mode count error when timer is disabled	General-Purpose Timers	A2
6.2	General-purpose timer 16-bit Edge Count or Edge Time mode does not load reload value	General-Purpose Timers	A2
6.3	The General-Purpose Timer match register does not function correctly in 32-bit mode	General-Purpose Timers	A2
7.1	The RTRIS bit in the UARTRIS register is only set when the interrupt is enabled	UART	A2

1 JTAG and Serial Wire Debug

1.1 JTAG pins do not have internal pull-ups enabled at power-on reset

Description:

Following a power-on reset, the JTAG pins $\overline{\text{TRST}}$, TCK, TMS, TDI, and TDO (PB7 and PC[3:0]) do not have internal pull-ups enabled. Consequently, if these pins are not driven from the board, two things may happen:

- The JTAG port may be held in reset and communication with a four-pin JTAG-based debugger may be intermittent or impossible.
- The receivers may draw excess current.

Workaround:

There are a number of workarounds for this problem, varying in complexity and impact:

1. Add external pull-up resistors to all of the affected pins. This workaround solves both issues of JTAG connectivity and current consumption.

2. Add an external pull-up resistor to TRST. Firmware should enable the internal pull-ups on the affected pins by setting the appropriate PUE bits of the appropriate **GPIO Pull-Up Select (GPIOPUR)** registers as early in the reset handler as possible. This workaround addresses the issue of JTAG connectivity, but does not address the current consumption other than to limit the affected period (from power-on reset to code execution).

3. Pull-ups on the JTAG pins are unnecessary for code loaded via the SWD interface or via the serial boot loader. Loaded firmware should enable the internal pull-ups on the affected pins by setting the appropriate PUE bits of the appropriate **GPIOPUR** registers as early in the reset handler as possible. This method does not address the current consumption other than to limit the affected period (from power-on reset to code execution).

Silicon Revision Affected:

A2

1.2 JTAG INTEST instruction does not work

Description:

The JTAG INTEST (Boundary Scan) instruction does not properly capture data.

Workaround:

None.

Silicon Revision Affected:

A2

2 System Control

2.1 Clock source incorrect when waking up from Deep-Sleep mode in some configurations

Description:

In some clocking configurations, the core prematurely starts executing code before the main oscillator (MOSC) has stabilized after waking up from Deep-Sleep mode. This situation can cause undesirable behavior for operations that are frequency dependent, such as UART communication.

This issue occurs if the system is configured to run off the main oscillator, with the PLL bypassed and the DSOSCSRC field of the **Deep-Sleep Clock Configuration (DSLPCLKCFG)** register set to use the internal 12-MHz oscillator, 30-KHz internal oscillator, or 32-KHz external oscillator. When the system is triggered to wake up, the core should wait for the main oscillator to stabilize before starting to execute code. Instead, the core starts executing code while being clocked from the deep-sleep clock source set in the **DSLPCLKCFG** register. When the main oscillator stabilizes, the clock to the core is properly switched to run from the main oscillator.

Workaround:

Run the system off of the main oscillator (MOSC) with the PLL enabled. In this mode, the clocks are switched at the proper time.

If the main oscillator must be used to clock the system without the PLL, a simple wait loop at the beginning of the interrupt handler for the wake-up event should be used to stall the frequency-dependent operation until the main oscillator has stabilized.

Silicon Revision Affected:

A2

2.2 PLL may not function properly at default LDO setting

Description:

In designs that enable and use the PLL module, unstable device behavior may occur with the LDO set at its default of 2.5 volts or below (minimum of 2.25 volts). Designs that do not use the PLL module are not affected.

Workaround:

Prior to enabling the PLL module, it is recommended that the default LDO voltage setting of 2.5 V be adjusted to 2.75 V using the **LDO Power Control (LDOPCTL)** register.

Silicon Revision Affected:

A2

2.3 I/O buffer 5-V tolerance issue

Description:

GPIO buffers are not 5-V tolerant when used in open-drain mode. Pulling up the open-drain pin above 4 V results in high current draw.

Workaround:

When configuring a pin as open drain, limit any pull-up resistor connections to the 3.3-V power rail.

Silicon Revision Affected:

A2

2.4 PLL Runs Fast When Using a 3.6864-MHz Crystal

Description:

If the PLL is enabled, and a 3.6864-MHz crystal is used, the PLL runs 4% fast.

Workaround:

Use a different crystal whose frequency is one of the other allowed crystal frequencies (see the values shown for the XTAL bit in the **RCC** register).

Silicon Revision Affected:

A2

2.5 External reset does not reset the XTAL to PLL Translation (PLLCFG) register

Description:

Performing an external reset (anything but power-on reset) reconfigures the XTAL field in the **Run-Mode Clock Configuration (RCC)** register to the 6 MHz setting, but does not reset the **XTAL to PLL Translation (PLLCFG)** register to the 6 MHz setting.

Consider the following sequence:

1. Performing a power-on reset results in XTAL = 6 MHz and **PLLCFG** = 6 MHz
2. Write an 8 MHz value to the XTAL field results in XTAL = 8 MHz and **PLLCFG** = 8 MHz
3. $\overline{\text{RST}}$ asserted results in XTAL = 6 MHz and **PLLCFG** = 8 MHz

In the last step, **PLLCFG** was not reset to its 6MHz setting. If this step is followed by enabling the PLL to run from an attached 6-MHz crystal, the PLL then operates at 300MHz instead of 400MHz. Subsequently configuring the XTAL field with the 8 MHz setting does not change the setting of **PLLCFG**.

Workaround:

Set XTAL in **PLLCFG** to an incorrect value, and then to the desired value. The second change updates the register correctly. Do not enable the PLL until after the second change.

Silicon Revision Affected:

A2

2.6 Standard R-C network cannot be used on $\overline{\text{RST}}$ to extend POR timing

Description:

The standard R-C network on $\overline{\text{RST}}$ does not work to extend POR timing beyond the 10 ms on-chip POR. Instead of following the standard capacitor charging curve, $\overline{\text{RST}}$ jumps straight to 3 V at power on. The capacitor is fully charged by current out of the $\overline{\text{RST}}$ pin and does not extend or filter the power-on condition. As a result, the reset input is not extended beyond the POR.

Workaround:

Add a diode to block the output current from $\overline{\text{RST}}$. This helps to extend the $\overline{\text{RST}}$ pulse, but also means that the R-C is not as effective as a noise filter.

Silicon Revision Affected:

A2

3 Hibernation Module

3.1 Hibernation module does not operate correctly

Description:

The Hibernation module on this microcontroller does not operate correctly.

Workaround:

This errata item does not apply to many Stellaris devices, including the LM3S1166, LM3S1636, LM3S1969, and LM3S2919. Refer to the Stellaris Product Selector Guide (www.ti.com/stellaris_search) and Errata documents to find an alternative microcontroller that meets the design requirements for your application.

Silicon Revision Affected:

A2

4 Flash Controller

4.1 MERASE bit of the FMC register does not erase the entire Flash array

Description:

The MERASE bit of the **Flash Memory Control (FMC)** register does not erase the entire Flash array. If the contents of the **Flash Memory Address (FMA)** register contain a value less than 0x20000, only the first 128 KB of the Flash array are erased. If bit 17 (value of 0x20000) is set, then only the upper address range of Flash (greater than 128 KB) is erased.

Workaround:

If the entire array must be erased, the following sequence is recommended:

1. Write a value of 0x00000000 to the **FMA** register.
2. Write a value of 0xA4420004 to the **FMC** register, and poll bit 2 until it is cleared.
3. Write a value of 0x00020000 to the **FMA** register.
4. Write a value of 0xA4420004 to the **FMC** register, and poll bit 2 until it is cleared.

The entire array can also be erased by individually erasing all of the pages in the array.

Silicon Revision Affected:

A2

5 GPIO

5.1 GPIO input pin latches in the Low state if pad type is open drain

Description:

GPIO pins function normally if configured as inputs and the open-drain configuration is disabled. If open drain is enabled while the pin is configured as an input using the **GPIO Alternate Function Select (GPIOAFSEL)**, **GPIO Open Drain Select (GPIOODR)**, and **GPIO Direction (GPIODIR)** registers, then the pin latches Low and excessive current (into pin) results if an attempt is made to drive the pin High. The open-drain device is not controllable.

A GPIO pin is not normally configured as open drain and as an input at the same time. A user may want to do this when driving a signal out of a GPIO open-drain pad while configuring the pad as an input to read data on the same pin being driven by an external device. Bit-banging a bidirectional, open-drain bus (for example, I^2C) is an example.

Workaround:

If a user wants to read the state of a GPIO pin on a bidirectional bus that is configured as an open-drain output, the user must first disable the open-drain configuration and then change the direction of the pin to an input. This precaution ensures that the pin is never configured as an input and open drain at the same time.

A second workaround is to use two GPIO pins connected to the same bus signal. The first GPIO pin is configured as an open-drain output, and the second is configured as a standard input. This way the open-drain output can control the state of the signal and the input pin allows the user to read the state of the signal without causing the latch-up condition.

Silicon Revision Affected:

A2

5.2 GPIO pins may glitch during power supply ramp up

Description:

Upon completing a POR (power on reset) sequence, the GPIO pins default to a tri-stated input condition. However, during the initial ramp up of the external V_{DD} supply from 0.0 V to 3.3 V, the GPIO pins are momentarily configured as output drivers during the time the internal LDO circuit is also ramping up. As a result, a signal glitch may occur on GPIO pins before both the external V_{DD} supply and internal LDO voltages reach their normal operating conditions. This situation can occur when the V_{DD} and LDO voltages ramp up at significantly different rates. The LDO voltage ramp-up time is affected by the load capacitance on the LDO pin, therefore, it is important to keep this load at a nominal 1 µF value as recommended in the data sheet. Adding significant more capacitance loading beyond the specification causes the time delay between the two supply ramp-up times to grow, which possibly increases the severity of the glitching behavior.

Workaround:

Ensuring that the V_{DD} power supply ramp up is a fast as possible helps minimize the potential for GPIO glitches. Follow guidelines for LDO pin capacitive loading documented in the electrical section of the data sheet. System designers must ensure that, during the V_{DD} supply ramp-up time, possible GPIO pin glitches can cause no adverse effects to their systems.

Silicon Revision Affected:

A2

6 General-Purpose Timers

6.1 General-purpose timer Edge Count mode count error when timer is disabled

Description:

When a general-purpose timer is configured for 16-Bit Input Edge Count Mode, the timer (A or B) erroneously decrements by one when the Timer Enable (TnEN) bit in the **GPTM Control (GPTMCTL)** register is cleared (the timer is disabled).

Workaround:

When the general-purpose timer is configured for Edge Count mode and software needs to “stop” the timer, the timer should be reloaded with the current count + 1 and restarted.

Silicon Revision Affected:

A2

6.2 General-purpose timer 16-bit Edge Count or Edge Time mode does not load reload value

Description:

In Edge Count or Edge Time mode, the input events on the CCP pin decrement the counter until the count matches what is in the **GPTM Timern Match (GPTMTnMATCHR)** register. At that point, an interrupt is asserted and then the counter should be reloaded with the original value and counting begins again. However, the reload value is not reloaded into the timer.

Workaround:

Rewrite the **GPTM Timern Interval Load (GPTMTnILR)** register before restarting.

Silicon Revision Affected:

A2

6.3 The General-Purpose Timer match register does not function correctly in 32-bit mode

Description:

The **GPTM Timer A Match (GPTMTAMATCHR)** register triggers a match interrupt when the lower 16 bits match, regardless of the value of the upper 16 bits.

Workaround:

None.

Silicon Revision Affected:

A2

7 UART

7.1 The RTRIS bit in the UARTRIS register is only set when the interrupt is enabled

Description:

The RTRIS (UART Receive Time-Out Raw Interrupt Status) bit in the **UART Raw Interrupt Status (UARTRIS)** register should be set when a receive time-out occurs, regardless of the state of the enable RTIM bit in the **UART Interrupt Mask (UARTIM)** register. However, currently the RTIM bit must be set in order for the RTRIS bit to be set when a receive time-out occurs.

Workaround:

For applications that require polled operation, the RTIM bit can be set while the UART interrupt is disabled in the NVIC using the IntDisable(n) function in the StellarisWare Peripheral Driver Library, where n is 21, 22, or 49 depending whether UART0, UART1 or UART2 is used. With this configuration, software can poll the RTRIS bit, but the interrupt is not reported to the NVIC.

Silicon Revision Affected:

A2

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