LOW-VOLTAGE RAIL-TO-RAIL OUTPUT OPERATIONAL AMPLIFIERS

Check for Samples: LMV821 SINGLE, LMV822 DUAL, LMV824 QUAD

FEATURES

- **2.5-V, 2.7-V, and 5-V Performance**
- **–40°C to 125°C Operation**
- **No Crossover Distortion**
- **Low Supply Current at V_{CC+} = 5 V:**
  - **LMV821…0.3 mA Typ**
  - **LMV822…0.5 mA Typ**
  - **LMV824…1 mA Typ**
- **Rail-to-Rail Output Swing**
- **Gain Bandwidth of 5.5 MHz Typ at 5 V**
- **Slew Rate of 1.9 V/µs Typ at 5 V**

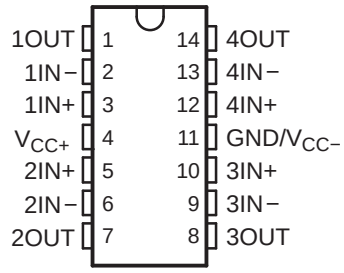
DESCRIPTION/ ORDERING INFORMATION

The LMV821 single, LMV822 dual, and LMV824 quad devices are low-voltage (2.5 V to 5.5 V), low-power commodity operational amplifiers. Electrical characteristics are very similar to the LMV3xx operational amplifiers (low supply current, rail-to-rail outputs, input common-mode range that includes ground). However, the LMV8xx devices offer a higher bandwidth (5.5 MHz typical) and faster slew rate (1.9 V/µs typical).

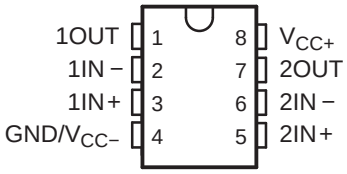
The LMV8xx devices are cost-effective solutions for applications requiring low-voltage/low-power operation and space-saving considerations. The LMV821 is available in the ultra-small DCK package, which is approximately half the size of SOT-23-5. The DCK package saves space on printed circuit boards and enables the design of small portable electronic devices (cordless and cellular phones, laptops, PDAs, PCMIA). It also allows the designer to place the device closer to the signal source to reduce noise pickup and increase signal integrity.

The LMV8xx devices are characterized for operation from –40°C to 85°C. The LMV8xxI devices are characterized for operation from –40°C to 125°C.

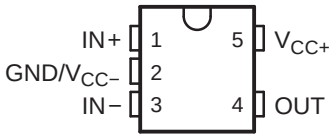
LMV824 . . . D, DGV, OR PW PACKAGE
(TOP VIEW)



LMV822 . . . D OR DGK PACKAGE
(TOP VIEW)



LMV821 . . . DBV OR DCK PACKAGE
(TOP VIEW)



ORDERING INFORMATION

T_A	PACKAGE[1]			ORDERABLE PART NUMBER	TOP-SIDE MARKING[2]
–40°C to 85°C	Single	SC-70 – DCK	Reel of 3000	LMV821DCKR	RY_
			Reel of 250	LMV821DCKT	
		SOT-23 – DBV	Reel of 3000	LMV821DBVR	RB8_
			Reel of 250	LMV821DBVT	
	Dual	SOIC – D	Tube of 75	LMV822D	MV822
			Reel of 2500	LMV822DR	
		MSOP/VSSOP – DGK	Tube of 100	LMV822DGK	RA_
			Reel of 2500	LMV822DGKR	
	Quad	SOIC – D	Tube of 50	LMV824D	LMV824
			Reel of 2500	LMV824DR	
		TSSOP – PW	Tube of 90	LMV824PW	MV824
			Reel of 2000	LMV824PWR	
		TVSOP – DGV	Reel of 2000	LMV824DGVR	MV824
–40°C to 125°C	Single	SC-70 – DCK	Reel of 3000	LMV821IDCKR	RZ_
			Reel of 250	LMV821IDCKT	
		SOT-23 – DBV	Reel of 3000	LMV821IDBVR	RB1_
			Reel of 250	LMV821IDBVT	
	Dual	SOIC – D	Tube of 75	LMV822ID	MV822I
			Reel of 2500	LMV822IDR	
		MSOP/VSSOP – DGK	Tube of 100	LMV822IDGK	R8_
			Reel of 2500	LMV822IDGKR	
	Quad	SOIC – D	Tube of 50	LMV824ID	LMV824I
			Reel of 2500	LMV824IDR	
		TSSOP – PW	Tube of 90	LMV824IPW	MV824I
			Reel of 2000	LMV824IPWR	
		TVSOP – DGV	Reel of 2000	LMV824IDGVR	MV824I

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
(2) DBV/DCK/DGK: The actual top-side marking has one additional character that designates the assembly/test site.

Figure 1. SYMBOL (EACH AMPLIFIER)

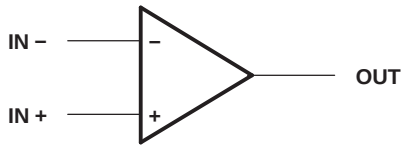
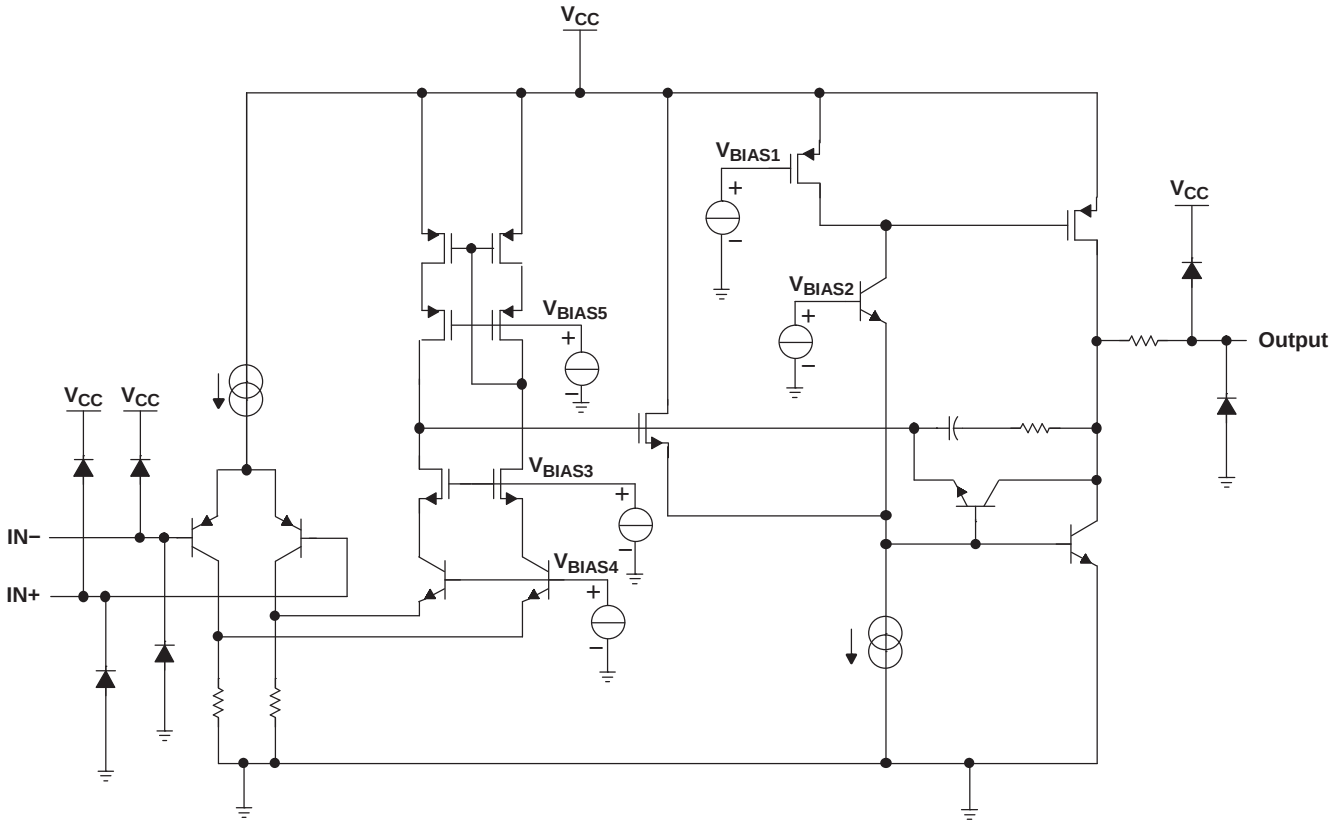


Figure 2. LMV824 SIMPLIFIED SCHEMATIC



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

				MIN	MAX	UNIT
V_{CC}	Supply voltage(2)				5.5	V
V_{ID}	Differential input voltage(3)				$\pm V_{CC}$	V
V_I	Input voltage range (either input)			V_{CC-}	V_{CC+}	V
	Duration of output short circuit (one amplifier) to ground(4)	At or below T_A = 25°C, $V_{CC} \le$ 5.5 V			Unlimited	
θ_{JA}	Package thermal impedance(5) (6)	D package	8 pin		97	°C/W
			14 pin		86	
		DBV package			206	
		DCK package			252	
		DGK package			172	
		DGV package			127	
		PW package			113	
T_J	Operating virtual junction temperature				150	°C
T_{stg}	Storage temperature range			–65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values (except differential voltages and V_{CC} specified for the measurement of I_{OS}) are with respect to the network GND.
(3) Differential voltages are at IN+ with respect to IN–.
(4) Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.
(5) Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(6) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage (single-supply operation)		2.5	5	V
T_A	Operating free-air temperature	LMV8xxI	–40	125	°C
		LMV8xx	–40	85	

LMV8xx 2.5-V Electrical Characteristics

V_{CC+} = 2.5 V, V_{CC-} = 0 V, V_{IC} = 1 V, V_O = 1.25 V, and R_L > 1 MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	LMV8xx			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage			25°C		1	3.5	mV
				–40°C to 85°C			4	
V_O	Output swing	V_{CC+} = 2.5 V, R_L = 600 Ω to 1.25 V	High level	25°C	2.3	2.37		V
				–40°C to 85°C	2.2			
			Low level	25°C		0.13	0.2	
				–40°C to 85°C			0.3	
		V_{CC+} = 2.5 V, R_L = 2 kΩ to 1.25 V	High level	25°C	2.4	2.46		
				–40°C to 85°C	2.3			
			Low level	25°C		0.08	0.12	
				–40°C to 85°C			0.2	

LMV8xxI 2.5-V Electrical Characteristics

V_{CC+} = 2.5 V, V_{CC-} = 0 V, V_{IC} = 1 V, V_O = 1.25 V, and R_L > 1 MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	LMV8xxI			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage			25°C		1	3.5	mV
				–40°C to 125°C			5.5	
V_O	Output swing	V_{CC+} = 2.5 V, R_L = 600 Ω to 1.25 V	High level	25°C	2.28	2.37		V
				–40°C to 125°C	2.18			
			Low level	25°C		0.13	0.22	
				–40°C to 125°C			0.32	
		V_{CC+} = 2.5 V, R_L = 2 kΩ to 1.25 V	High level	25°C	2.38	2.46		
				–40°C to 125°C	2.28			
			Low level	25°C		0.08	0.14	
				–40°C to 125°C			0.22	

LMV8xx 2.7-V Electrical Characteristics

V_{CC+} = 2.7 V, V_{CC-} = 0 V, V_{IC} = 1 V, V_O = 1.35 V, and R_L > 1 MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	LMV8xx			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage			25°C		1	3.5	mV
				–40°C to 85°C			4	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C		1		µV/°C
I_{IB}	Input bias current			25°C		30	90	nA
				–40°C to 85°C			140	
I_{IO}	Input offset current			25°C		0.5	30	nA
				–40°C to 85°C			50	
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 1.7 V		25°C	70	85		dB
				–40°C to 85°C	68			
$+k_{SVR}$	Positive supply-voltage rejection ratio	V_{CC+} = 1.7 V to 4 V, V_{CC-} = –1 V, V_O = 0, V_{IC} = 0		25°C	75	85		dB
				–40°C to 85°C	70			
$–k_{SVR}$	Negative supply-voltage rejection ratio	V_{CC+} = 1.7 V, V_{CC-} = –1 V to –3.3 V, V_O = 0, V_{IC} = 0		25°C	73	85		dB
				–40°C to 85°C	70			
V_{ICR}	Common-mode input voltage range	CMRR ≥ 50 dB		25°C	–0.2 to 1.9	–0.3 to 2		V
A_V	Large-signal voltage amplification	R_L = 600 Ω to 1.35 V, V_O = 1.35 V to 2.2 V	Sourcing	25°C	90	100		dB
				–40°C to 85°C	85			
		R_L = 600 Ω to 1.35 V, V_O = 1.35 V to 0.5 V	Sinking	25°C	85	90		
				–40°C to 85°C	80			
		R_L = 2 kΩ to 1.35 V, V_O = 1.35 V to 2.2 V	Sourcing	25°C	95	100		
				–40°C to 85°C	90			
		R_L = 2 kΩ to 1.35 V, V_O = 1.35 V to 0.5 V	Sinking	25°C	90	95		
				–40°C to 85°C	85			
V_O	Output swing	V_{CC+} = 2.7 V, R_L = 600 Ω to 1.35 V	High level	25°C	2.5	2.58		V
				–40°C to 85°C	2.4			
			Low level	25°C		0.13	0.2	
				–40°C to 85°C			0.3	
		V_{CC+} = 2.7 V, R_L = 2 kΩ to 1.35 V	High level	25°C	2.6	2.66		
				–40°C to 85°C	2.5			
			Low level	25°C		0.08	0.12	
				–40°C to 85°C			0.2	
I_O	Output current	V_O = 0 V	Sourcing	25°C	12	16		mA
		V_O = 2.7 V	Sinking	25°C	12	26		
I_{CC}	Supply current	LMV821		25°C		0.22	0.3	mA
				–40°C to 85°C			0.5	
		LMV822 (both amplifiers)		25°C		0.45	0.6	
				–40°C to 85°C			0.8	
		LMV824 (all four amplifiers)		25°C		0.72	1	
				–40°C to 85°C			1.2	

LMV8xx 2.7-V Electrical Characteristics (continued)

V_{CC+} = 2.7 V, $V_{CC–}$ = 0 V, V_{IC} = 1 V, V_O = 1.35 V, and R_L > 1 MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	LMV8xx			UNIT
				MIN	TYP	MAX	
SR	Slew rate(1)		25°C		1.7		V/μs
GBW	Gain bandwidth product	(2)	25°C		5		MHz
Φ_m	Phase margin	(2)	25°C		60		deg
	Gain margin	(2)	25°C		8.6		dB
	Amplifier-to-amplifier isolation	V_{CC+} = 5 V, R_L = 100 kΩ to 2.5 V(3)	25°C		135		dB
V_n	Equivalent input noise voltage	f = 1 kHz, V_{IC} = 1 V	25°C		45		nV/√Hz
I_n	Equivalent input noise current	f = 1 kHz	25°C		0.18		pA/√Hz
THD	Total harmonic distortion	f = 1 kHz, A_V = –2, R_L = 10 kΩ, V_O = 4.1 V_{p-p}	25°C		0.01		%

(1) Connected as voltage follower with 1-V step input. Value specified is the slower of the positive and negative slew rates.
(2) 40-dB closed-loop dc gain, C_L = 22 pF
(3) Each amplifier excited in turn with 1 kHz to produce V_O = 3 V_{p-p}

LMV8xxI 2.7-V Electrical Characteristics

V_{CC+} = 2.7 V, V_{CC-} = 0 V, V_{IC} = 1 V, V_O = 1.35 V, and R_L > 1 MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	LMV8xxI			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage			25°C		1	3.5	mV
				–40°C to 125°C			5.5	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C		1		µV/°C
I_{IB}	Input bias current			25°C		30	90	nA
				–40°C to 125°C			140	
I_{IO}	Input offset current			25°C		0.5	30	nA
				–40°C to 125°C			50	
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 1.7 V		25°C	70	85		dB
				–40°C to 125°C	68			
$+k_{SVR}$	Positive supply-voltage rejection ratio	V_{CC+} = 1.7 V to 4 V, V_{CC-} = –1 V, V_O = 0, V_{IC} = 0		25°C	75	85		dB
				–40°C to 125°C	70			
$–k_{SVR}$	Negative supply-voltage rejection ratio	V_{CC+} = 1.7 V, V_{CC-} = –1 V to –3.3 V, V_O = 0, V_{IC} = 0		25°C	73	85		dB
				–40°C to 125°C	70			
V_{ICR}	Common-mode input voltage range	CMRR ≥ 50 dB		25°C	–0.2 to 1.9	–0.3 to 2		V
A_V	Large-signal voltage amplification	R_L = 600 Ω to 1.35 V, V_O = 1.35 V to 2.2 V	Sourcing	25°C	90	100		dB
				–40°C to 125°C	85			
		R_L = 600 Ω to 1.35 V, V_O = 1.35 V to 0.5 V	Sinking	25°C	85	90		
				–40°C to 125°C	80			
		R_L = 2 kΩ to 1.35 V, V_O = 1.35 V to 2.2 V	Sourcing	25°C	95	100		
				–40°C to 125°C	90			
		R_L = 2 kΩ to 1.35 V, V_O = 1.35 V to 0.5 V	Sinking	25°C	90	95		
				–40°C to 125°C	85			
V_O	Output swing	V_{CC+} = 2.7 V, R_L = 600 Ω to 1.35 V	High level	25°C	2.5	2.58		V
				–40°C to 125°C	2.4			
			Low level	25°C		0.13	0.2	
				–40°C to 125°C			0.3	
		V_{CC+} = 2.7 V, R_L = 2 kΩ to 1.35 V	High level	25°C	2.6	2.66		
				–40°C to 125°C	2.5			
			Low level	25°C		0.08	0.12	
				–40°C to 125°C			0.2	
I_O	Output current	V_O = 0 V	Sourcing	25°C	12	16		mA
		V_O = 2.7 V	Sinking	25°C	12	26		
I_{CC}	Supply current	LMV821		25°C		0.22	0.3	mA
				–40°C to 125°C			0.5	
		LMV822 (both amplifiers)		25°C		0.45	0.6	
				–40°C to 125°C			0.8	
		LMV824 (all four amplifiers)		25°C		0.72	1	
				–40°C to 125°C			1.2	

LMV8xxI 2.7-V Electrical Characteristics (continued)

V_{CC+} = 2.7 V, V_{CC-} = 0 V, V_{IC} = 1 V, V_O = 1.35 V, and R_L > 1 MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	LMV8xxI			UNIT
				MIN	TYP	MAX	
SR	Slew rate(1)		25°C		1.7		V/µs
GBW	Gain bandwidth product	(2)	25°C		5		MHz
Φ_m	Phase margin	(2)	25°C		60		deg
	Gain margin	(2)	25°C		8.6		dB
	Amplifier-to-amplifier isolation	V_{CC+} = 5 V, R_L = 100 kΩ to 2.5 V(3)	25°C		135		dB
V_n	Equivalent input noise voltage	f = 1 kHz, V_{IC} = 1 V	25°C		45		nV/√Hz
I_n	Equivalent input noise current	f = 1 kHz	25°C		0.18		pA/√Hz
THD	Total harmonic distortion	f = 1 kHz, A_V = –2, R_L = 10 kΩ, V_O = 4.1 V_{p-p}	25°C		0.01		%

(1) Connected as voltage follower with 1-V step input. Value specified is the slower of the positive and negative slew rates.
(2) 40-dB closed-loop dc gain, C_L = 22 pF
(3) Each amplifier excited in turn with 1 kHz to produce V_O = 3 V_{p-p}

LMV8xx 5-V Electrical Characteristics

V_{CC+} = 5 V, V_{CC-} = 0 V, V_{IC} = 2 V, V_O = 2.5 V, and R_L > 1 MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	LMV8xx			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage			25°C		1	3.5	mV
				–40°C to 85°C			4	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C		1		µV/°C
I_{IB}	Input bias current			25°C		40	100	nA
				–40°C to 85°C			150	
I_{IO}	Input offset current			25°C		0.5	30	nA
				–40°C to 85°C			50	
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 4 V		25°C	72	90		dB
				–40°C to 85°C	70			
$+k_{SVR}$	Positive supply-voltage rejection ratio	V_{CC+} = 1.7 V to 4 V, V_{CC-} = –1 V, V_O = 0, V_{IC} = 0		25°C	75	85		dB
				–40°C to 85°C	70			
$–k_{SVR}$	Negative supply-voltage rejection ratio	V_{CC+} = 1.7 V, V_{CC-} = –1 V to –3.3 V, V_O = 0, V_{IC} = 0		25°C	73	85		dB
				–40°C to 85°C	70			
V_{ICR}	Common-mode input voltage range	CMRR ≥ 50 dB		25°C	–0.2 to 4.2	–0.3 to 4.3		V
A_V	Large-signal voltage amplification	R_L = 600 Ω to 2.5 V, V_O = 2.5 V to 4.5 V	Sourcing	25°C	95	105		dB
				–40°C to 85°C	90			
		R_L = 600 Ω to 2.5 V, V_O = 2.5 V to 0.5 V	Sinking	25°C	95	105		
				–40°C to 85°C	90			
		R_L = 2 kΩ to 2.5 V, V_O = 2.5 V to 4.5 V	Sourcing	25°C	95	105		
				–40°C to 85°C	90			
		R_L = 2 kΩ to 2.5 V, V_O = 2.5 V to 0.5 V	Sinking	25°C	95	105		
				–40°C to 85°C	90			
V_O	Output swing	V_{CC+} = 5 V, R_L = 600 Ω to 2.5 V	High level	25°C	4.75	4.84		V
				–40°C to 85°C	4.7			
			Low level	25°C		0.17	0.25	
				–40°C to 85°C			0.3	
		V_{CC+} = 5 V, R_L = 2 kΩ to 2.5 V	High level	25°C	4.85	4.9		
				–40°C to 85°C	4.8			
			Low level	25°C		0.1	0.15	
				–40°C to 85°C			0.2	
I_O	Output current	V_O = 0 V	Sourcing	25°C	20	45		mA
				–40°C to 85°C	15			
		V_O = 5 V	Sinking	25°C	20	40		
				–40°C to 85°C	15			
I_{CC}	Supply current	LMV821		25°C		0.3	0.4	mA
				–40°C to 85°C			0.6	
		LMV822 (both amplifiers)		25°C		0.5	0.7	
				–40°C to 85°C			0.9	
		LMV824 (all four amplifiers)		25°C		1	1.3	
				–40°C to 85°C			1.5	

LMV8xx 5-V Electrical Characteristics (continued)

V_{CC+} = 5 V, V_{CC-} = 0 V, V_{IC} = 2 V, V_O = 2.5 V, and R_L > 1 MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	LMV8xx			UNIT
				MIN	TYP	MAX	
SR	Slew rate	V_{CC+} = 5 V (1)	25°C	1.4	1.9		V/µs
GBW	Gain bandwidth product	(2)	25°C		5.5		MHz
Φ_m	Phase margin	(2)	25°C		64.2		deg
	Gain margin	(2)	25°C		8.7		dB
	Amplifier-to-amplifier isolation	V_{CC+} = 5 V, R_L = 100 kΩ to 2.5 V (3)	25°C		135		dB
V_n	Equivalent input noise voltage	f = 1 kHz, V_{IC} = 1 V	25°C		42		nV/√Hz
I_n	Equivalent input noise current	f = 1 kHz	25°C		0.2		pA/√Hz
THD	Total harmonic distortion	f = 1 kHz, A_V = –2, R_L = 10 kΩ, V_O = 4.1 V_{p-p}	25°C		0.01		%

(1) Connected as voltage follower with 3-V step input. Value specified is the slower of the positive and negative slew rates.
(2) 40-dB closed-loop dc gain, C_L = 22 pF
(3) Each amplifier excited in turn with 1 kHz to produce V_O = 3 V_{p-p}

LMV8xxI 5-V Electrical Characteristics

V_{CC+} = 5 V, V_{CC-} = 0 V, V_{IC} = 2 V, V_O = 2.5 V, and R_L > 1 MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	LMV8xxI			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage			25°C		1	3.5	mV
				–40°C to 125°C			5.5	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C		1		µV/°C
I_{IB}	Input bias current			25°C		40	100	nA
				–40°C to 125°C			150	
I_{IO}	Input offset current			25°C		0.5	30	nA
				–40°C to 125°C			50	
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 4 V		25°C	72	90		dB
				–40°C to 125°C	70			
$+k_{SVR}$	Positive supply-voltage rejection ratio	V_{CC+} = 1.7 V to 4 V, V_{CC-} = –1 V, V_O = 0, V_{IC} = 0		25°C	75	85		dB
				–40°C to 125°C	70			
$–k_{SVR}$	Negative supply-voltage rejection ratio	V_{CC+} = 1.7 V, V_{CC-} = –1 V to –3.3 V, V_O = 0, V_{IC} = 0		25°C	73	85		dB
				–40°C to 125°C	70			
V_{ICR}	Common-mode input voltage range	CMRR ≥ 50 dB		25°C	–0.2 to 4.2	–0.3 to 4.3		V
A_V	Large-signal voltage amplification	R_L = 600 Ω to 2.5 V, V_O = 2.5 V to 4.5 V	Sourcing	25°C	95	105		dB
				–40°C to 125°C	90			
		R_L = 600 Ω to 2.5 V, V_O = 2.5 V to 0.5 V	Sinking	25°C	95	105		
				–40°C to 125°C	90			
		R_L = 2 kΩ to 2.5 V, V_O = 2.5 V to 4.5 V	Sourcing	25°C	95	105		
				–40°C to 125°C	90			
		R_L = 2 kΩ to 2.5 V, V_O = 2.5 V to 0.5 V	Sinking	25°C	95	105		
				–40°C to 125°C	90			
V_O	Output swing	V_{CC+} = 5 V, R_L = 600 Ω to 2.5 V	High level	25°C	4.75	4.84		V
				–40°C to 125°C	4.6			
			Low level	25°C		0.17	0.25	
				–40°C to 125°C			0.3	
		V_{CC+} = 5 V, R_L = 2 kΩ to 2.5 V	High level	25°C	4.85	4.9		
				–40°C to 125°C	4.8			
			Low level	25°C		0.1	0.15	
				–40°C to 125°C			0.2	
I_O	Output current	V_O = 0 V	Sourcing	25°C	20	45		mA
				–40°C to 125°C	15			
		V_O = 5 V	Sinking	25°C	20	40		
				–40°C to 125°C	15			
I_{CC}	Supply current	LMV821		25°C		0.3	0.4	mA
				–40°C to 125°C			0.6	
		LMV822 (both amplifiers)		25°C		0.5	0.7	
				–40°C to 125°C			0.9	
		LMV824 (all four amplifiers)		25°C		1	1.3	
				–40°C to 125°C			1.5	

LMV8xxI 5-V Electrical Characteristics (continued)

V_{CC+} = 5 V, V_{CC-} = 0 V, V_{IC} = 2 V, V_O = 2.5 V, and R_L > 1 MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	LMV8xxI			UNIT
				MIN	TYP	MAX	
SR	Slew rate	V_{CC+} = 5 V (1)	25°C	1.4	1.9		V/µs
GBW	Gain bandwidth product	(2)	25°C		5.5		MHz
Φ_m	Phase margin	(2)	25°C		64.2		deg
	Gain margin	(2)	25°C		8.7		dB
	Amplifier-to-amplifier isolation	V_{CC+} = 5 V, R_L = 100 kΩ to 2.5 V (3)	25°C		135		dB
V_n	Equivalent input noise voltage	f = 1 kHz, V_{IC} = 1 V	25°C		42		nV/√Hz
I_n	Equivalent input noise current	f = 1 kHz	25°C		0.2		pA/√Hz
THD	Total harmonic distortion	f = 1 kHz, A_V = –2, R_L = 10 kΩ, V_O = 4.1 V_{p-p}	25°C		0.01		%

(1) Connected as voltage follower with 3-V step input. Value specified is the slower of the positive and negative slew rates.
(2) 40-dB closed-loop dc gain, C_L = 22 pF
(3) Each amplifier excited in turn with 1 kHz to produce V_O = 3 V_{p-p}

TYPICAL CHARACTERISTICS

T_A = 25°C, V_{CC+} = 5-V Single Supply (Unless Otherwise Noted)

SUPPLY CURRENT vs SUPPLY VOLTAGE

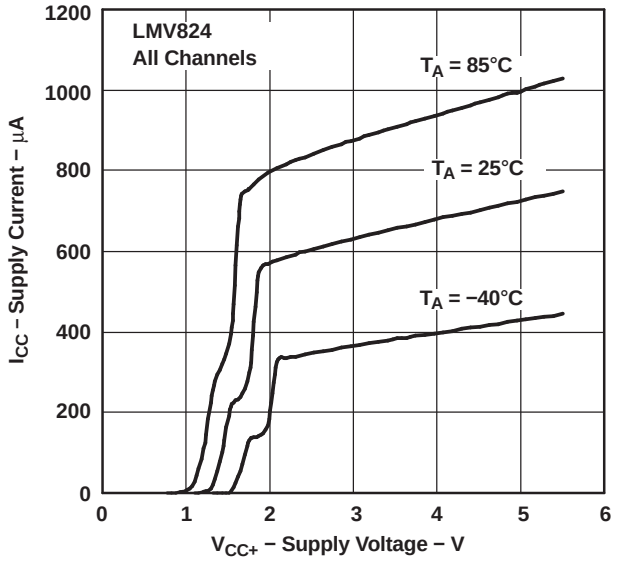


Figure 3.

INPUT CURRENT vs TEMPERATURE

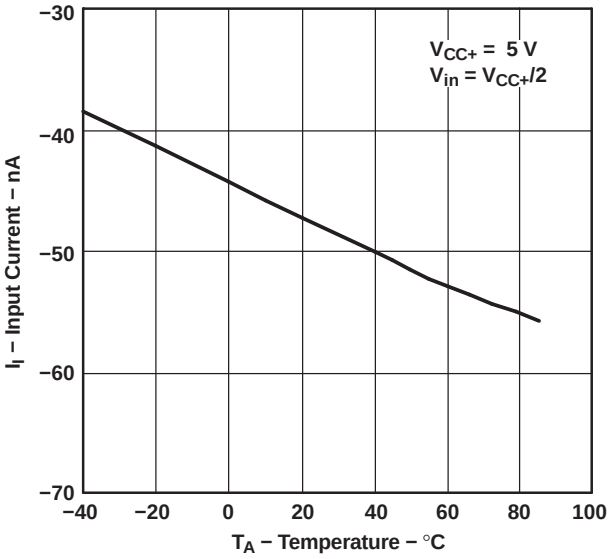


Figure 4.

SOURCING CURRENT vs OUTPUT VOLTAGE

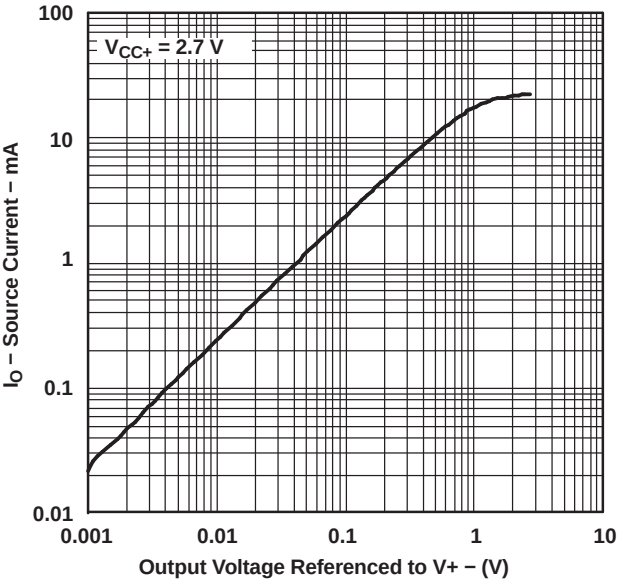


Figure 5.

SOURCING CURRENT vs OUTPUT VOLTAGE

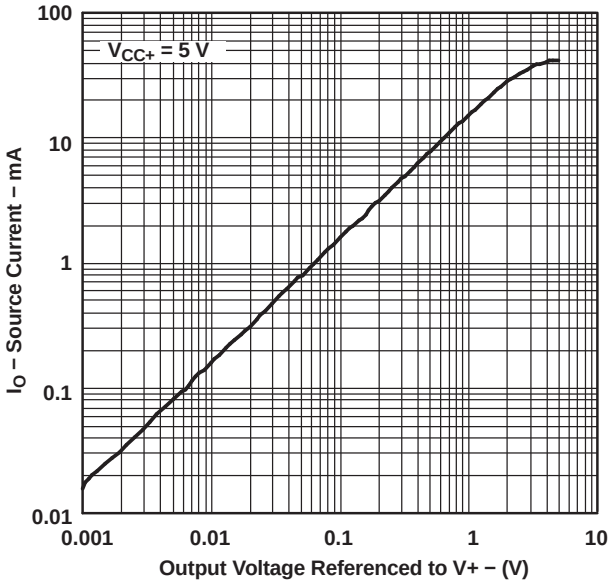


Figure 6.

TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, V_{CC+} = 5-V Single Supply (Unless Otherwise Noted)

SINKING CURRENT vs OUTPUT VOLTAGE

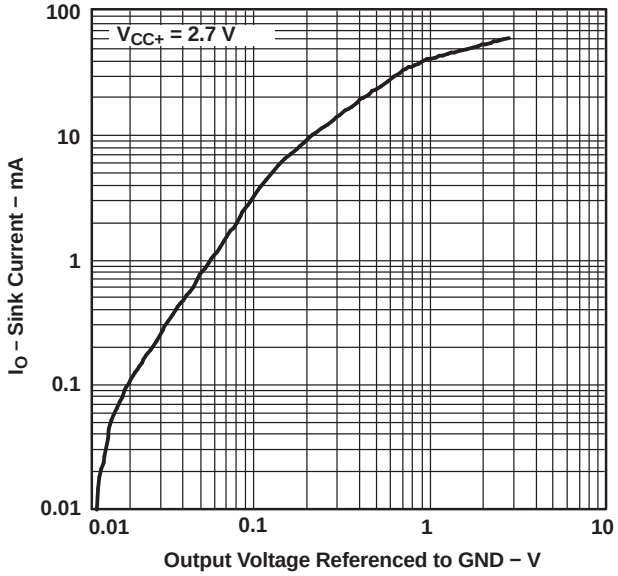


Figure 7.

SINKING CURRENT vs OUTPUT VOLTAGE

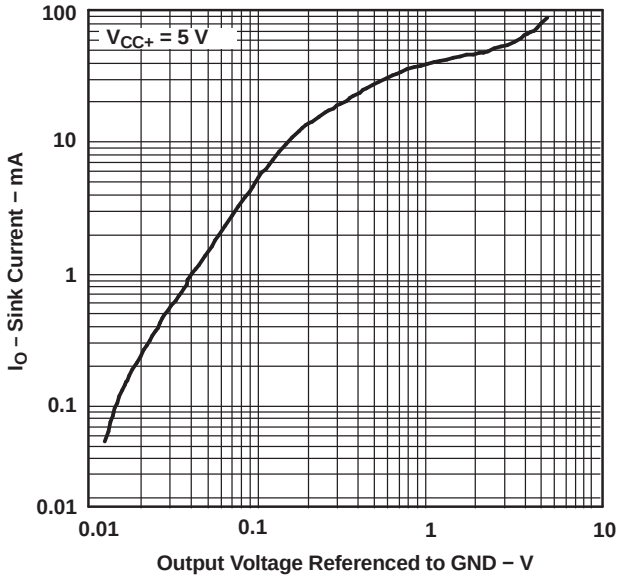


Figure 8.

OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE

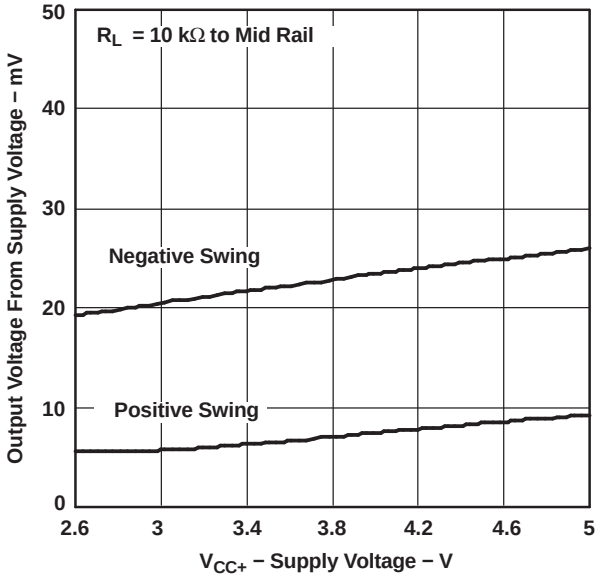


Figure 9.

OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE

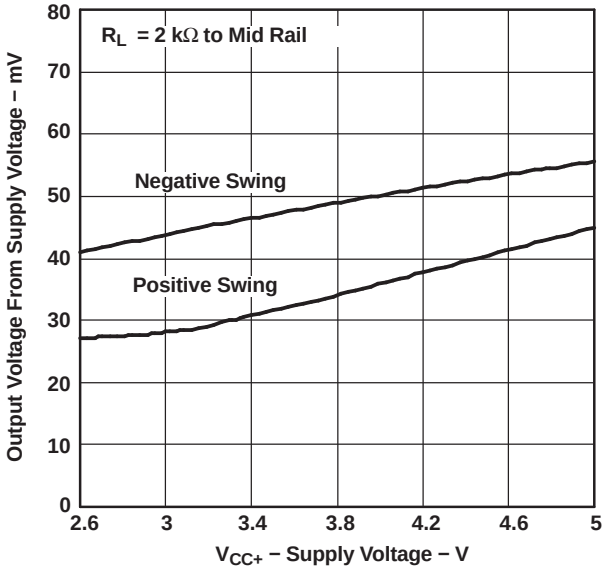


Figure 10.

TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, V_{CC+} = 5-V Single Supply (Unless Otherwise Noted)

OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE

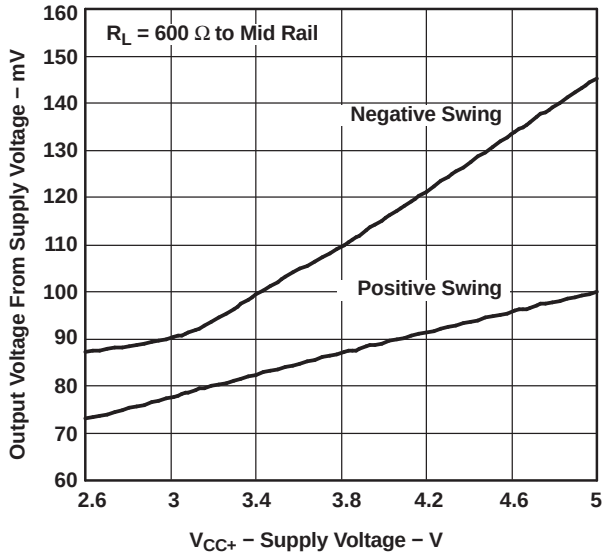


Figure 11.

OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

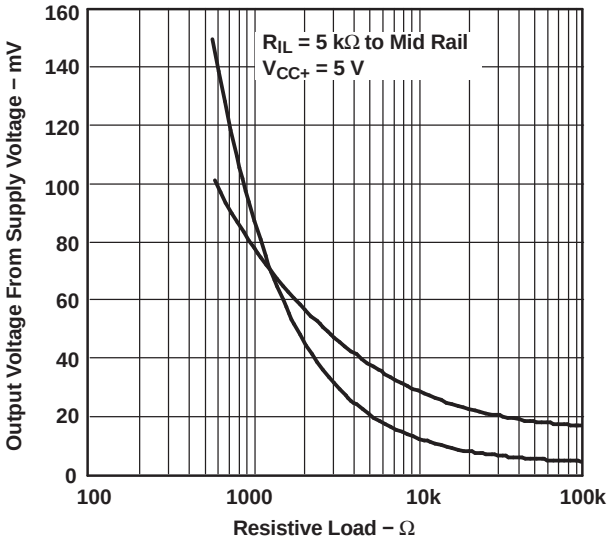


Figure 12.

CROSSTALK REJECTION vs FREQUENCY

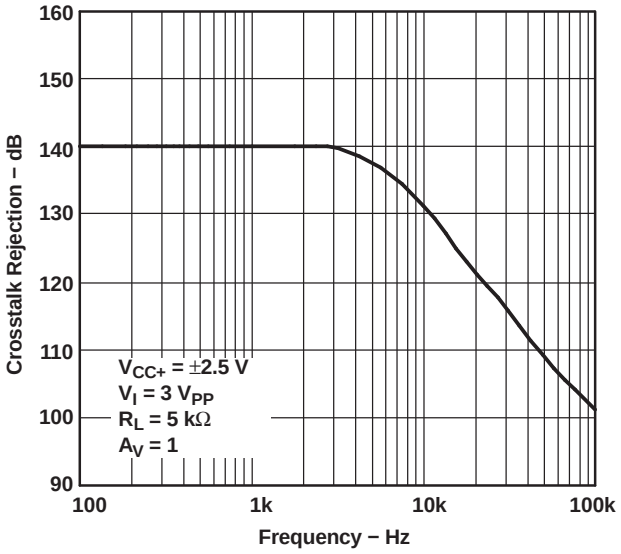


Figure 13.

+PSRR vs FREQUENCY

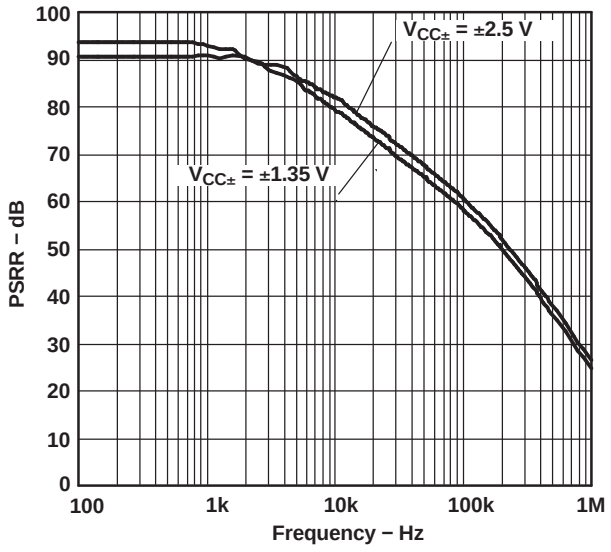


Figure 14.

TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, V_{CC+} = 5-V Single Supply (Unless Otherwise Noted)

–PSRR vs FREQUENCY

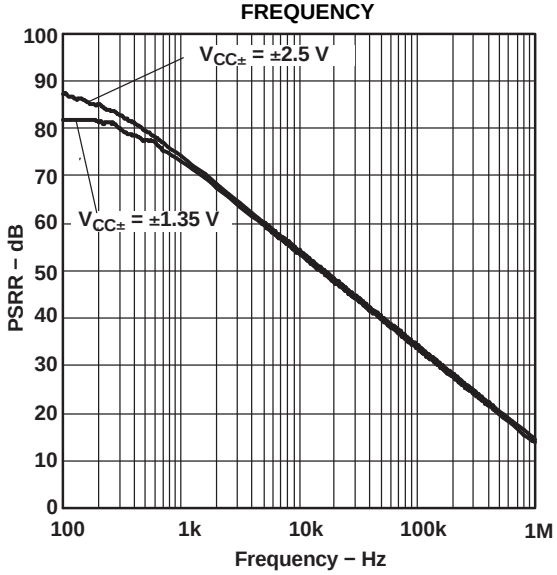


Figure 15.

GAIN AND PHASE MARGIN vs FREQUENCY (V_{CC+} = 2.7 V, R_L = 600 Ω, 2 kΩ, 100 kΩ)

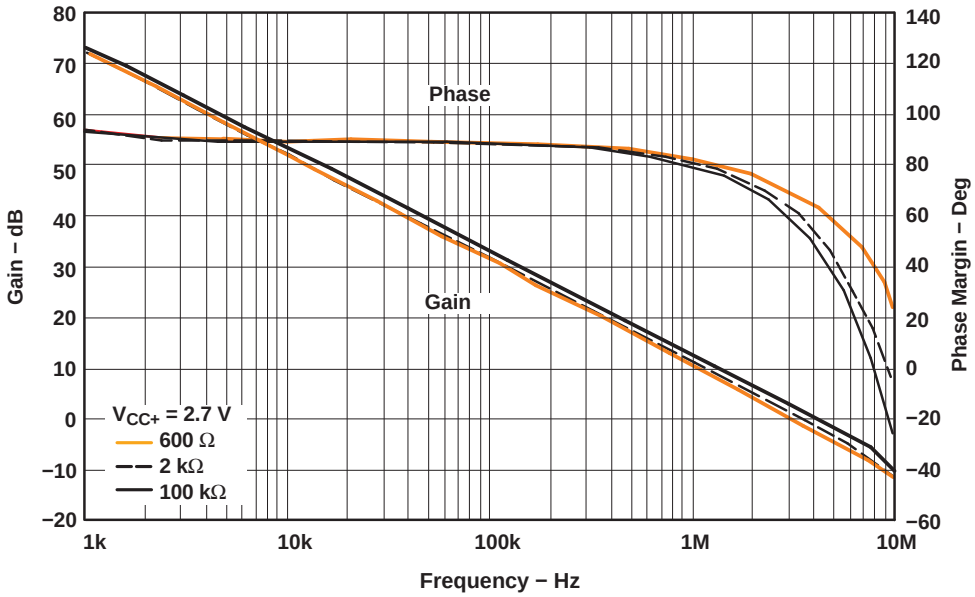


Figure 16.

TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, V_{CC+} = 5-V Single Supply (Unless Otherwise Noted)

GAIN AND PHASE MARGIN vs FREQUENCY (V_{CC+} = 5 V, R_L = 600 Ω, 2 kΩ, 100 kΩ)

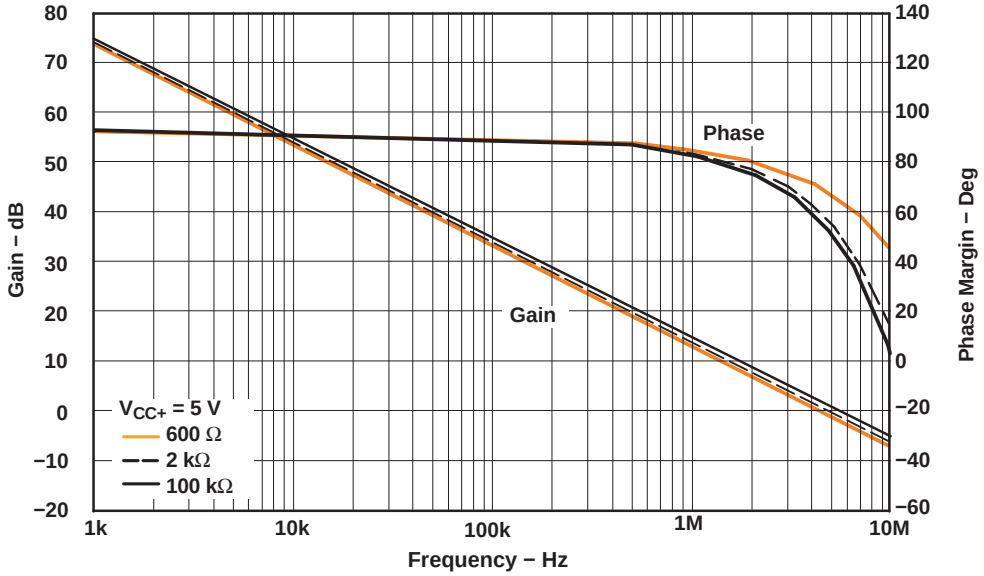


Figure 17.

GAIN AND PHASE MARGIN vs FREQUENCY (V_{CC+} = 2.7 V, R_L = 10 kΩ, C_L = 22 pF, 100 pF, 200 pF)

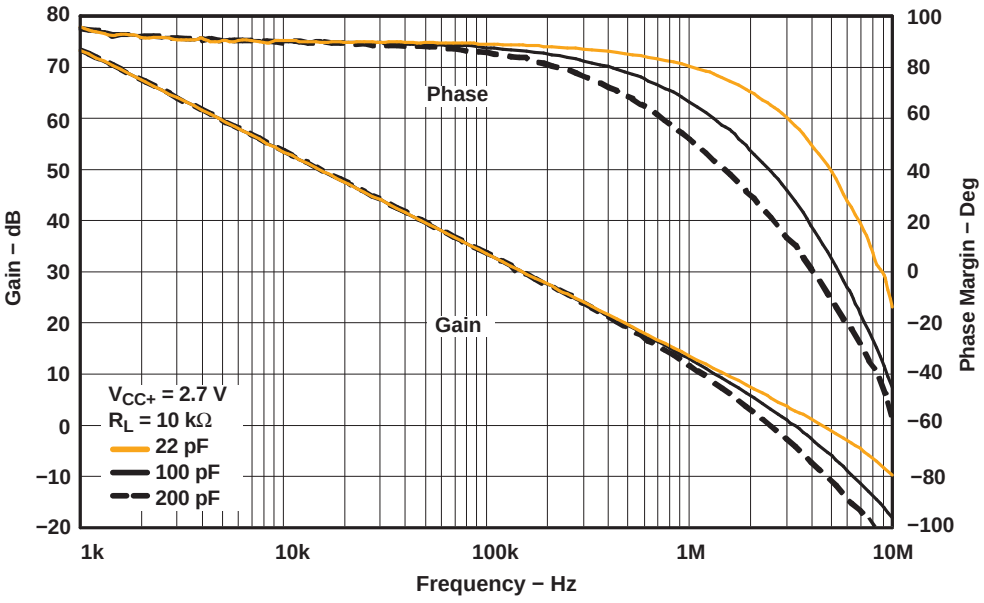


Figure 18.

TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, V_{CC+} = 5-V Single Supply (Unless Otherwise Noted)

GAIN AND PHASE MARGIN vs FREQUENCY (V_{CC+} = 5 V, R_L = 10 kΩ, C_L = 22 pF, 100 pF, 200 pF)

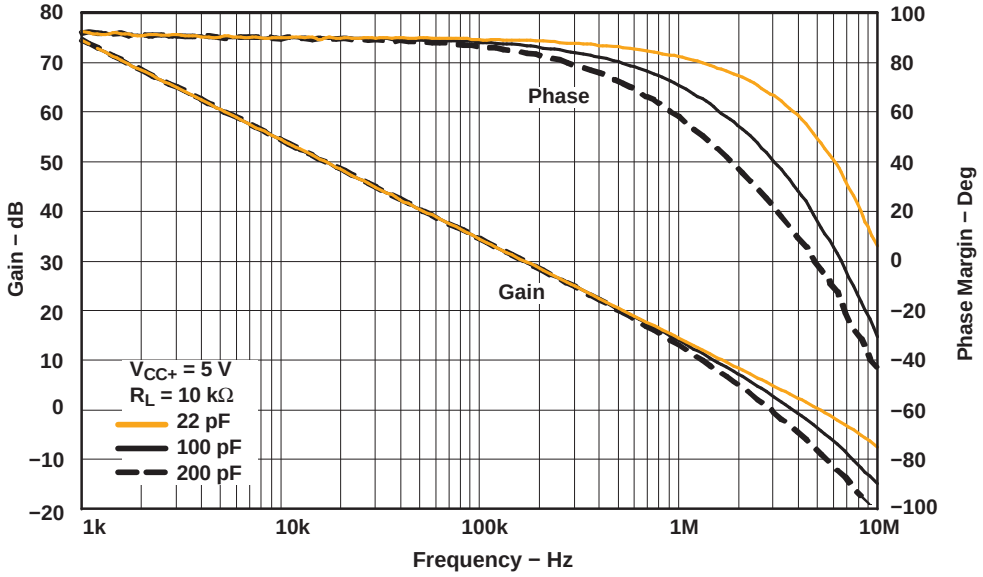


Figure 19.

GAIN AND PHASE MARGIN vs FREQUENCY (V_{CC+} = 2.7 V, R_L = 600 Ω, C_L = 22 pF, 100 pF, 200 pF)

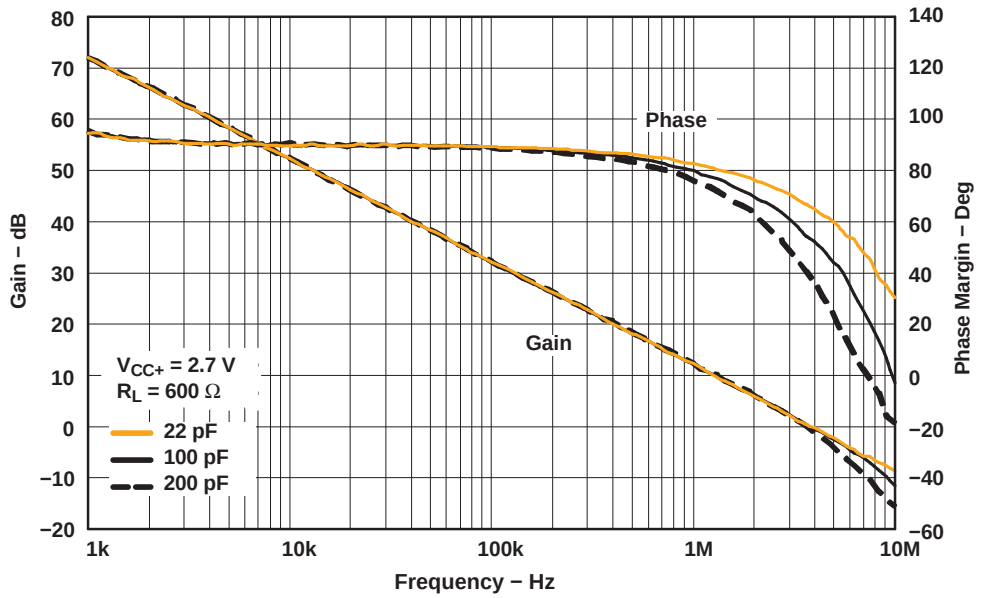


Figure 20.

TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, V_{CC+} = 5-V Single Supply (Unless Otherwise Noted)

GAIN AND PHASE MARGIN vs FREQUENCY (V_{CC+} = 5 V, R_L = 600 Ω, C_L = 22 pF, 100 pF, 200 pF)

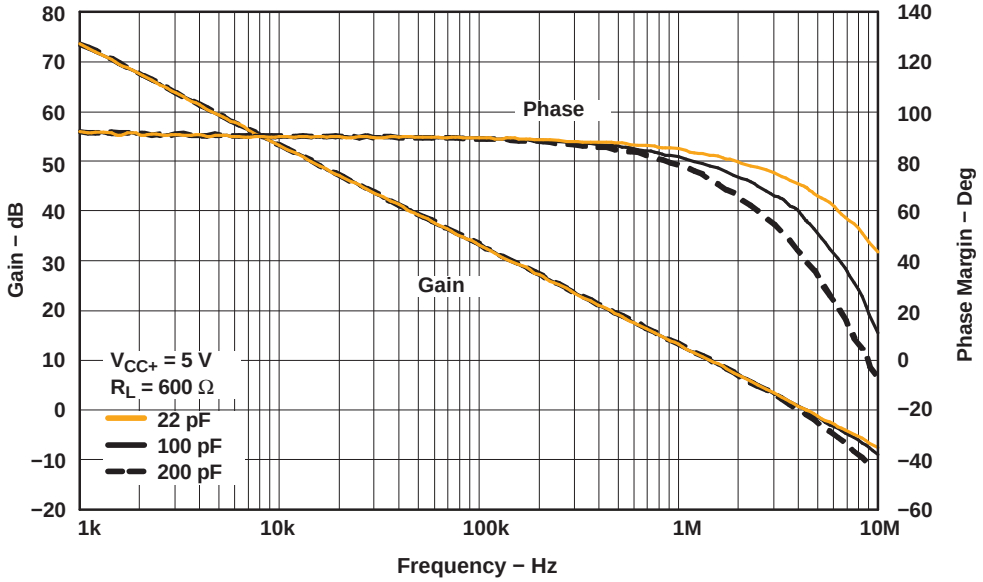


Figure 21.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
LMV821DBVR	NRND	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV821DBVRE4	NRND	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV821DBVRG4	NRND	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV821DBVT	NRND	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV821DBVTE4	NRND	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV821DBVTG4	NRND	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV821DCKR	NRND	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV821DCKRE4	NRND	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV821DCKRG4	NRND	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV821DCKT	NRND	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV821DCKTE4	NRND	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV821DCKTG4	NRND	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV821IDBVR	NRND	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV821IDBVRE4	NRND	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV821IDBVRG4	NRND	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV821IDBVT	NRND	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV821IDBVTE4	NRND	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
LMV821IDBVTG4	NRND	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV821IDCKR	NRND	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV821IDCKRE4	NRND	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV821IDCKRG4	NRND	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV821IDCKT	NRND	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV821IDCKTE4	NRND	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV821IDCKTG4	NRND	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV822D	NRND	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV822DE4	NRND	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV822DG4	NRND	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV822DGKR	NRND	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV822DGKRG4	NRND	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV822DR	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV822DRE4	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV822DRG4	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV822ID	NRND	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV822IDE4	NRND	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV822IDG4	NRND	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
LMV822IDGKR	NRND	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV822IDGKRG4	NRND	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV822IDR	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV822IDRE4	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV822IDRG4	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV824D	NRND	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV824DE4	NRND	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV824DG4	NRND	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV824DGVR	NRND	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV824DGVRE4	NRND	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV824DGVRG4	NRND	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV824DR	NRND	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV824DRE4	NRND	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV824DRG4	NRND	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV824ID	NRND	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV824IDE4	NRND	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV824IDG4	NRND	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV824IDGVR	NRND	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
LMV824IDGVRE4	NRND	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV824IDGVRG4	NRND	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV824IDR	NRND	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV824IDRE4	NRND	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV824IDRG4	NRND	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV824IPW	NRND	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV824IPWE4	NRND	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV824IPWG4	NRND	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV824IPWR	NRND	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV824IPWRE4	NRND	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV824IPWRG4	NRND	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV824PW	NRND	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV824PWE4	NRND	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV824PWG4	NRND	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV824PWR	NRND	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV824PWRE4	NRND	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV824PWRG4	NRND	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

OTHER QUALIFIED VERSIONS OF LMV821, LMV822, LMV824 :

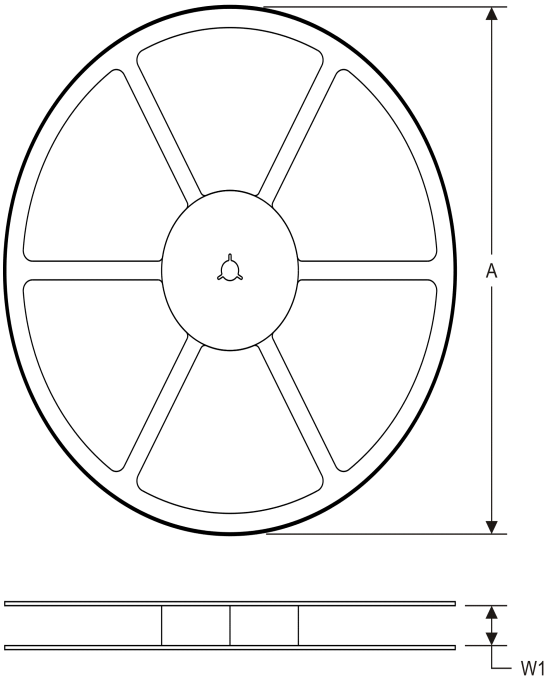
- Automotive: LMV821-Q1, LMV822-Q1, LMV824-Q1

NOTE: Qualified Version Definitions:

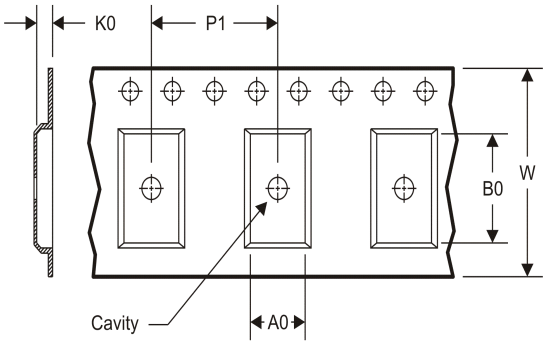
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

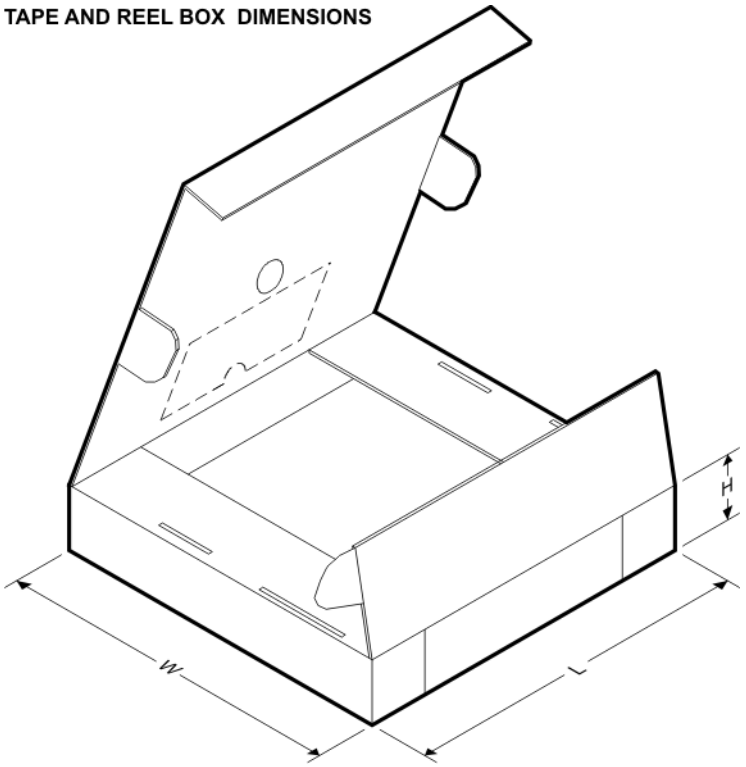
TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV821DBVR	SOT-23	DBV	5	3000	180.0	9.2	3.17	3.23	1.37	4.0	8.0	Q3
LMV821DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
LMV821DBVT	SOT-23	DBV	5	250	180.0	9.2	3.17	3.23	1.37	4.0	8.0	Q3
LMV821DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
LMV821DCKR	SC70	DCK	5	3000	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
LMV821DCKR	SC70	DCK	5	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
LMV821DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
LMV821DCKT	SC70	DCK	5	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
LMV821IDBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV821IDBVT	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV821IDCKR	SC70	DCK	5	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
LMV821IDCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
LMV821IDCKT	SC70	DCK	5	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
LMV822DGKR	MSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV822DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LMV822IDGKR	MSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV822IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LMV824DGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV824DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LMV824IDGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
LMV824IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LMV824IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LMV824PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



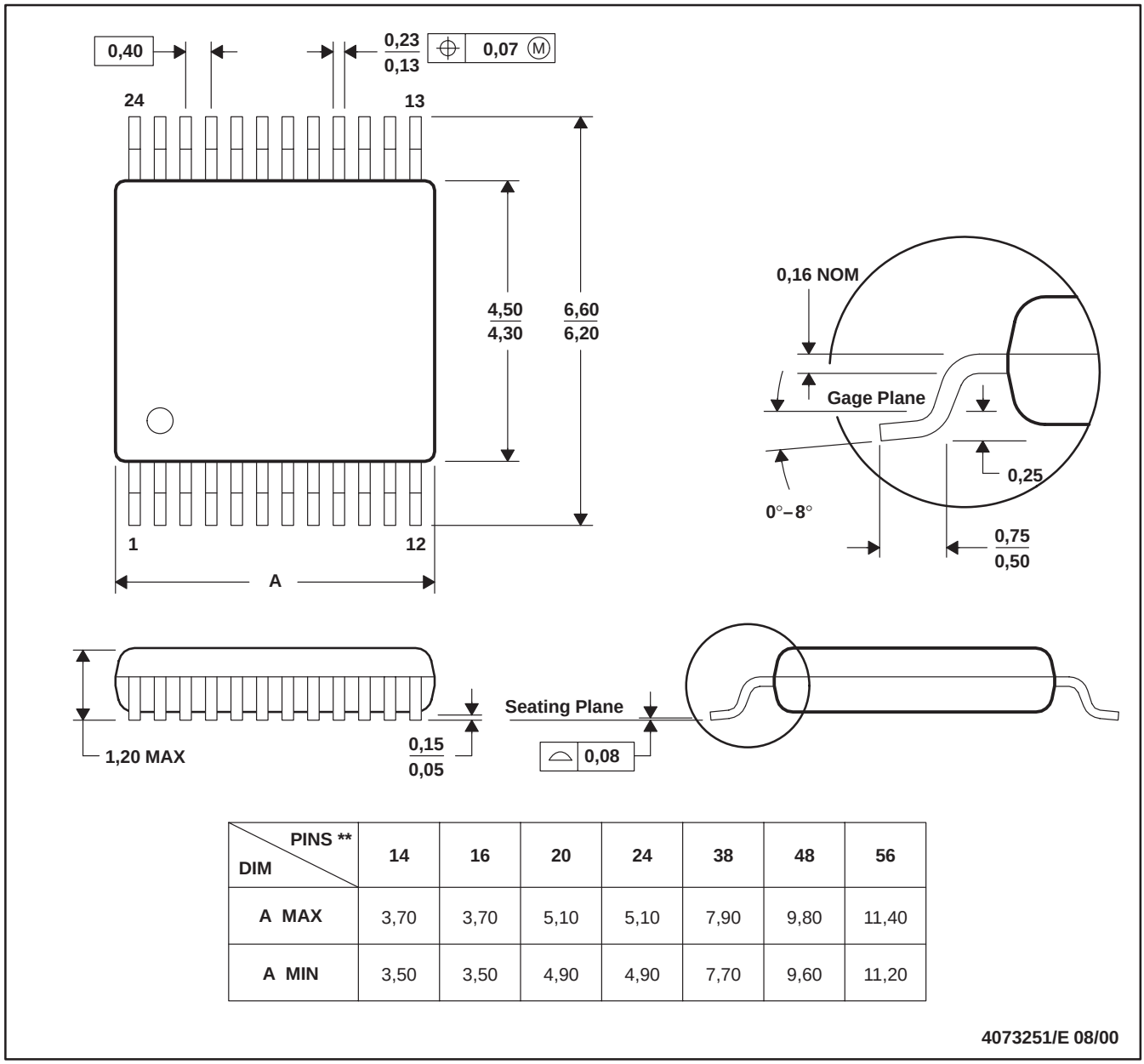
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV821DBVR	SOT-23	DBV	5	3000	205.0	200.0	33.0
LMV821DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
LMV821DBVT	SOT-23	DBV	5	250	205.0	200.0	33.0
LMV821DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
LMV821DCKR	SC70	DCK	5	3000	205.0	200.0	33.0
LMV821DCKR	SC70	DCK	5	3000	203.0	203.0	35.0
LMV821DCKT	SC70	DCK	5	250	180.0	180.0	18.0
LMV821DCKT	SC70	DCK	5	250	203.0	203.0	35.0
LMV821IDBVR	SOT-23	DBV	5	3000	203.0	203.0	35.0
LMV821IDBVT	SOT-23	DBV	5	250	203.0	203.0	35.0
LMV821IDCKR	SC70	DCK	5	3000	203.0	203.0	35.0
LMV821IDCKT	SC70	DCK	5	250	180.0	180.0	18.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV821IDCKT	SC70	DCK	5	250	203.0	203.0	35.0
LMV822DGKR	MSOP	DGK	8	2500	332.0	358.0	35.0
LMV822DR	SOIC	D	8	2500	340.5	338.1	20.6
LMV822IDGKR	MSOP	DGK	8	2500	332.0	358.0	35.0
LMV822IDR	SOIC	D	8	2500	340.5	338.1	20.6
LMV824DGVR	TVSOP	DGV	14	2000	346.0	346.0	29.0
LMV824DR	SOIC	D	14	2500	346.0	346.0	33.0
LMV824IDGVR	TVSOP	DGV	14	2000	346.0	346.0	29.0
LMV824IDR	SOIC	D	14	2500	346.0	346.0	33.0
LMV824IPWR	TSSOP	PW	14	2000	346.0	346.0	29.0
LMV824PWR	TSSOP	PW	14	2000	346.0	346.0	29.0

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

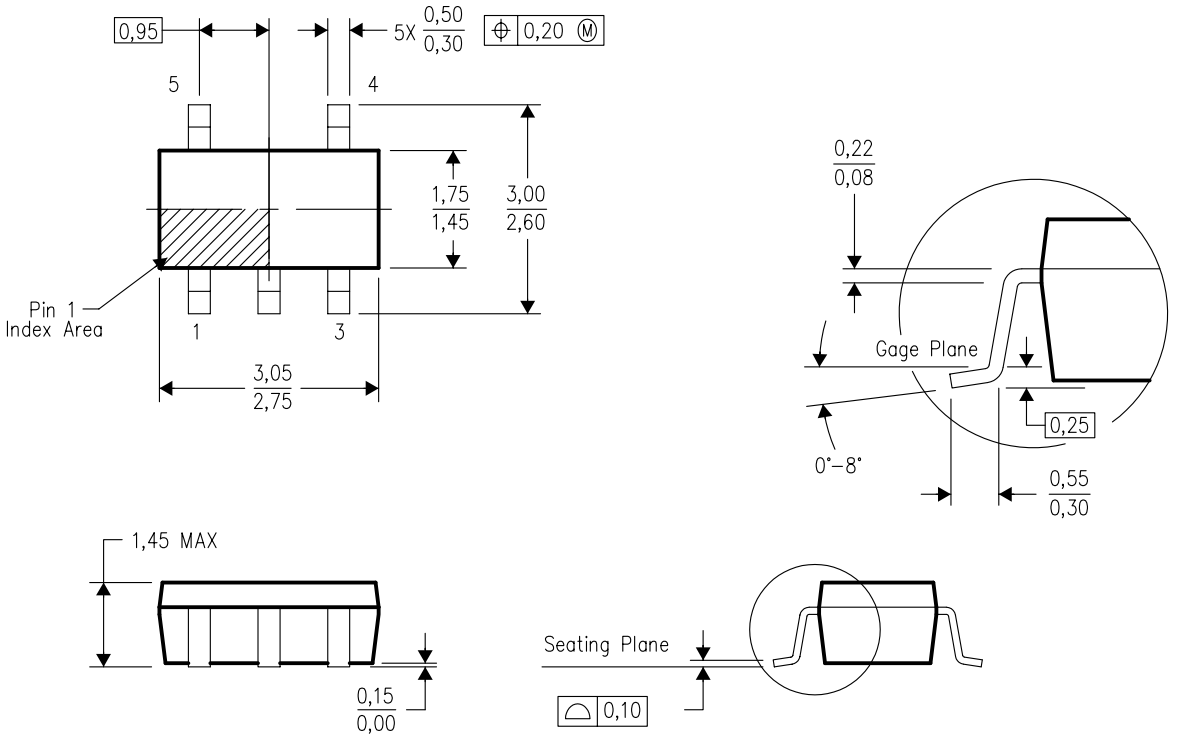


DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

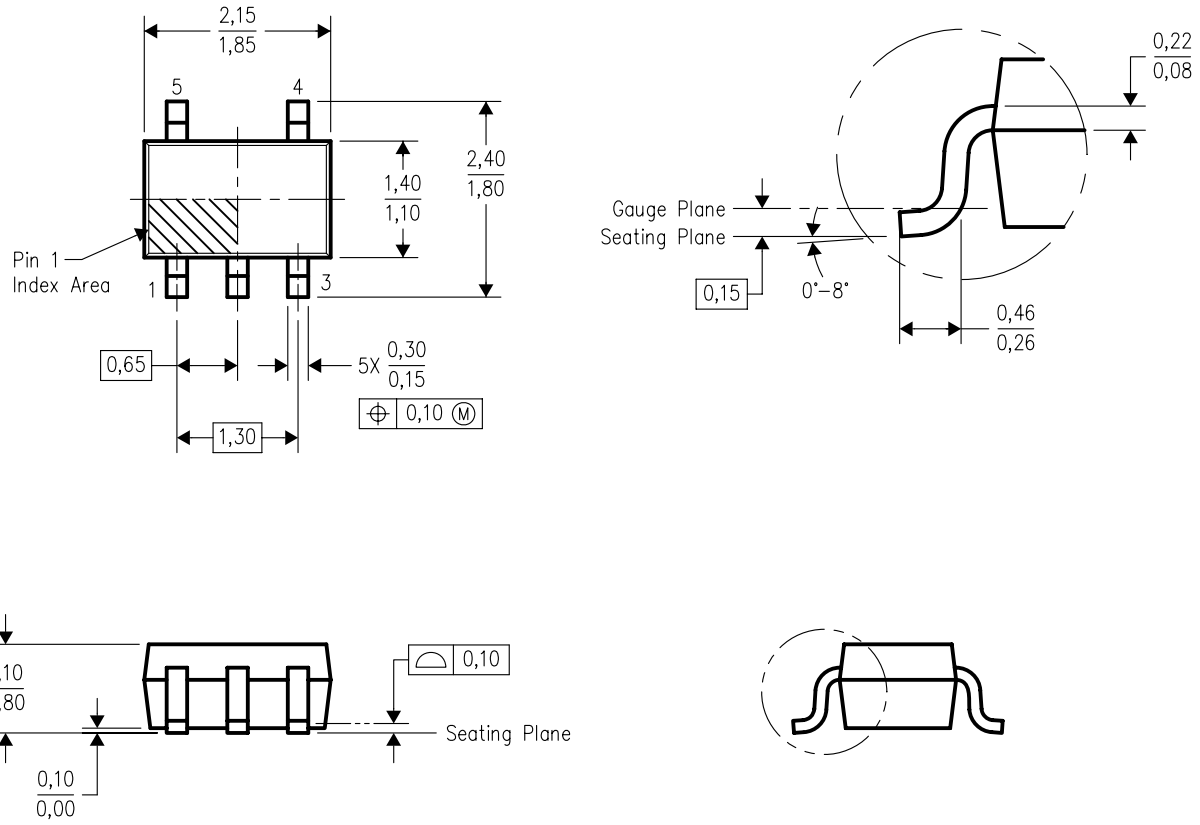
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/K 03/2006

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

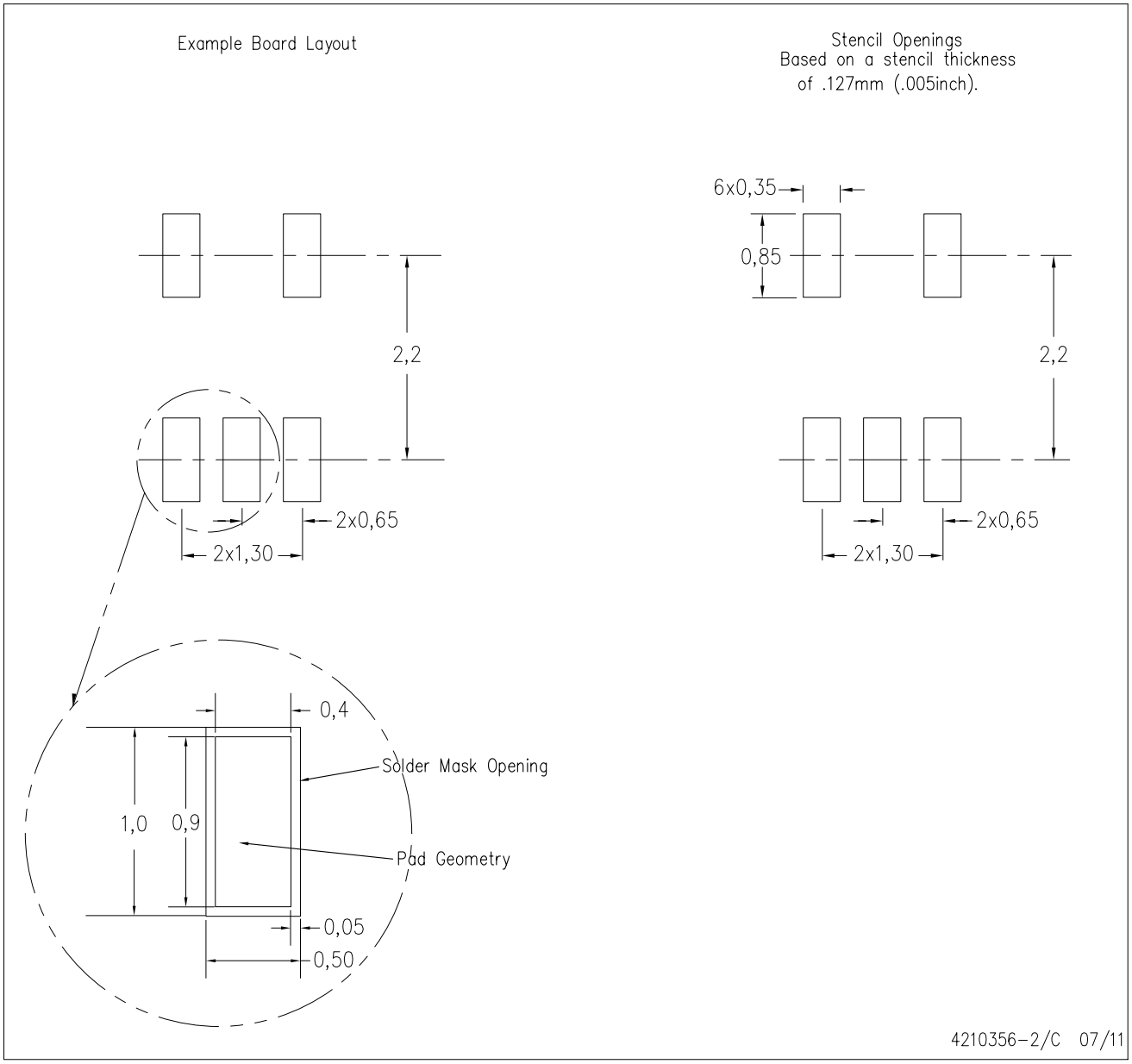
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

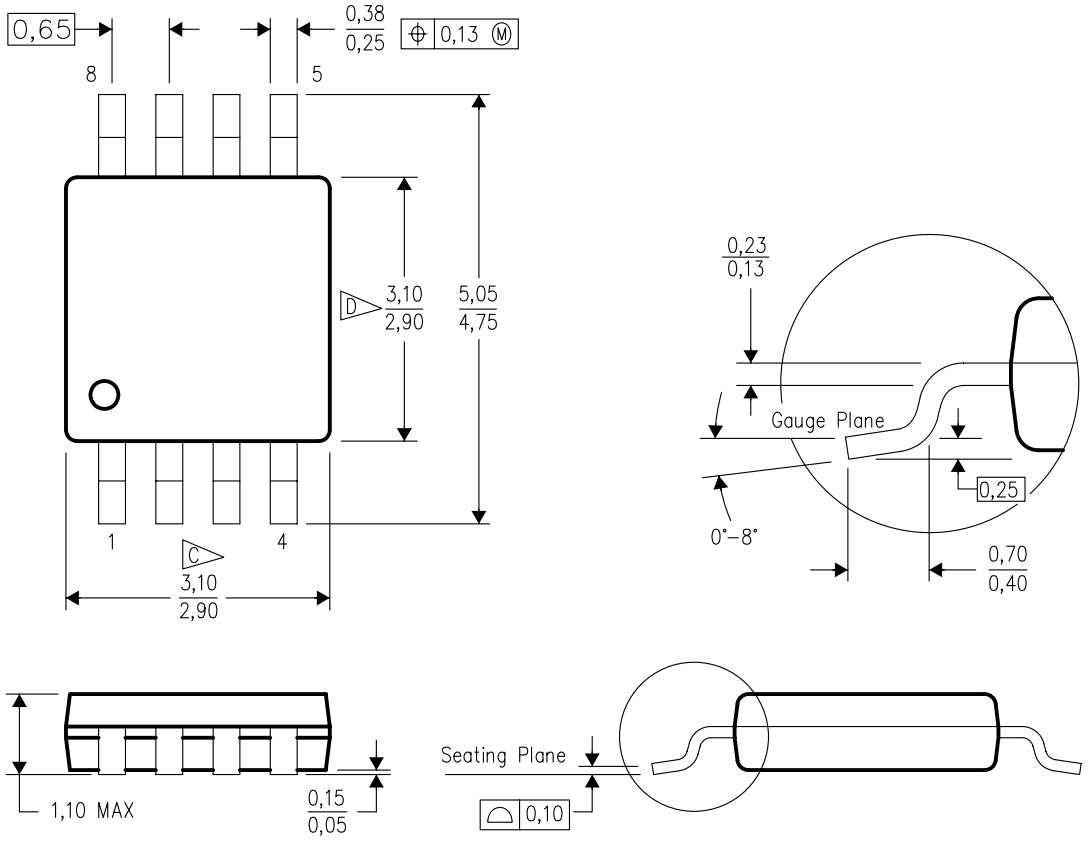
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

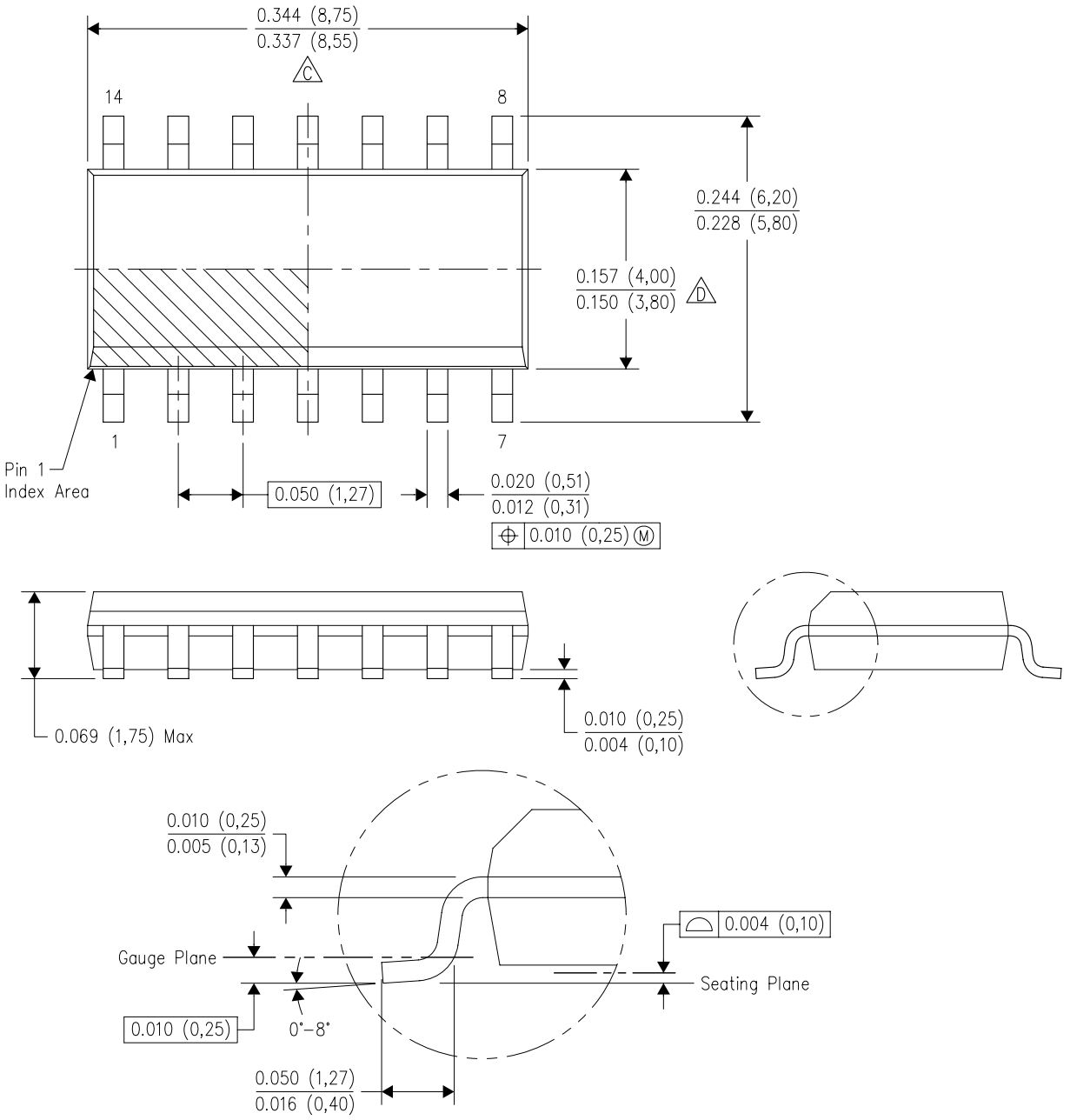
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

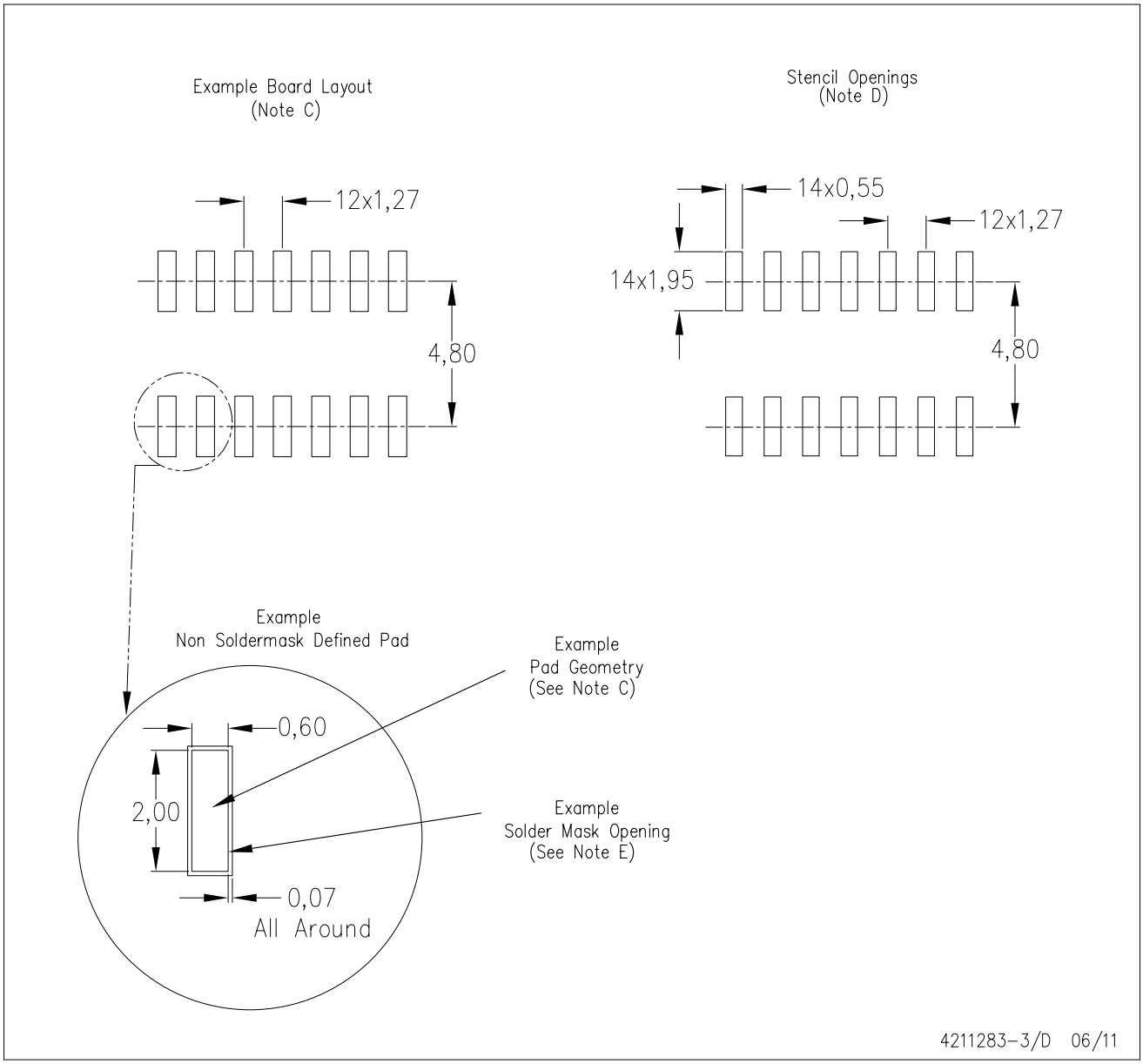
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

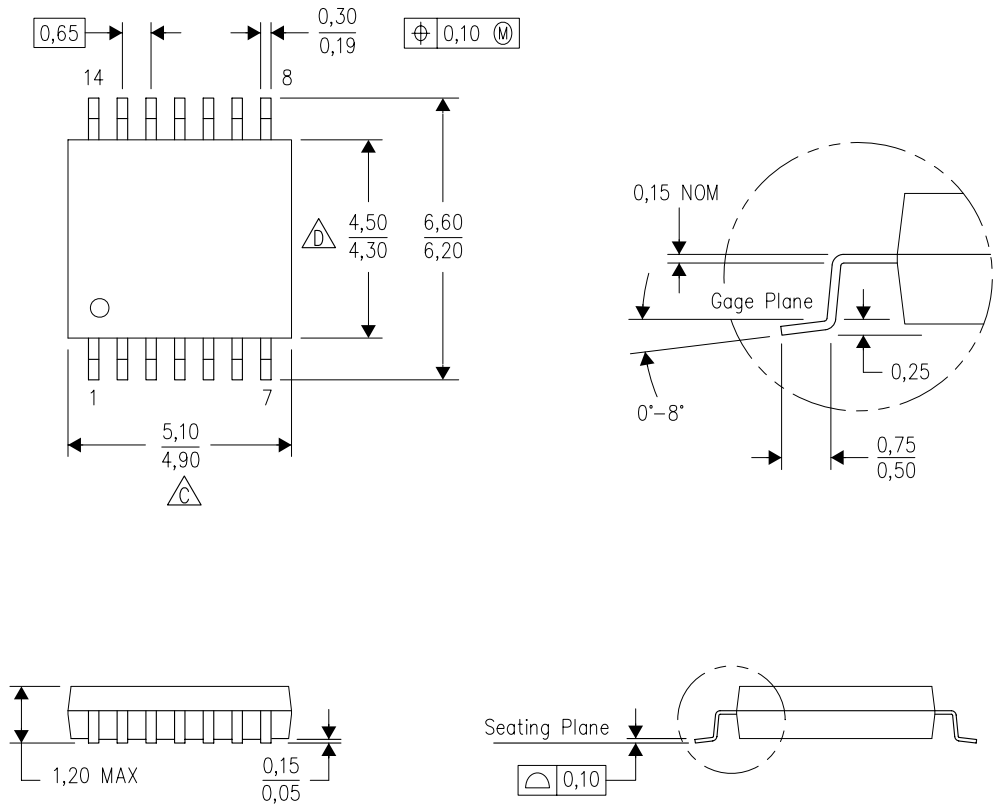
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

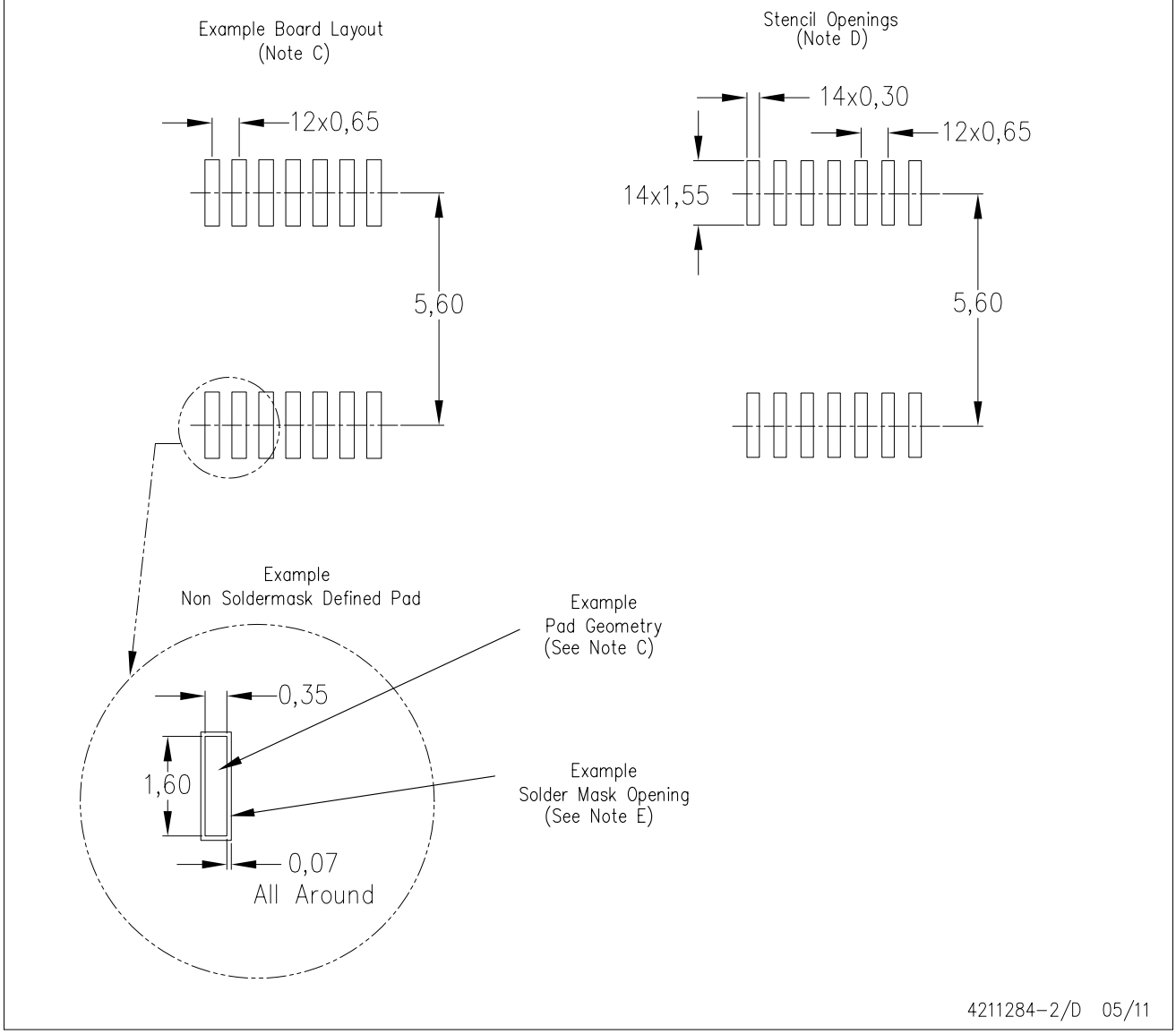
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

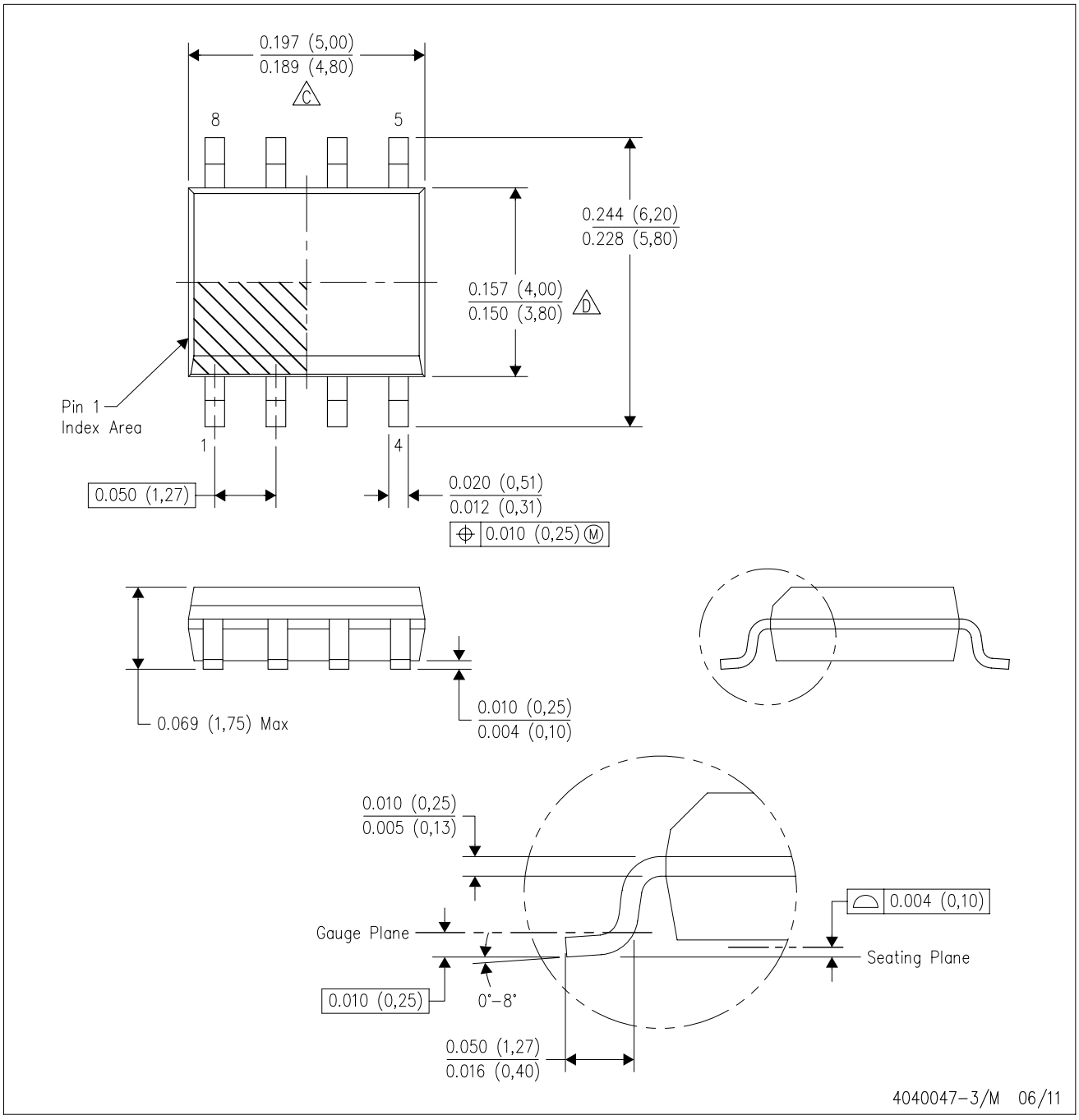
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



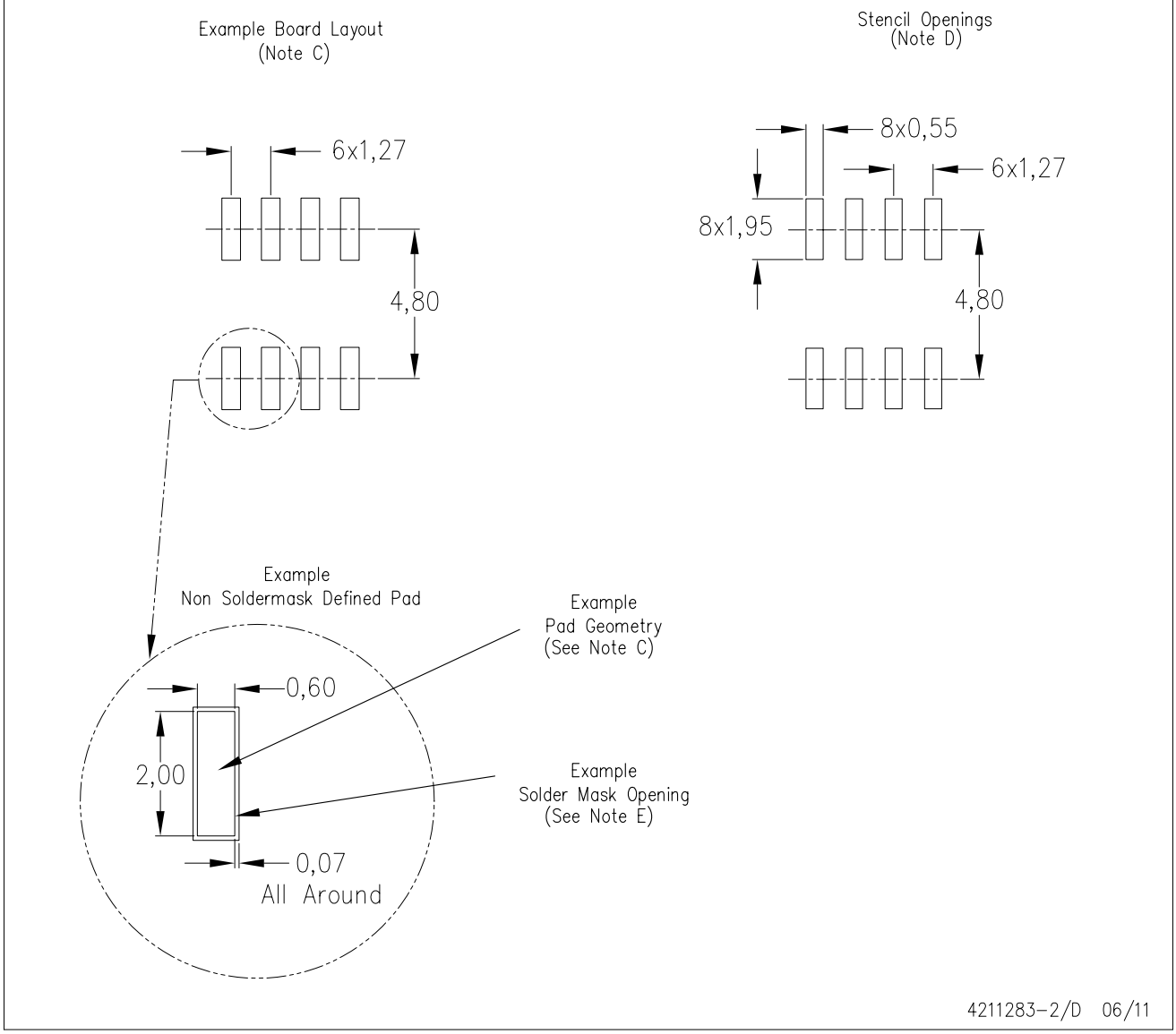
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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