LP38690-ADJ
LP38692-ADJ 1A Low Dropout CMOS Linear Regulators with Adjustable Output
Stable with Ceramic Output Capacitors

Check for Samples: LP38690-ADJ, LP38692-ADJ

FEATURES

- **Output Voltage Range of 1.25V - 9V**
- **2.5% Adjust Pin Voltage Accuracy (25°C)**
- **Low Dropout Voltage: 450mV @ 1A (typ, 5V out)**
- **Wide Input Voltage Range (2.7V to 10V)**
- **Precision (Trimmed) Bandgap Reference**
- **Ensured Specs for -40°C to +125°C**
- **1µA Off-State Quiescent Current**
- **Thermal Overload Protection**
- **Foldback Current Limiting**
- **SOT-223 and 6-Lead WSON Packages**
- **Enable Pin (LP38692-ADJ)**

APPLICATIONS

- **Hard Disk Drives**
- **Notebook Computers**
- **Battery Powered Devices**
- **Portable Instrumentation**

DESCRIPTION

The LP38690/2-ADJ low dropout CMOS linear regulators provide 2.5% precision reference voltage, extremely low dropout voltage (450mV @ 1A load current, V_{OUT} = 5V) and excellent AC performance utilizing ultra low ESR ceramic output capacitors.

The low thermal resistance of the WSON and SOT-223 packages allow the full operating current to be used even in high ambient temperature environments.

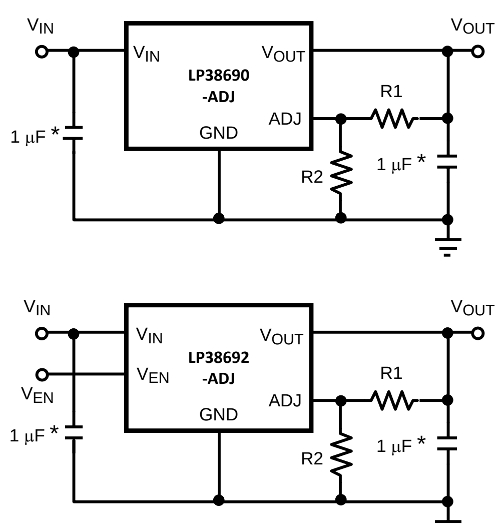
The use of a PMOS power transistor means that no DC base drive current is required to bias it allowing ground pin current to remain below 100 µA regardless of load current, input voltage, or operating temperature.

Dropout Voltage: 450 mV (typ) @ 1A (typ. 5V out).

Ground Pin Current: 55 µA (typ) at full load.

Adjust Pin Voltage: 2.5% (25°C) accuracy.

Typical Application Circuits



$V_{OUT} = V_{ADJ}$ x (1 + R1/R2)
*Minimum value required for stability.

Connection Diagrams

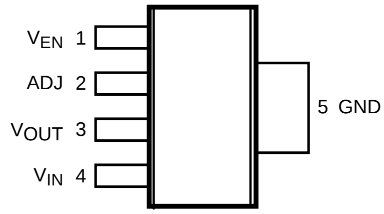


Figure 1. SOT-223 (LP38692MP-ADJ) – Top View
See Package Number NDC0005A

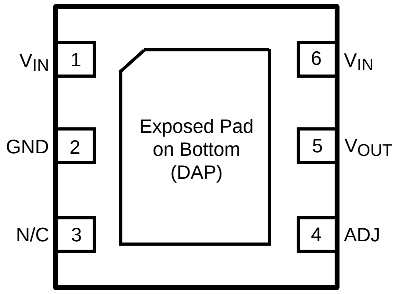


Figure 2. 6-Lead WSON (LP38690SD-ADJ) – Top View
See Package Number NGG0006A

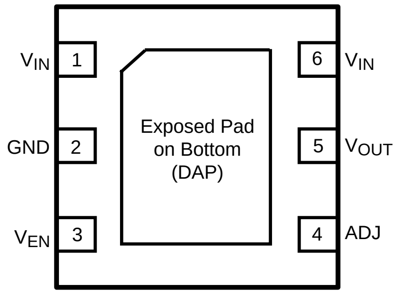


Figure 3. 6-Lead WSON (LP38692SD-ADJ) Top View
See Package Number NGG

PIN DESCRIPTIONS

Pin	Description
V_{IN}	This is the input supply voltage to the regulator. For WSON package devices, both V_{IN} pins must be tied together for full current operation (500mA maximum per pin).
GND	Circuit ground for the regulator. For the SOT-223 package this is thermally connected to the die and functions as a thermal connection when the soldered down to a large copper plane.
V_{OUT}	Regulated output voltage.
V_{EN}	The enable pin allows the part to be turned ON and OFF by pulling this pin high or low.
ADJ	The adjust pin is used to set the regulated output voltage by connecting it to the external resistors R1 and R2 (see Typical Application Circuits).
DAP	WSON Only - The DAP (Exposed Pad) functions as a thermal connection when soldered to a copper plane. See WSON MOUNTING section in APPLICATION HINTS for more information.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)

Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 5 seconds)	260°C
ESD Rating(3)	2 kV
Power Dissipation(4)	Internally Limited
V(max) All pins (with respect to GND)	-0.3V to 12V
I_{OUT}(5)	Internally Limited
Junction Temperature	−40°C to +150°C

(1) Absolute maximum ratings indicate limits beyond which damage to the component may occur. Operating ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications, see Electrical Characteristics. Specifications do not apply when operating the device outside of its rated operating conditions.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) ESD is tested using the human body model which is a 100pF capacitor discharged through a 1.5k resistor into each pin.
(4) At elevated temperatures, device power dissipation must be derated based on package thermal resistance and heatsink values (if a heatsink is used). The junction-to-ambient thermal resistance (θ_{J-A}) for the SOT-223 is approximately 125 °C/W for a PC board mounting with the device soldered down to minimum copper area (less than 0.1 square inch). If one square inch of copper is used as a heat dissipator for the SOT-223, the θ_{J-A} drops to approximately 70 °C/W. The θ_{J-A} values for the WSON package are also dependent on trace area, copper thickness, and the number of thermal vias used (refer to the TI AN-1187 Application Report and the WSON MOUNTING section in this datasheet). If power disspation causes the junction temperature to exceed specified limits, the device will go into thermal shutdown.
(5) If used in a dual-supply system where the regulator load is returned to a negative supply, the output pin must be diode clamped to ground.

OPERATING RATINGS

V_{IN} Supply Voltage	2.7V to 10V
Operating Junction Temperature Range	−40°C to +125°C

ELECTRICAL CHARACTERISTICS

Limits in standard typeface are for T_J = 25°C, and limits in **boldface type** apply over the full operating temperature range. Unless otherwise specified: $V_{IN} = V_{OUT}$ + 1V, $C_{IN} = C_{OUT}$ = 10 µF, I_{LOAD} = 10mA. Min/Max limits are specified through testing, statistical correlation, or design.

Symbol	Parameter	Conditions	Min	Typ (1)	Max	Units
V_{ADJ}	ADJ Pin Voltage	V_{IN} = 2.7V	1.219	1.25	1.281	V
		3.2V ≤ V_{IN} ≤ 10V 100 µA < I_L < 1A	**1.187**	1.25	**1.313**	
$\Delta V_O/\Delta V_{IN}$	Output Voltage Line Regulation (2)	V_O + 0.5V ≤ V_{IN} ≤ 10V I_L = 25mA		0.03	**0.1**	%/V
$\Delta V_O/\Delta I_L$	Output Voltage Load Regulation (3)	1 mA < I_L < 1A $V_{IN} = V_O$ + 1V		1.8	**5**	%/A
V_{IN} - V_O	Dropout Voltage (4)	(V_O = 1.8V) I_L = 1A		950	**1600**	mV
		(V_O = 2.5V) I_L = 0.1A I_L = 1A		80 800	**145** **1300**	
		(V_O = 3.3V) I_L = 0.1A I_L = 1A		65 650	**110** **1000**	
		(V_O = 5V) I_L = 0.1A I_L = 1A		45 450	**100** **800**	
I_Q	Quiescent Current	V_{IN} ≤ 10V, I_L = 100 µA - 1A		55	**100**	µA
		V_{EN} ≤ 0.4V, (LP38692-ADJ Only)		0.001	1	
I_L(MIN)	Minimum Load Current	V_{IN} - V_O ≤ 4V			**100**	
I_{FB}	Foldback Current Limit	V_{IN} - V_O > 5V		450		mA
		V_{IN} - V_O < 4V		1500		
PSRR	Ripple Rejection	$V_{IN} = V_O$ + 2V(DC), with 1V(p-p) / 120Hz Ripple		55		dB
T_{SD}	Thermal Shutdown Activation (Junction Temp)			160		°C
T_{SD} (HYST)	Thermal Shutdown Hysteresis (Junction Temp)			10		
I_{ADJ}	ADJ Input Leakage Current	V_{ADJ} = 0 - 1.5V V_{IN} = 10V	-100	0.01	100	nA
e_n	Output Noise	BW = 10Hz to 10kHz V_O = 3.3V		0.7		$\mu V/\sqrt{Hz}$
V_O (LEAK)	Output Leakage Current	$V_O = V_O$(NOM) + 1V @ 10V_{IN}		0.5	2	µA
V_{EN}	Enable Voltage (LP38692-ADJ Only)	Output = OFF			**0.4**	V
		Output = ON, V_{IN} = 4V	**1.8**			
		Output = ON, V_{IN} = 6V	**3.0**			
		Output = ON, V_{IN} = 10V	**4.0**			
I_{EN}	Enable Pin Leakage (LP38692-ADJ Only)	V_{EN} = 0V or 10V, V_{IN} = 10V	-1	0.001	1	µA

(1) Typical numbers represent the most likely parametric norm for 25°C operation.
(2) Output voltage line regulation is defined as the change in output voltage from nominal value resulting from a change in input voltage.
(3) Output voltage load regulation is defined as the change in output voltage from nominal value as the load current increases from 1mA to full load.
(4) Dropout voltage is defined as the minimum input to output differential required to maintain the output within 100mV of nominal value.

BLOCK DIAGRAMS

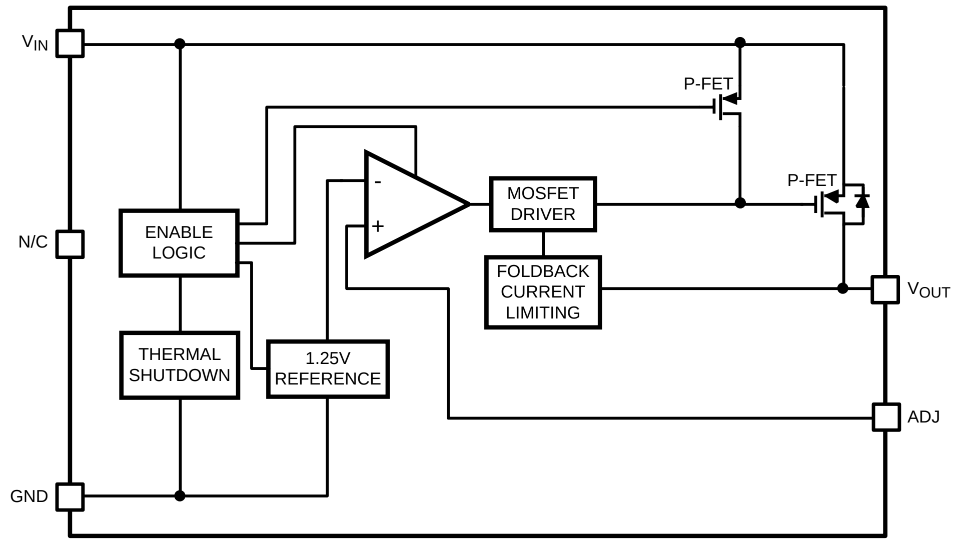


Figure 4. LP38690-ADJ Functional Diagram (WSON)

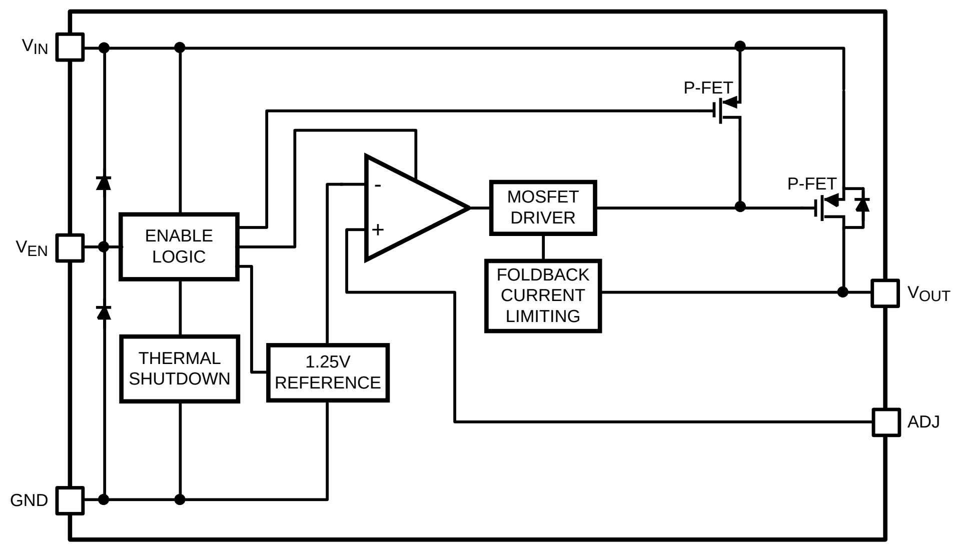


Figure 5. LP38692-ADJ Functional Diagram (SOT-223, WSON)

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified: T_J = 25°C, C_{IN} = C_{OUT} = 10 µF, enable pin is tied to V_{IN} (LP38692-ADJ only), V_O = 1.25V, V_{IN} = 2.7V, I_L = 10mA.

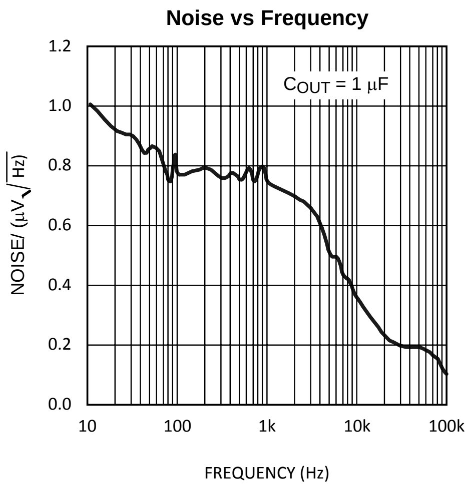


Figure 6.

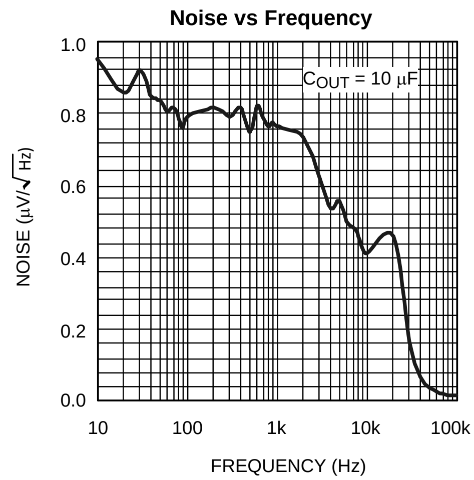


Figure 7.

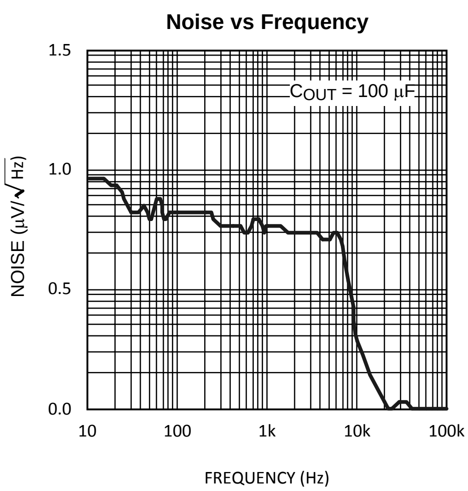


Figure 8.

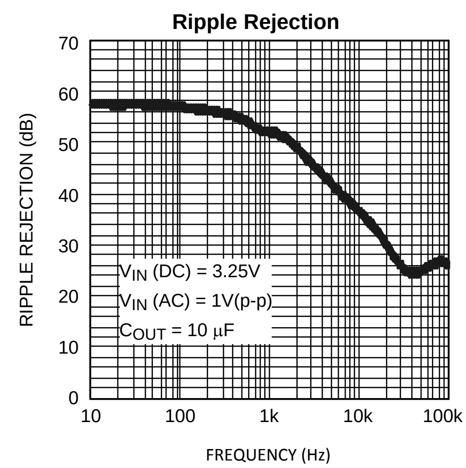


Figure 9.

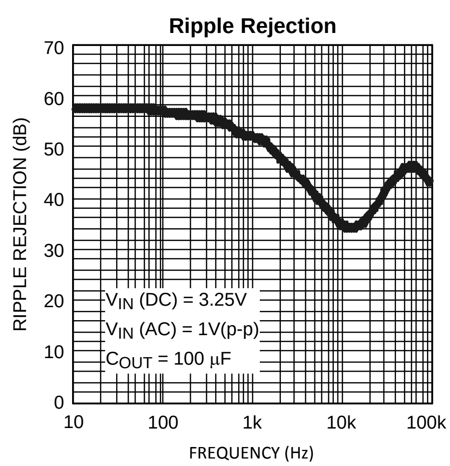


Figure 10.

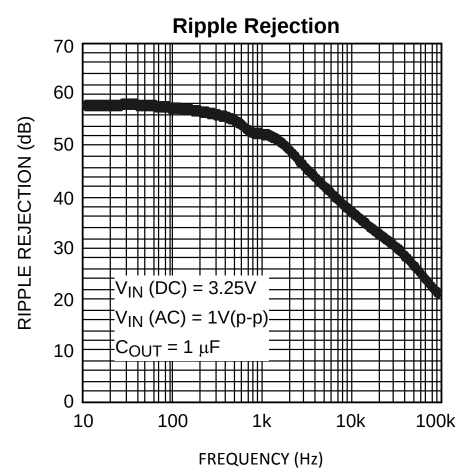


Figure 11.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: T_J = 25°C, C_{IN} = C_{OUT} = 10 µF, enable pin is tied to V_{IN} (LP38692-ADJ only), V_O = 1.25V, V_{IN} = 2.7V, I_L = 10mA.

V_{ADJ} vs Temperature

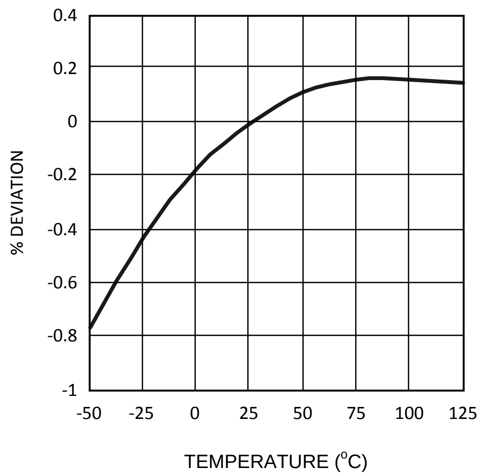


Figure 12.

Line Transient Response

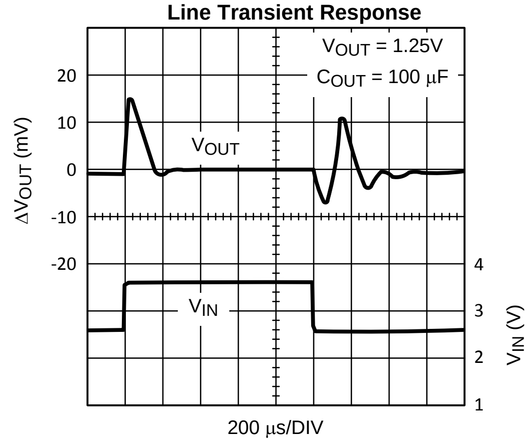


Figure 13.

Line Transient Response

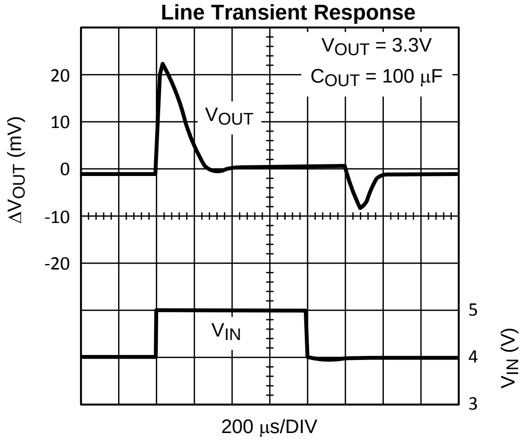


Figure 14.

Line Transient Response

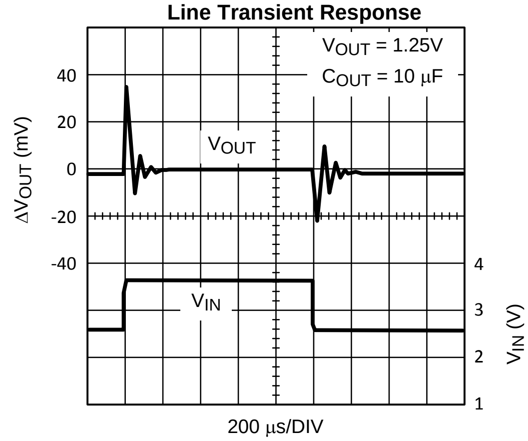


Figure 15.

Line Transient Response

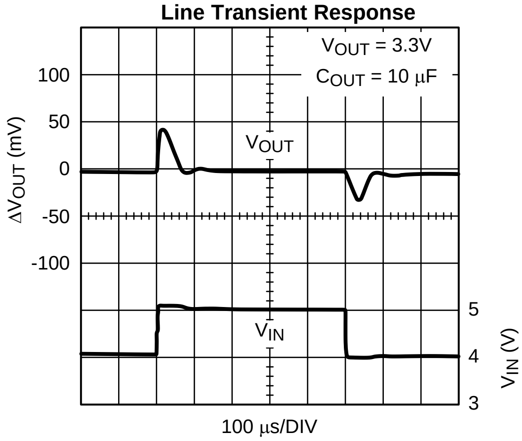


Figure 16.

Line Transient Response

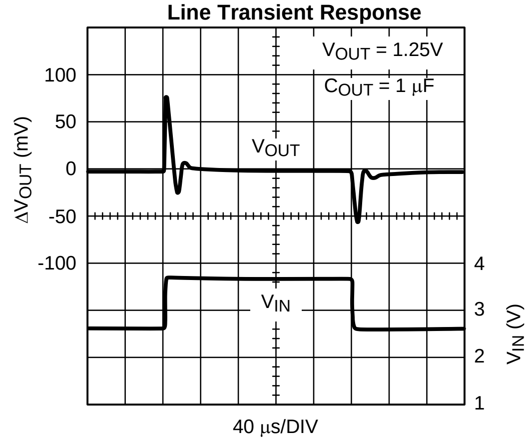


Figure 17.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: T_J = 25°C, C_{IN} = C_{OUT} = 10 µF, enable pin is tied to V_{IN} (LP38692-ADJ only), V_O = 1.25V, V_{IN} = 2.7V, I_L = 10mA.

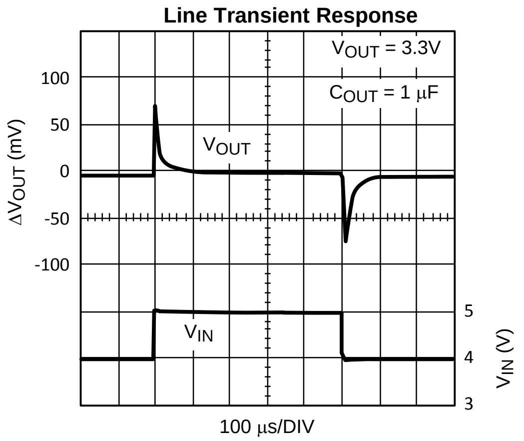


Figure 18.

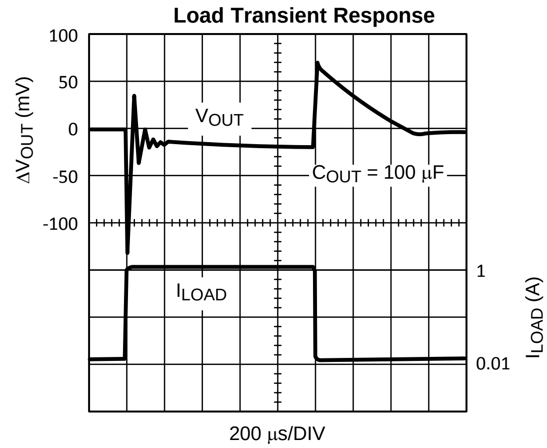


Figure 19.

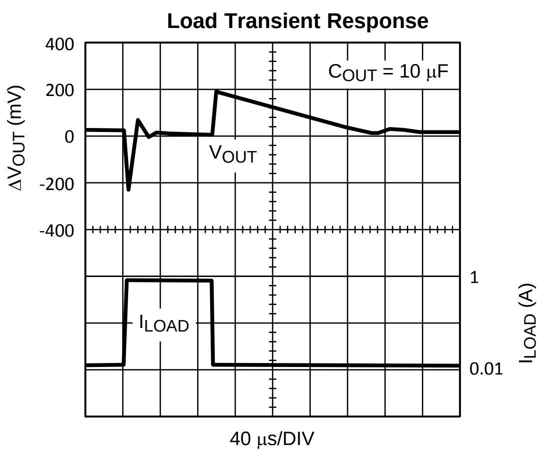


Figure 20.

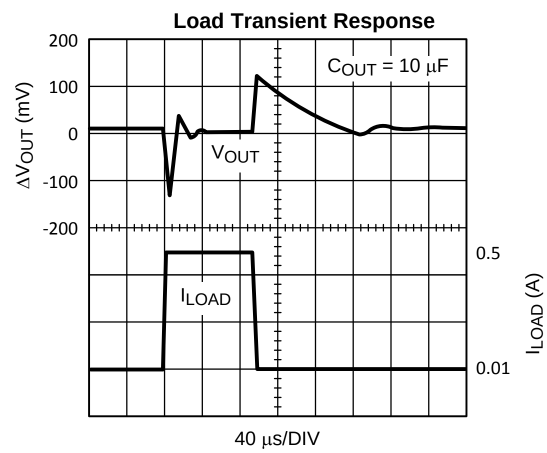


Figure 21.

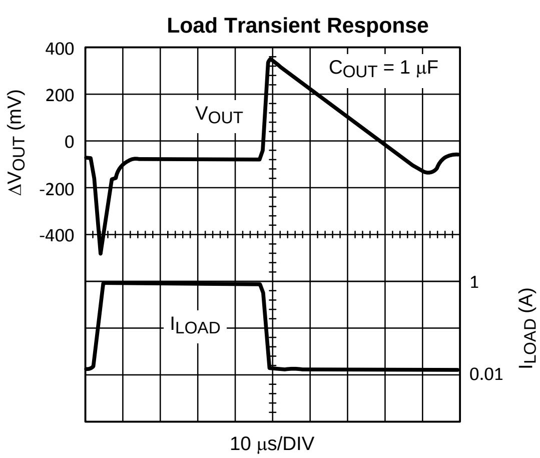


Figure 22.

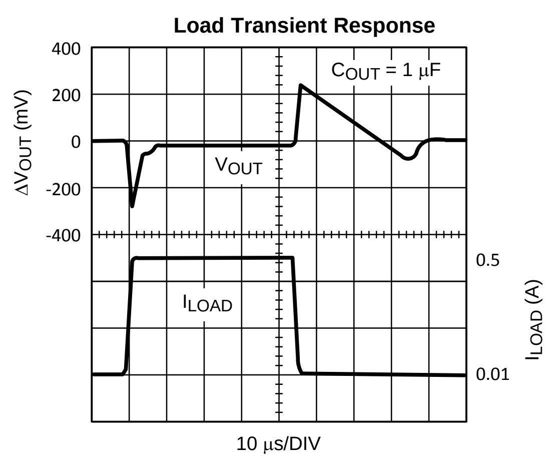


Figure 23.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: T_J = 25°C, C_{IN} = C_{OUT} = 10 µF, enable pin is tied to V_{IN} (LP38692-ADJ only), V_O = 1.25V, V_{IN} = 2.7V, I_L = 10mA.

V_{OUT} vs V_{IN} , V_{OUT} = 1.25V

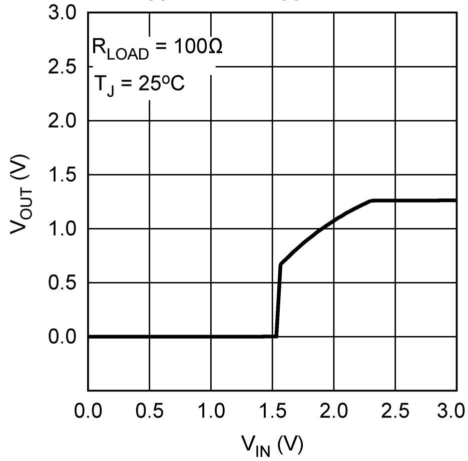


Figure 24.

V_{OUT} vs V_{IN} , V_{OUT} = 1.80V

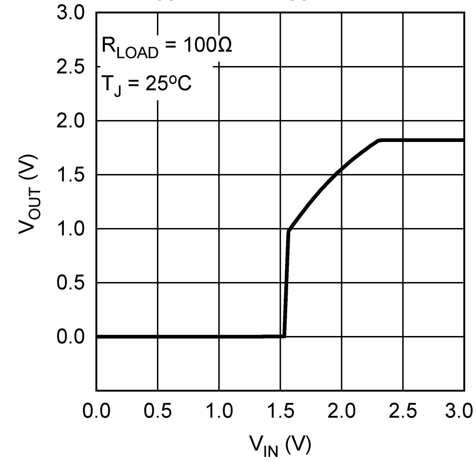


Figure 25.

V_{OUT} vs V_{IN} (Power-Up)

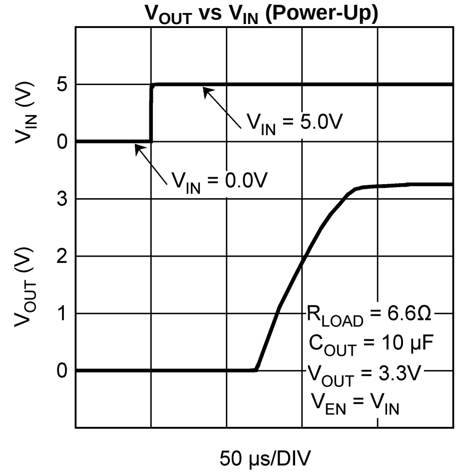


Figure 26.

V_{OUT} vs V_{EN}, ON (LP38692 Only)

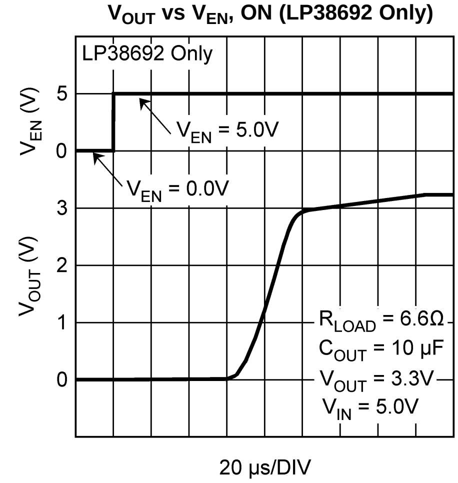


Figure 27.

V_{OUT} vs V_{EN}, OFF (LP38692 Only)

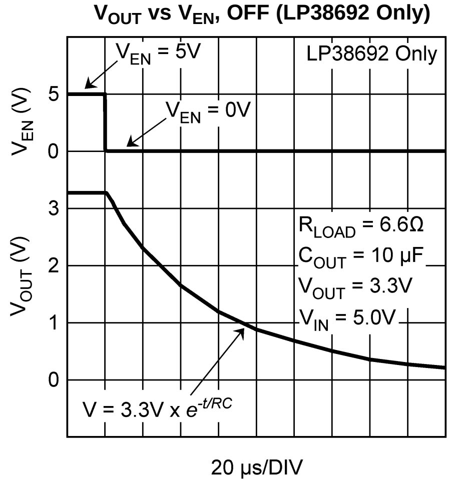


Figure 28.

Minimum V_{IN} vs I_{OUT}

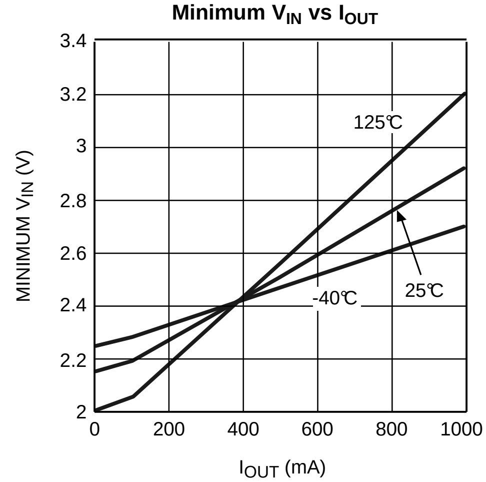


Figure 29.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: T_J = 25°C, C_{IN} = C_{OUT} = 10 µF, enable pin is tied to V_{IN} (LP38692-ADJ only), V_O = 1.25V, V_{IN} = 2.7V, I_L = 10mA.

Dropout Voltage vs I_{OUT}

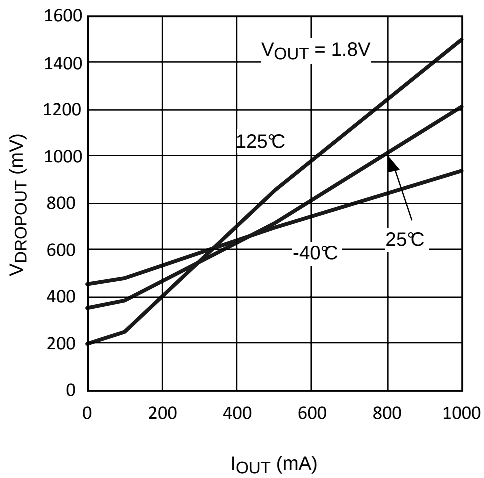


Figure 30.

Enable Voltage vs Temperature

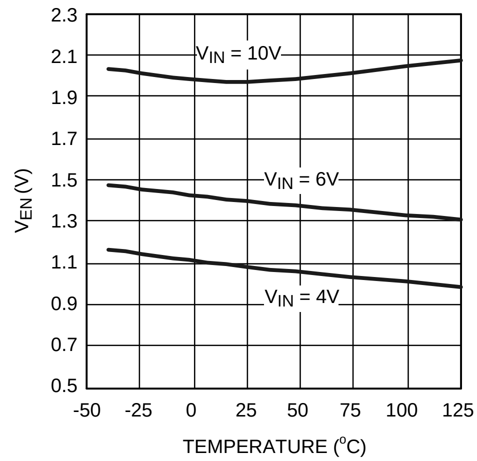


Figure 31.

Load Regulation vs Temperature

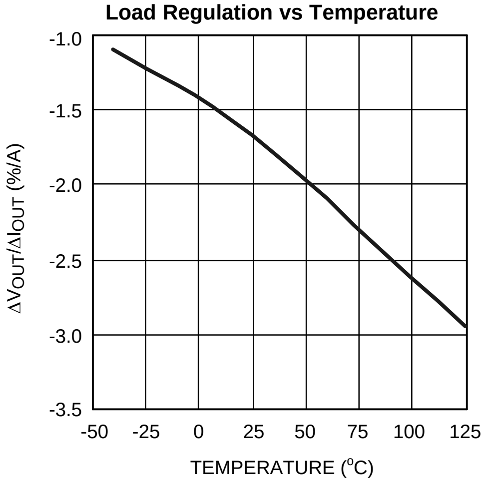


Figure 32.

Line Regulation vs Temperature

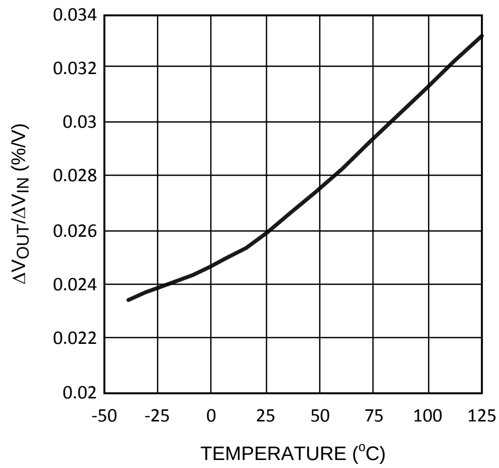


Figure 33.

APPLICATION HINTS

EXTERNAL CAPACITORS

Like any low-dropout regulator, external capacitors are required to assure stability. These capacitors must be correctly selected for proper performance.

INPUT CAPACITOR:

An input capacitor of at least 1µF is required (ceramic recommended). The capacitor must be located not more than one centimeter from the input pin and returned to a clean analog ground.

OUTPUT CAPACITOR:

An output capacitor is required for loop stability. It must be located less than 1 centimeter from the device and connected directly to the output and ground pins using traces which have no other currents flowing through them.

The minimum amount of output capacitance that can be used for stable operation is 1µF. Ceramic capacitors are recommended (the LP38690/2-ADJ was designed for use with ultra low ESR capacitors). The LP38690/2-ADJ is stable with any output capacitor ESR between zero and 100 Ohms.

SETTING THE OUTPUT VOLTAGE:

The output voltage is set using the external resistors R1 and R2 (see Typical Application Circuits). The output voltage will be given by the equation:

$$V_{OUT} = V_{ADJ} \times (1 + (R1 / R2)) \quad (1)$$

Because the part has a minimum load current requirement of 100 µA, it is recommended that R2 always be 12k Ohms or less to provide adequate loading. Even if a minimum load is always provided by other means, it is not recommended that very high value resistors be used for R1 and R2 because it can make the ADJ node susceptible to noise pickup. A maximum value of 100k is recommended for R2 to prevent this from occurring.

ENABLE PIN (LP38692-ADJ only):

The LP38692–ADJ has an Enable pin (EN) which allows an external control signal to turn the regulator output On and Off. The Enable On/Off threshold has no hysteresis. The voltage signal must rise and fall cleanly, and promptly, through the ON and OFF voltage thresholds. The Enable pin has no internal pull-up or pull-down to establish a default condition and, as a result, this pin must be terminated either actively or passively. If the Enable pin is driven from a source that actively pulls high and low, the drive voltage should not be allowed to go below ground potential or higher than V_{IN}. If the application does not require the Enable function, the pin should be connected directly to the V_{IN} pin.

FOLDBACK CURRENT LIMITING:

Foldback current limiting is built into the LP38690/2-ADJ which reduces the amount of output current the part can deliver as the output voltage is reduced. The amount of load current is dependent on the differential voltage between V_{IN} and V_{OUT}. Typically, when this differential voltage exceeds 5V, the load current will limit at about 450 mA. When the V_{IN} -V_{OUT} differential is reduced below 4V, load current is limited to about 1500 mA.

SELECTING A CAPACITOR

It is important to note that capacitance tolerance and variation with temperature must be taken into consideration when selecting a capacitor so that the minimum required amount of capacitance is provided over the full operating temperature range.

Capacitor Characteristics

CERAMIC

For values of capacitance in the 10 to 100 µF range, ceramics are usually larger and more costly than tantalums but give superior AC performance for bypassing high frequency noise because of very low ESR (typically less than 10 mΩ). However, some dielectric types do not have good capacitance characteristics as a function of voltage and temperature.

Z5U and Y5V dielectric ceramics have capacitance that drops severely with applied voltage. A typical Z5U or Y5V capacitor can lose 60% of its rated capacitance with half of the rated voltage applied to it. The Z5U and Y5V also exhibit a severe temperature effect, losing more than 50% of nominal capacitance at high and low limits of the temperature range.

X7R and X5R dielectric ceramic capacitors are strongly recommended if ceramics are used, as they typically maintain a capacitance range within ±20% of nominal over full operating ratings of temperature and voltage. Of course, they are typically larger and more costly than Z5U/Y5U types for a given voltage and capacitance.

TANTALUM

Solid Tantalum capacitors have good temperature stability: a high quality Tantalum will typically show a capacitance value that varies less than 10-15% across the full temperature range of -40°C to 125°C. ESR will vary only about 2X going from the high to low temperature limits.

The increasing ESR at lower temperatures can cause oscillations when marginal quality capacitors are used (if the ESR of the capacitor is near the upper limit of the stability range at room temperature).

REVERSE VOLTAGE

A reverse voltage condition will exist when the voltage at the output pin is higher than the voltage at the input pin. Typically this will happen when V_{IN} is abruptly taken low and C_{OUT} continues to hold a sufficient charge such that the input to output voltage becomes reversed. A less common condition is when an alternate voltage source is connected to the output.

There are two possible paths for current to flow from the output pin back to the input during a reverse voltage condition.

1) While V_{IN} is high enough to keep the control circuity alive, and the Enable pin (LP38692-ADJ only) is above the $V_{EN(ON)}$ threshold, the control circuitry will attempt to regulate the output voltage. If the input voltage is less than the programmed output voltage, the control circuit will drive the gate of the pass element to the full ON condition. In this condition, reverse current will flow from the output pin to the input pin, limited only by the $R_{DS(ON)}$ of the pass element and the output to input voltage differential. Discharging an output capacitor up to 1000 µF in this manner will not damage the device as the current will rapidly decay. However, continuous reverse current should be avoided. When the Enable pin is low this condition will be prevented.

2) The internal PFET pass element has an inherent parasitic diode. During normal operation, the input voltage is higher than the output voltage and the parasitic diode is reverse biased. However, when V_{IN} is below the value where the control circuity is alive, or the Enable pin is low (LP38692-ADJ only), and the output voltage is more than 500 mV (typical) above the input voltage the parasitic diode becomes forward biased and current flows from the output pin to the input pin through the diode. The current in the parasitic diode should be limited to less than 1A continuous and 5A peak.

If used in a dual-supply system where the regulator output load is returned to a negative supply, the output pin must be diode clamped to ground to limit the negative voltage transition. A Schottky diode is recommended for this protective clamp.

PCB LAYOUT

Good PC layout practices must be used or instability can be induced because of ground loops and voltage drops. The input and output capacitors must be directly connected to the input, output, and ground pins of the regulator using traces which do not have other currents flowing in them (Kelvin connect).

The best way to do this is to lay out C_{IN} and C_{OUT} near the device with short traces to the V_{IN}, V_{OUT}, and ground pins. The regulator ground pin should be connected to the external circuit ground so that the regulator and its capacitors have a "single point ground".

It should be noted that stability problems have been seen in applications where "vias" to an internal ground plane were used at the ground points of the IC and the input and output capacitors. This was caused by varying ground potentials at these nodes resulting from current flowing through the ground plane. Using a single point ground technique for the regulator and it’s capacitors fixed the problem. Since high current flows through the traces going into V_{IN} and coming from V_{OUT}, Kelvin connect the capacitor leads to these pins so there is no voltage drop in series with the input and output capacitors.

WSON MOUNTING

The NGG0006A (No Pullback) 6-Lead WSON package requires specific mounting techniques which are detailed in the TI AN-1187 Application Report. Referring to the section **PCB Design Recommendations** (Page 5), it should be noted that the pad style which should be used with the WSON package is the NSMD (non-solder mask defined) type. Additionally, it is recommended the PCB terminal pads to be 0.2 mm longer than the package pads to create a solder fillet to improve reliability and inspection.

The input current is split between two V_{IN} pins, 1 and 6. The two V_{IN} pins must be connected together to ensure that the device can meet all specifications at the rated current.

The thermal dissipation of the WSON package is directly related to the printed circuit board construction and the amount of additional copper area connected to the DAP.

The DAP (exposed pad) on the bottom of the WSON package is connected to the die substrate with a conductive die attach adhesive. The DAP has no direct electrical (wire) connection to any of the pins. There is a parasitic PN junction between the die substrate and the device ground. As such, it is strongly recommend that the DAP be connected directly to the ground at device lead 2 (i.e. GND). Alternately, but not recommended, the DAP may be left floating (i.e. no electrical connection). The DAP must not be connected to any potential other than ground.

For the LP38690-ADJ and LP38692-ADJ in the NGG0006A 6- Lead WSON package, the junction-to-case thermal rating, θ_{JC}, is 10.4°C/W, where the case is the bottom of the package at the center of the DAP. The junction-to-ambient thermal performance for the LP38690-ADJ and LP38692-ADJ in the NGG0006A 6-Lead WSON package, using the JEDEC JESD51 standards is summarized in the following table:

Board Type	Thermal Vias	θ_{JC}	θ_{JA}
JEDEC 2–Layer JESD 51-3	None	10.4°C/W	237°C/W
JEDEC 4–Layer JESD 51-7	1	10.4°C/W	74°C/W
	2	10.4°C/W	60°C/W
	4	10.4°C/W	49°C/W
	6	10.4°C/W	45°C/W

RFI/EMI SUSCEPTIBILITY

RFI (radio frequency interference) and EMI (electromagnetic interference) can degrade any integrated circuit's performance because of the small dimensions of the geometries inside the device. In applications where circuit sources are present which generate signals with significant high frequency energy content (> 1 MHz), care must be taken to ensure that this does not affect the IC regulator.

If RFI/EMI noise is present on the input side of the regulator (such as applications where the input source comes from the output of a switching regulator), good ceramic bypass capacitors must be used at the input pin of the IC.

If a load is connected to the IC output which switches at high speed (such as a clock), the high-frequency current pulses required by the load must be supplied by the capacitors on the IC output. Since the bandwidth of the regulator loop is less than 100 kHz, the control circuitry cannot respond to load changes above that frequency. This means the effective output impedance of the IC at frequencies above 100 kHz is determined only by the output capacitor(s).

In applications where the load is switching at high speed, the output of the IC may need RF isolation from the load. It is recommended that some inductance be placed between the output capacitor and the load, and good RF bypass capacitors be placed directly across the load.

PCB layout is also critical in high noise environments, since RFI/EMI is easily radiated directly into PC traces. Noisy circuitry should be isolated from "clean" circuits where possible, and grounded through a separate path. At MHz frequencies, ground planes begin to look inductive and RFI/ EMI can cause ground bounce across the ground plane. In multi-layer PCB applications, care should be taken in layout so that noisy power and ground planes do not radiate directly into adjacent layers which carry analog power and ground.

OUTPUT NOISE

Noise is specified in two ways- **Spot Noise** or **Output Noise** density is the RMS sum of all noise sources, measured at the regulator output, at a specific frequency (measured with a 1Hz bandwidth). This type of noise is usually plotted on a curve as a function of frequency. **Total Output Noise** or **Broad-Band Noise** is the RMS sum of spot noise over a specified bandwidth, usually several decades of frequencies.

Attention should be paid to the units of measurement. Spot noise is measured in units µV/root-Hz or nV/root-Hz and total output noise is measured in µV(rms)

The primary source of noise in low-dropout regulators is the internal reference. Noise can be reduced in two ways: by increasing the transistor area or by increasing the current drawn by the internal reference. Increasing the area will decrease the chance of fitting the die into a smaller package. Increasing the current drawn by the internal reference increases the total supply current (ground pin current).

REVISION HISTORY

Changes from Revision G (April 2013) to Revision H	Page
• Changed layout of National Data Sheet to TI format	14

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