

LP3872/LP3875 1.5A Fast Ultra Low Dropout Linear Regulators

Check for Samples: [LP3872, LP3875](#)

FEATURES

- Ultra Low Dropout Voltage
- Low Ground Pin Current
- Load Regulation of 0.06%
- 10nA Quiescent Current in Shutdown Mode
- Ensured Output Current of 1.5A DC
- Available in DDPAK/TO-263, TO-220 and SOT-223 Packages
- Output Voltage Accuracy $\pm 1.5\%$
- Error Flag Indicates Output Status
- Sense Option Improves Load Regulation
- Minimum Output Capacitor Requirements
- Overtemperature/Overcurrent Protection
- -40°C to $+125^{\circ}\text{C}$ Junction Temperature Range

APPLICATIONS

- Microprocessor Power Supplies
- GTL, GTL+, BTL, and SSTL Bus Terminators
- Power Supplies for DSPs
- SCSI Terminator
- Post Regulators
- High Efficiency Linear Regulators
- Battery Chargers
- Other Battery Powered Applications

DESCRIPTION

The LP3872/LP3875 series of fast ultra low-dropout linear regulators operate from a +2.5V to +7.0V input supply. Wide range of preset output voltage options are available. These ultra low dropout linear regulators respond very quickly to step changes in load, which makes them suitable for low voltage microprocessor applications. The LP3872/LP3875 are developed on a CMOS process which allows low quiescent current operation independent of output load current. This CMOS process also allows the LP3872/LP3875 to operate under extremely low dropout conditions.

Dropout Voltage: Ultra low dropout voltage; typically 38mV at 150mA load current and 380mV at 1.5A load current.

Ground Pin Current: Typically 6mA at 1.5A load current.

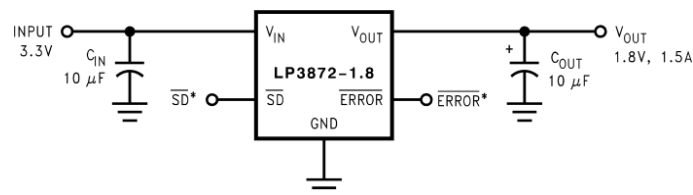
Shutdown Mode: Typically 10nA quiescent current when the shutdown pin is pulled low.

Error Flag: Error flag goes low when the output voltage drops 10% below nominal value.

SENSE: Sense pin improves regulation at remote loads.

Precision Output Voltage: Multiple output voltage options are available ranging from 1.8V to 5.0V with a specified accuracy of $\pm 1.5\%$ at room temperature, and $\pm 3.0\%$ over all conditions (varying line, load, and temperature).

TYPICAL APPLICATION CIRCUITS



*SD and ERROR pins must be pulled high through a 10kΩ pull-up resistor. Connect the ERROR pin to ground if this function is not used. See application hints for more information.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

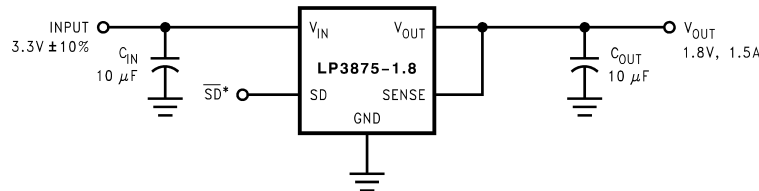
All trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2003–2013, Texas Instruments Incorporated



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.



*SD must be pulled high through a 10kΩ pull-up resistor. See application hints for more information.

CONNECTION DIAGRAM

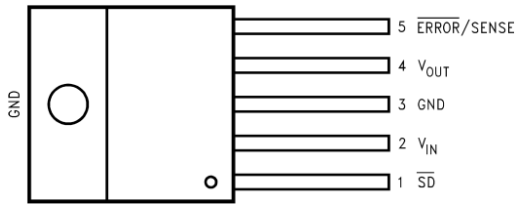


Figure 1. 5-Pin TO-220 (Top View)
See NDH0005D Package

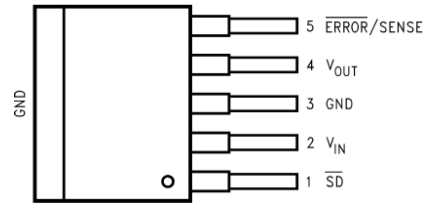


Figure 2. 5-Pin DPAK/TO-263 (Top View)
See KTT Package

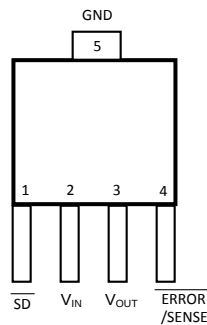


Figure 3. 5-Pin SOT-223 (Top View)
See NDC0005A Package

Table 1. Pin Descriptions for TO-220 and DPAK/TO-263 Packages

Pin #	LP3872		LP3875	
	Name	Function	Name	Function
1	$\overline{\text{SD}}$	Shutdown	$\overline{\text{SD}}$	Shutdown
2	V_{IN}	Input Supply	V_{IN}	Input Supply
3	GND	Ground	GND	Ground
4	V_{OUT}	Output Voltage	V_{OUT}	Output Voltage
5	ERROR	ERROR Flag	SENSE	Remote Sense Pin

Table 2. Pin Descriptions for SOT-223 Package

Pin #	LP3872		LP3875	
	Name	Function	Name	Function
1	$\overline{\text{SD}}$	Shutdown	$\overline{\text{SD}}$	Shutdown
2	V_{IN}	Input Supply	V_{IN}	Input Supply
3	V_{OUT}	Output Voltage	V_{OUT}	Output Voltage
4	ERROR	ERROR Flag	SENSE	Remote Sense Pin

Table 2. Pin Descriptions for SOT-223 Package (continued)

Pin #	LP3872		LP3875	
	Name	Function	Name	Function
5	GND	Ground	GND	Ground

BLOCK DIAGRAM

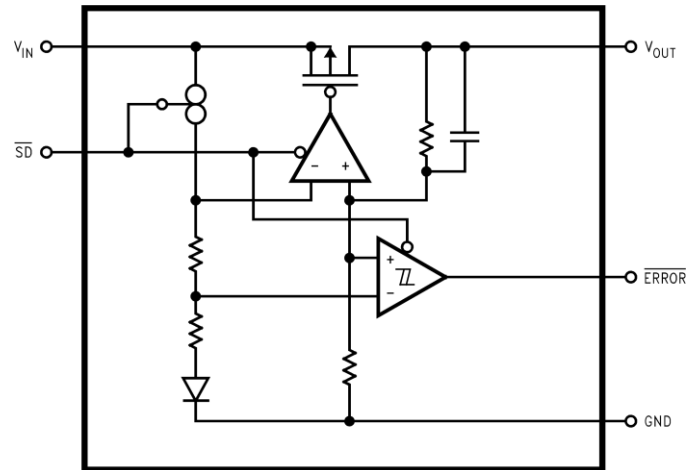


Figure 4. LP3872

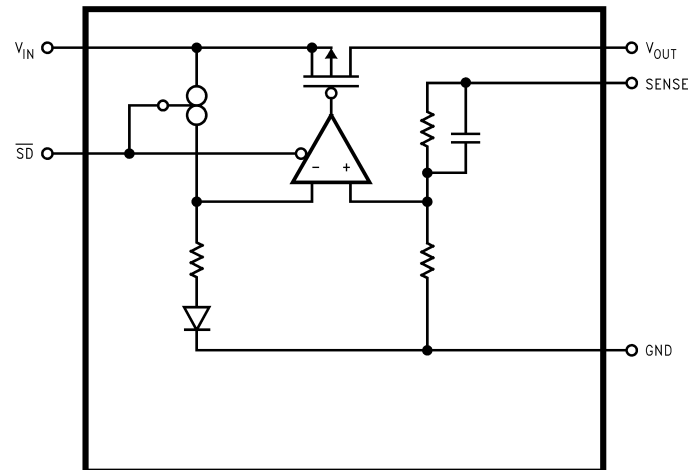


Figure 5. LP3875

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/Distributors for availability and specifications.

	VALUE / UNITS
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering, 5 sec.)	260°C
ESD Rating ⁽²⁾	2 kV
Power Dissipation ⁽³⁾	Internally Limited
Input Supply Voltage (Survival)	–0.3V to +7.5V
Shutdown Input Voltage (Survival)	–0.3V to +7.5V
Output Voltage (Survival), ⁽⁴⁾ , ⁽⁵⁾	–0.3V to +6.0V
I _{OUT} (Survival)	Short Circuit Protected
Maximum Voltage for $\overline{\text{ERROR}}$ Pin	V _{IN}
Maximum Voltage for SENSE Pin	V _{OUT}

- (1) Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions for which the device is intended to be functional, but does not ensure specific performance limits. For specifications and test conditions, see Electrical Characteristics. The specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
- (2) The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.
- (3) At elevated temperatures, devices must be derated based on package thermal resistance. The devices in TO-220 package must be derated at $\theta_{JA} = 50^{\circ}\text{C/W}$ (with 0.5in², 1oz. copper area), junction-to-ambient (with no heat sink). The devices in the DDPAK/TO-263 surface-mount package must be derated at $\theta_{JA} = 60^{\circ}\text{C/W}$ (with 0.5in², 1oz. copper area), junction-to-ambient. The SOT-223 package must be derated at $\theta_{JA} = 90^{\circ}\text{C/W}$ (with 0.5in², 1oz. copper area), junction-to-ambient.
- (4) If used in a dual-supply system where the regulator load is returned to a negative supply, the output must be diode-clamped to ground.
- (5) The output PMOS structure contains a diode between the V_{IN} and V_{OUT} terminals. This diode is normally reverse biased. This diode will get forward biased if the voltage at the output terminal is forced to be higher than the voltage at the input terminal. This diode can typically withstand 200mA of DC current and 1Amp of peak current.

RECOMMENDED OPERATING CONDITIONS

	VALUE / UNITS
Input Supply Voltage ⁽¹⁾	2.5V to 7.0V
Shutdown Input Voltage	–0.3V to 7.0V
Maximum Operating Current (DC)	1.5A
Junction Temperature	–40°C to +125°C

- (1) The minimum operating value for V_{IN} is equal to either [V_{OUT(NOM)} + V_{DROPOUT}] or 2.5V, whichever is greater.

ELECTRICAL CHARACTERISTICS – LP3872/LP3875

Limits in standard typeface are for $T_J = 25^\circ\text{C}$, and limits in **boldface type** apply over the **full operating temperature range**. Unless otherwise specified: $V_{IN} = V_{O(NOM)} + 1\text{V}$, $I_L = 10\text{ mA}$, $C_{OUT} = 10\mu\text{F}$, $V_{SD} = 2\text{V}$.

Symbol	Parameter	Conditions	Typ ⁽¹⁾	LP3872/5 ⁽²⁾		Units
				Min	Max	
V_O	Output Voltage Tolerance ⁽³⁾	$V_{OUT} + 1\text{V} \leq V_{IN} \leq 7.0\text{V}$, $10\text{ mA} \leq I_L \leq 1.5\text{A}$	0	-1.5 -3.0	+1.5 +3.0	%
ΔV_{OL}	Output Voltage Line Regulation ⁽³⁾	$V_{OUT} + 1\text{V} \leq V_{IN} \leq 7.0\text{V}$	0.02 0.06			%
$\Delta V_O / \Delta I_{OUT}$	Output Voltage Load Regulation ⁽³⁾	$10\text{ mA} \leq I_L \leq 1.5\text{A}$	0.06 0.12			%
$V_{IN} - V_{OUT}$	Dropout Voltage ⁽⁴⁾	$I_L = 150\text{ mA}$	38		50 60	mV
		$I_L = 1.5\text{A}$	380		450 550	
I_{GND}	Ground Pin Current In Normal Operation Mode	$I_L = 150\text{ mA}$	5		9 10	mA
		$I_L = 1.5\text{A}$	6		14 15	
I_{GND}	Ground Pin Current In Shutdown Mode	$V_{SD} \leq 0.3\text{V}$	0.01		10	μA
		$-40^\circ\text{C} \leq T_J \leq 85^\circ\text{C}$			50	
$I_{O(PK)}$	Peak Output Current	$V_O \geq V_{O(NOM)} - 4\%$	1.8			A
Short Circuit Protection						
I_{SC}	Short Circuit Current		3.2			A
Shutdown Input						
V_{SDT}	Shutdown Threshold	Output = High	V_{IN}	2		V
		Output = Low	0		0.3	
T_{dOFF}	Turn-off delay	$I_L = 1.5\text{A}$	20			μs
T_{dON}	Turn-on delay	$I_L = 1.5\text{A}$	25			μs
I_{SD}	$\overline{\text{SD}}$ Input Current	$V_{SD} = V_{IN}$	1			nA
Error Flag						
V_T	Threshold	See ⁽⁵⁾	10	5	16	%
V_{TH}	Threshold Hysteresis	See ⁽⁵⁾	5	2	8	%
$V_{EF(Sat)}$	Error Flag Saturation	$I_{sink} = 100\mu\text{A}$	0.02		0.1	V
T_d	Flag Reset Delay		1			μs
I_{lk}	Error Flag Pin Leakage Current		1			nA
I_{max}	Error Flag Pin Sink Current	$V_{Error} = \mathbf{0.5V}$	1			mA
AC Parameters						
PSRR	Ripple Rejection	$V_{IN} = V_{OUT} + 1\text{V}$, $C_{OUT} = 10\mu\text{F}$ $V_{OUT} = 3.3\text{V}$, $f = 120\text{Hz}$	73			dB
		$V_{IN} = V_{OUT} + 0.5\text{V}$, $C_{OUT} = 10\mu\text{F}$ $V_{OUT} = 3.3\text{V}$, $f = 120\text{Hz}$	57			
$\rho_{n(f)}$	Output Noise Density	$f = 120\text{Hz}$	0.8			μV
e_n	Output Noise Voltage	$\text{BW} = 10\text{Hz} - 100\text{kHz}$, $V_{OUT} = 2.5\text{V}$	150			μV (rms)
		$\text{BW} = 300\text{Hz} - 300\text{kHz}$, $V_{OUT} = 2.5\text{V}$	100			

(1) Typical numbers are at 25°C and represent the most likely parametric norm.

(2) Limits are specified by testing, design, or statistical correlation.

(3) Output voltage line regulation is defined as the change in output voltage from the nominal value due to change in the input line voltage. Output voltage load regulation is defined as the change in output voltage from the nominal value due to change in load current. The line and load regulation specification contains only the typical number. However, the limits for line and load regulation are included in the output voltage tolerance specification.

(4) Dropout voltage is defined as the minimum input to output differential voltage at which the output drops 2% below the nominal value. Dropout voltage specification applies only to output voltages of 2.5V and above. For output voltages below 2.5V, the drop-out voltage is nothing but the input to output differential, since the minimum input voltage is 2.5V.

(5) Error Flag threshold and hysteresis are specified as percentage of regulated output voltage. See Application Hints.

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified: $T_J = 25^\circ\text{C}$, $C_{OUT} = 10\mu\text{F}$, $C_{IN} = 10\mu\text{F}$, S/D pin is tied to V_{IN} , $V_{OUT} = 2.5\text{V}$, $V_{IN} = V_{O(NOM)} + 1\text{V}$, $I_L = 10\text{mA}$

Dropout Voltage vs Output Load Current

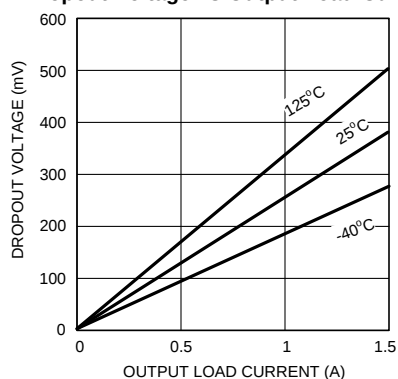


Figure 6.

Ground Current vs Output Voltage
 $I_L = 1.5\text{A}$

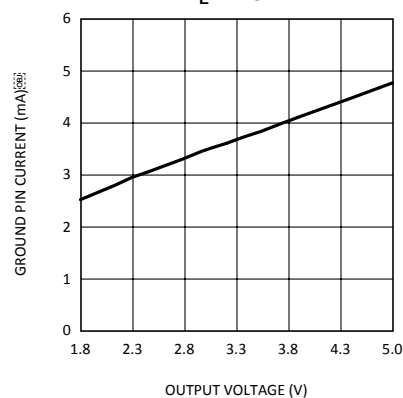


Figure 7.

Shutdown I_Q vs Junction Temperature

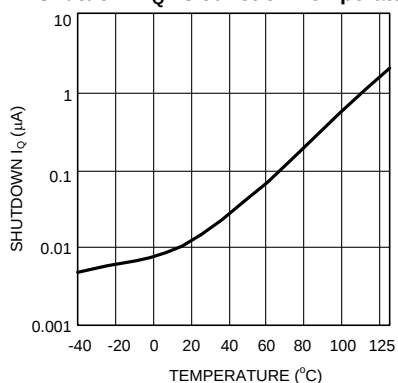


Figure 8.

Errorflag Threshold vs Junction Temperature

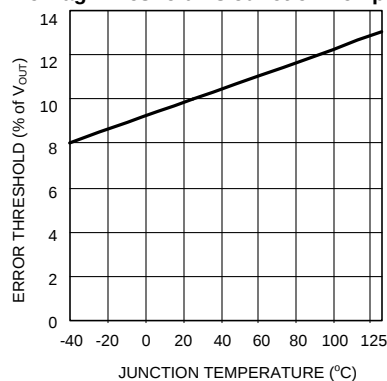


Figure 9.

DC Load Reg. vs Junction Temperature

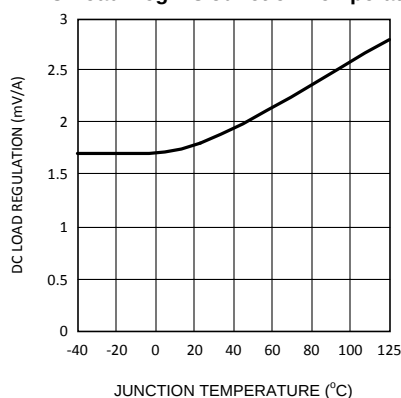


Figure 10.

DC Line Regulation vs Temperature

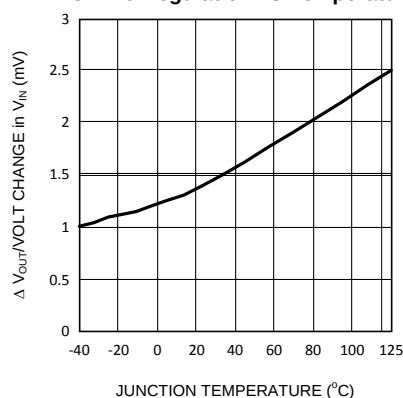


Figure 11.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: $T_J = 25^\circ\text{C}$, $C_{OUT} = 10\mu\text{F}$, $C_{IN} = 10\mu\text{F}$, S/D pin is tied to V_{IN} , $V_{OUT} = 2.5\text{V}$, $V_{IN} = V_{O(NOM)} + 1\text{V}$, $I_L = 10\text{mA}$

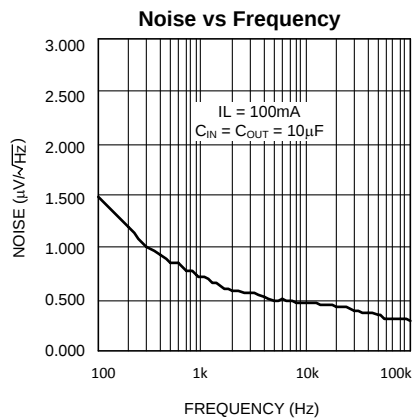


Figure 12.

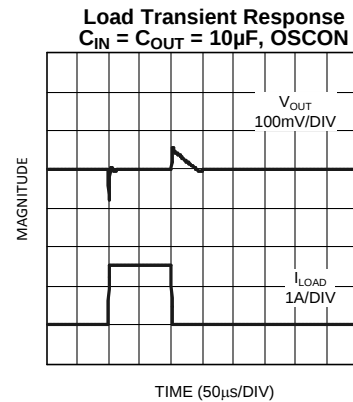


Figure 13.

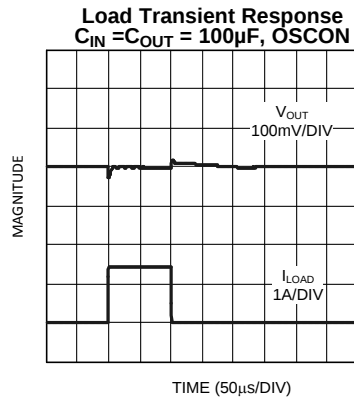


Figure 14.

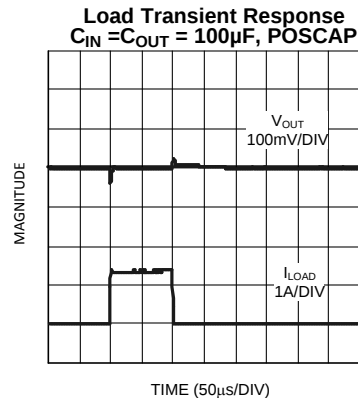


Figure 15.

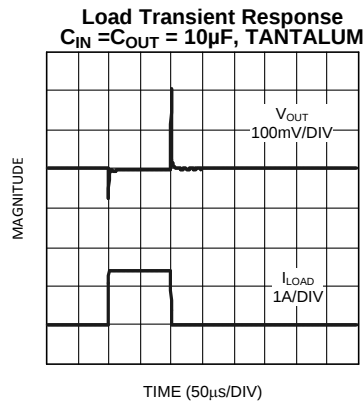


Figure 16.

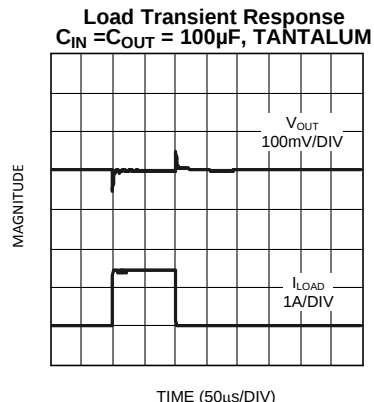


Figure 17.

Application Hints

EXTERNAL CAPACITORS

Like any low-dropout regulator, external capacitors are required to assure stability. These capacitors must be correctly selected for proper performance.

INPUT CAPACITOR: An input capacitor of at least 10 μ F is required. Ceramic, Tantalum, or Electrolytic capacitors may be used, and capacitance may be increased without limit

OUTPUT CAPACITOR: An output capacitor is required for loop stability. It must be located less than 1 cm from the device and connected directly to the output and ground pins using traces which have no other currents flowing through them (see PCB Layout section).

The minimum value of output capacitance that can be used for stable full-load operation is 10 μ F, but it may be increased without limit. The output capacitor must have an ESR value as shown in the stable region of the curve below. Tantalum capacitors are recommended for the output capacitor.

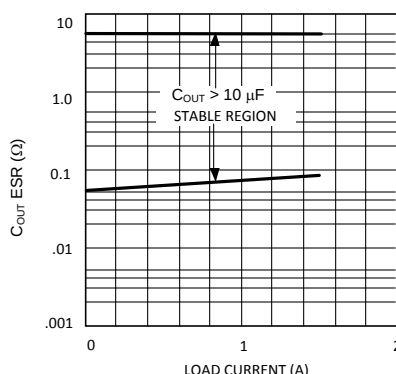


Figure 18. ESR Curve

SELECTING A CAPACITOR

It is important to note that capacitance tolerance and variation with temperature must be taken into consideration when selecting a capacitor so that the minimum required amount of capacitance is provided over the full operating temperature range. In general, a good Tantalum capacitor will show very little capacitance variation with temperature, but a ceramic may not be as good (depending on dielectric type). Aluminum electrolytics also typically have large temperature variation of capacitance value.

Equally important to consider is a capacitor's ESR change with temperature: this is not an issue with ceramics, as their ESR is extremely low. However, it is very important in Tantalum and aluminum electrolytic capacitors. Both show increasing ESR at colder temperatures, but the increase in aluminum electrolytic capacitors is so severe they may not be feasible for some applications (see Capacitor Characteristics Section).

CAPACITOR CHARACTERISTICS

CERAMIC: For values of capacitance in the 10 to 100 μ F range, ceramics are usually larger and more costly than tantalums but give superior AC performance for bypassing high frequency noise because of very low ESR (typically less than 10 m Ω). However, some dielectric types do not have good capacitance characteristics as a function of voltage and temperature.

Z5U and Y5V dielectric ceramics have capacitance that drops severely with applied voltage. A typical Z5U or Y5V capacitor can lose 60% of its rated capacitance with half of the rated voltage applied to it. The Z5U and Y5V also exhibit a severe temperature effect, losing more than 50% of nominal capacitance at high and low limits of the temperature range.

X7R and X5R dielectric ceramic capacitors are strongly recommended if ceramics are used, as they typically maintain a capacitance range within $\pm 20\%$ of nominal over full operating ratings of temperature and voltage. Of course, they are typically larger and more costly than Z5U/Y5U types for a given voltage and capacitance.

TANTALUM: Solid Tantalum capacitors are recommended for use on the output because their typical ESR is very close to the ideal value required for loop compensation. They also work well as input capacitors if selected to meet the ESR requirements previously listed.

Tantalums also have good temperature stability: a good quality Tantalum will typically show a capacitance value that varies less than 10-15% across the full temperature range of 125°C to –40°C. ESR will vary only about 2X going from the high to low temperature limits.

The increasing ESR at lower temperatures can cause oscillations when marginal quality capacitors are used (if the ESR of the capacitor is near the upper limit of the stability range at room temperature).

ALUMINUM: This capacitor type offers the most capacitance for the money. The disadvantages are that they are larger in physical size, not widely available in surface mount, and have poor AC performance (especially at higher frequencies) due to higher ESR and ESL.

Compared by size, the ESR of an aluminum electrolytic is higher than either Tantalum or ceramic, and it also varies greatly with temperature. A typical aluminum electrolytic can exhibit an ESR increase of as much as 50X when going from 25°C down to –40°C.

It should also be noted that many aluminum electrolytics only specify impedance at a frequency of 120 Hz, which indicates they have poor high frequency performance. Only aluminum electrolytics that have an impedance specified at a higher frequency (between 20 kHz and 100 kHz) should be used for the LP387X. Derating must be applied to the manufacturer's ESR specification, since it is typically only valid at room temperature.

Any applications using aluminum electrolytics should be thoroughly tested at the lowest ambient operating temperature where ESR is maximum.

TURN-ON CHARACTERISTICS FOR OUTPUT VOLTAGES PROGRAMMED TO 2.0V OR BELOW

As V_{in} increases during start-up, the regulator output will track the input until V_{in} reaches the minimum operating voltage (typically about 2.2V). For output voltages programmed to 2.0V or below, the regulator output may momentarily exceed its programmed output voltage during start up. Outputs programmed to voltages above 2.0V are not affected by this behavior.

PCB LAYOUT

Good PC layout practices must be used or instability can be induced because of ground loops and voltage drops. The input and output capacitors must be directly connected to the input, output, and ground pins of the regulator using traces which do not have other currents flowing in them (Kelvin connect).

The best way to do this is to lay out C_{IN} and C_{OUT} near the device with short traces to the V_{IN} , V_{OUT} , and ground pins. The regulator ground pin should be connected to the external circuit ground so that the regulator and its capacitors have a "single point ground".

It should be noted that stability problems have been seen in applications where "vias" to an internal ground plane were used at the ground points of the IC and the input and output capacitors. This was caused by varying ground potentials at these nodes resulting from current flowing through the ground plane. Using a single point ground technique for the regulator and its capacitors fixed the problem.

Since high current flows through the traces going into V_{IN} and coming from V_{OUT} , Kelvin connect the capacitor leads to these pins so there is no voltage drop in series with the input and output capacitors.

RFI/EMI SUSCEPTIBILITY

RFI (radio frequency interference) and EMI (electromagnetic interference) can degrade any integrated circuit's performance because of the small dimensions of the geometries inside the device. In applications where circuit sources are present which generate signals with significant high frequency energy content (> 1 MHz), care must be taken to ensure that this does not affect the IC regulator.

If RFI/EMI noise is present on the input side of the regulator (such as applications where the input source comes from the output of a switching regulator), good ceramic bypass capacitors must be used at the input pin of the IC.

If a load is connected to the IC output which switches at high speed (such as a clock), the high-frequency current pulses required by the load must be supplied by the capacitors on the IC output. Since the bandwidth of the regulator loop is less than 100 kHz, the control circuitry cannot respond to load changes above that frequency. This means the effective output impedance of the IC at frequencies above 100 kHz is determined only by the output capacitor(s).

In applications where the load is switching at high speed, the output of the IC may need RF isolation from the load. It is recommended that some inductance be placed between the output capacitor and the load, and good RF bypass capacitors be placed directly across the load.

PCB layout is also critical in high noise environments, since RFI/EMI is easily radiated directly into PC traces. Noisy circuitry should be isolated from "clean" circuits where possible, and grounded through a separate path. At MHz frequencies, ground planes begin to look inductive and RFI/EMI can cause ground bounce across the ground plane.

In multi-layer PCB applications, care should be taken in layout so that noisy power and ground planes do not radiate directly into adjacent layers which carry analog power and ground.

OUTPUT NOISE

Noise is specified in two ways-

Spot Noise or **Output noise density** is the RMS sum of all noise sources, measured at the regulator output, at a specific frequency (measured with a 1Hz bandwidth). This type of noise is usually plotted on a curve as a function of frequency.

Total output Noise or **Broad-band noise** is the RMS sum of spot noise over a specified bandwidth, usually several decades of frequencies.

Attention should be paid to the units of measurement. Spot noise is measured in units $\mu\text{V}/\sqrt{\text{Hz}}$ or $\text{nV}/\sqrt{\text{Hz}}$ and total output noise is measured in $\mu\text{V}(\text{rms})$.

The primary source of noise in low-dropout regulators is the internal reference. In CMOS regulators, noise has a low frequency component and a high frequency component, which depend strongly on the silicon area and quiescent current. Noise can be reduced in two ways: by increasing the transistor area or by increasing the current drawn by the internal reference. Increasing the area will decrease the chance of fitting the die into a smaller package. Increasing the current drawn by the internal reference increases the total supply current (ground pin current). Using an optimized trade-off of ground pin current and die size, LP3872/LP3875 achieves low noise performance and low quiescent current operation.

The total output noise specification for LP3872/LP3875 is presented in the Electrical Characteristics table. The Output noise density at different frequencies is represented by a curve under typical performance characteristics.

SHORT-CIRCUIT PROTECTION

The LP3872 and LP3875 are short circuit protected and in the event of a peak over-current condition, the short-circuit control loop will rapidly drive the output PMOS pass element off. Once the power pass element shuts down, the control loop will rapidly cycle the output on and off until the average power dissipation causes the thermal shutdown circuit to respond to servo the on/off cycling to a lower frequency. Please refer to the section on thermal information for power dissipation calculations.

ERROR FLAG OPERATION

The LP3872/LP3875 produces a logic low signal at the $\overline{\text{Error}}$ Flag pin when the output drops out of regulation due to low input voltage, current limiting, or thermal limiting. This flag has a built in hysteresis. The timing diagram in [Figure 19](#) shows the relationship between the ERROR flag and the output voltage. In this example, the input voltage is changed to demonstrate the functionality of the Error Flag.

The internal $\overline{\text{Error}}$ flag comparator has an open drain output stage. Hence, the $\overline{\text{ERROR}}$ pin should be pulled high through a pull up resistor. Although the $\overline{\text{ERROR}}$ flag pin can sink current of 1mA, this current is energy drain from the input supply. Hence, the value of the pull up resistor should be in the range of 10k Ω to 1M Ω . **The $\overline{\text{ERROR}}$ pin must be connected to ground if this function is not used.** It should also be noted that when the shutdown pin is pulled low, the ERROR pin is forced to be invalid for reasons of saving power in shutdown mode.

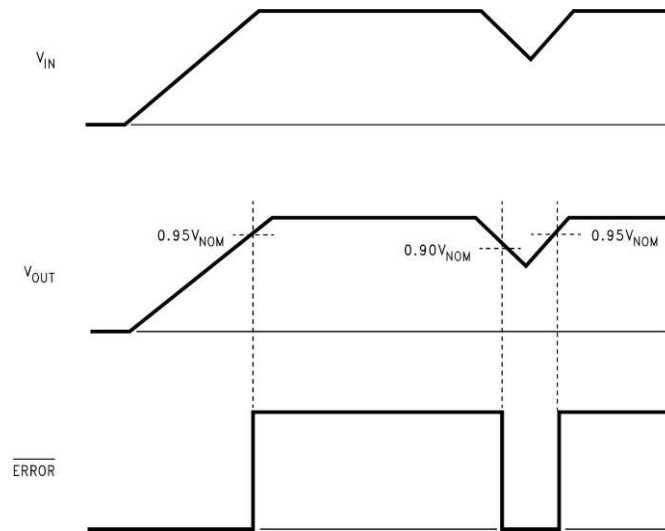


Figure 19. Error Flag Operation

SENSE PIN

In applications where the regulator output is not very close to the load, LP3875 can provide better remote load regulation using the SENSE pin. Figure 20 depicts the advantage of the SENSE option. LP3872 regulates the voltage at the output pin. Hence, the voltage at the remote load will be the regulator output voltage minus the drop across the trace resistance. For example, in the case of a 3.3V output, if the trace resistance is 100mΩ, the voltage at the remote load will be 3.15V with 1.5A of load current, I_{LOAD} . The LP3875 regulates the voltage at the sense pin. Connecting the sense pin to the remote load will provide regulation at the remote load, as shown in Figure 20. If the sense option pin is not required, the sense pin must be connected to the V_{OUT} pin.

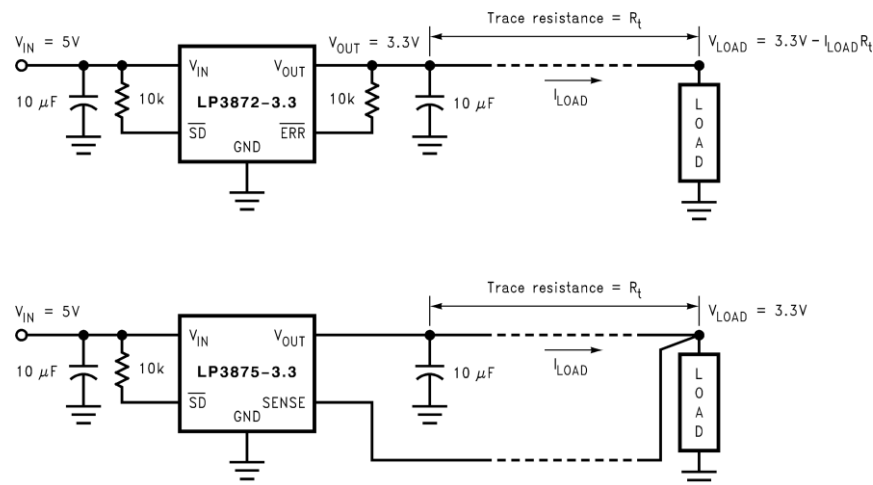


Figure 20. Improving Remote Load Regulation Using LP3875

SHUTDOWN OPERATION

A CMOS Logic level signal at the shutdown ($\overline{SD}$) pin will turn-off the regulator. Pin $\overline{SD}$ must be actively terminated through a 10kΩ pull-up resistor for a proper operation. If this pin is driven from a source that actively pulls high and low (such as a CMOS rail to rail comparator), the pull-up resistor is not required. This pin must be tied to V_{IN} if not used.

DROPOUT VOLTAGE

The dropout voltage of a regulator is defined as the minimum input-to-output differential required to stay within 2% of the nominal output voltage. For CMOS LDOs, the dropout voltage is the product of the load current and the $R_{ds(on)}$ of the internal MOSFET.

REVERSE CURRENT PATH

The internal MOSFET in LP3872 and LP3875 has an inherent parasitic diode. During normal operation, the input voltage is higher than the output voltage and the parasitic diode is reverse biased. However, if the output is pulled above the input in an application, then current flows from the output to the input as the parasitic diode gets forward biased. The output can be pulled above the input as long as the current in the parasitic diode is limited to 200mA continuous and 1A peak.

POWER DISSIPATION/HEATSINKING

LP3872 and LP3875 can deliver a continuous current of 1.5A over the full operating temperature range. A heatsink may be required depending on the maximum power dissipation and maximum ambient temperature of the application. Under all possible conditions, the junction temperature must be within the range specified under operating conditions. The total power dissipation of the device is given by:

$$P_D = (V_{IN} - V_{OUT})I_{OUT} + (V_{IN})I_{GND}$$

where I_{GND} is the operating ground current of the device (specified under Electrical Characteristics).

The maximum allowable temperature rise (T_{Rmax}) depends on the maximum ambient temperature (T_{Amax}) of the application, and the maximum allowable junction temperature (T_{Jmax}): $T_{Rmax} = T_{Jmax} - T_{Amax}$

The maximum allowable value for junction to ambient Thermal Resistance, θ_{JA} , can be calculated using the formula:

$$\theta_{JA} = T_{Rmax} / P_D$$

LP3872 and LP3875 are available in TO-220 and DDPAK/TO-263 packages. The thermal resistance depends on amount of copper area or heat sink, and on air flow. If the maximum allowable value of θ_{JA} calculated above is ≥ 60 °C/W for TO-220 package and ≥ 60 °C/W for DDPAK/TO-263 package no heatsink is needed since the package can dissipate enough heat to satisfy these requirements. If the value for allowable θ_{JA} falls below these limits, a heat sink is required.

HEATSINKING TO-220 PACKAGE

The thermal resistance of a TO-220 package can be reduced by attaching it to a heat sink or a copper plane on a PC board. If a copper plane is to be used, the values of θ_{JA} will be same as shown in next section for DDPAK/TO-263 package.

The heatsink to be used in the application should have a heatsink to ambient thermal resistance, $\theta_{HA} \leq \theta_{JA} - \theta_{CH} - \theta_{JC}$.

In this equation, θ_{CH} is the thermal resistance from the case to the surface of the heat sink and θ_{JC} is the thermal resistance from the junction to the surface of the case. θ_{JC} is about 3°C/W for a TO-220 package. The value for θ_{CH} depends on method of attachment, insulator, etc. θ_{CH} varies between 1.5°C/W to 2.5°C/W. If the exact value is unknown, 2°C/W can be assumed.

HEATSINKING DDPAK/TO-263 PACKAGE

The DDPAK/TO-263 package uses the copper plane on the PCB as a heatsink. The tab of these packages are soldered to the copper plane for heat sinking. [Figure 21](#) shows a curve for the θ_{JA} of DDPAK/TO-263 package for different copper area sizes, using a typical PCB with 1 ounce copper and no solder mask over the copper area for heat sinking.

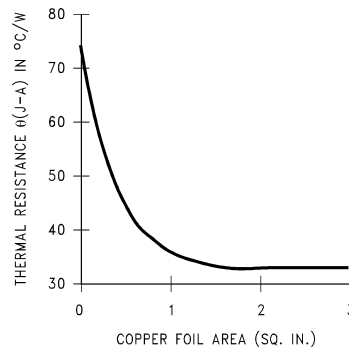


Figure 21. θ_{JA} vs Copper (1 Ounce) Area for DDPAK/TO-263 package

As shown in the figure, increasing the copper area beyond 1 square inch produces very little improvement. The minimum value for θ_{JA} for the DDPAK/TO-263 package mounted to a PCB is 32°C/W.

Figure 22 shows the maximum allowable power dissipation for DDPAK/TO-263 packages for different ambient temperatures, assuming θ_{JA} is 35°C/W and the maximum junction temperature is 125°C.

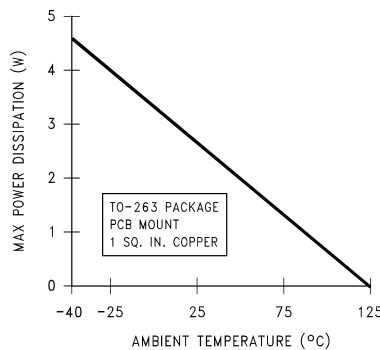


Figure 22. Maximum power dissipation vs ambient temperature for DDPAK/TO-263 package

HEATSINKING SOT-223 PACKAGE

Figure 23 shows a curve for the θ_{JA} of SOT-223 package for different copper area sizes, using a typical PCB with 1 ounce copper and no solder mask over the copper area for heat sinking.

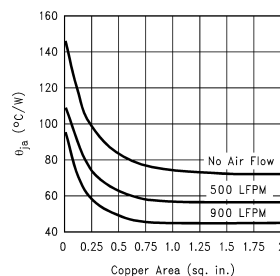


Figure 23. θ_{JA} vs Copper(1 Ounce) Area for SOT-223 package

The following figures show different layout scenarios for SOT-223 package.

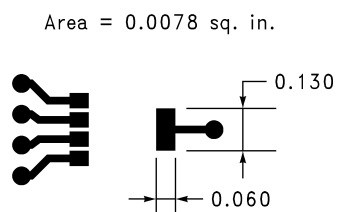


Figure 24. SCENARIO A, $\theta_{JA} = 148^{\circ}\text{C/W}$

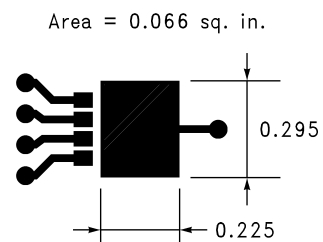


Figure 25. SCENARIO B, $\theta_{JA} = 125^{\circ}\text{C/W}$

REVISION HISTORY

Changes from Revision E (April 2013) to Revision F

Page

- Changed layout of National Data Sheet to TI format [13](#)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LP3872EMP-1.8	ACTIVE	SOT-223	NDC	5	1000	TBD	Call TI	Call TI	-40 to 125	LHAB	Samples
LP3872EMP-1.8/NOPB	ACTIVE	SOT-223	NDC	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LHAB	Samples
LP3872EMP-2.5	ACTIVE	SOT-223	NDC	5	1000	TBD	Call TI	Call TI	-40 to 125	LHBB	Samples
LP3872EMP-2.5/NOPB	ACTIVE	SOT-223	NDC	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LHBB	Samples
LP3872EMP-3.3	ACTIVE	SOT-223	NDC	5	1000	TBD	Call TI	Call TI	-40 to 125	LHCB	Samples
LP3872EMP-3.3/NOPB	ACTIVE	SOT-223	NDC	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LHCB	Samples
LP3872EMP-5.0	ACTIVE	SOT-223	NDC	5	1000	TBD	Call TI	Call TI	-40 to 125	LHDB	Samples
LP3872EMP-5.0/NOPB	ACTIVE	SOT-223	NDC	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LHDB	Samples
LP3872EMPX-2.5	ACTIVE	SOT-223	NDC	5	2000	TBD	Call TI	Call TI	-40 to 125	LHBB	Samples
LP3872EMPX-2.5/NOPB	ACTIVE	SOT-223	NDC	5	2000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LHBB	Samples
LP3872EMPX-3.3	ACTIVE	SOT-223	NDC	5	2000	TBD	Call TI	Call TI	-40 to 125	LHCB	Samples
LP3872EMPX-3.3/NOPB	ACTIVE	SOT-223	NDC	5	2000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LHCB	Samples
LP3872ES-1.8	ACTIVE	DDPAK/ TO-263	KTT	5	45	TBD	Call TI	Call TI	-40 to 125	LP3872ES -1.8	Samples
LP3872ES-1.8/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LP3872ES -1.8	Samples
LP3872ES-2.5	ACTIVE	DDPAK/ TO-263	KTT	5	45	TBD	Call TI	Call TI	-40 to 125	LP3872ES -2.5	Samples
LP3872ES-2.5/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LP3872ES -2.5	Samples
LP3872ES-3.3	ACTIVE	DDPAK/ TO-263	KTT	5	45	TBD	Call TI	Call TI	-40 to 125	LP3872ES -3.3	Samples
LP3872ES-3.3/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LP3872ES -3.3	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LP3872ES-5.0	ACTIVE	DDPAK/ TO-263	KTT	5	45	TBD	Call TI	Call TI	-40 to 125	LP3872ES -5.0	Samples
LP3872ES-5.0/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LP3872ES -5.0	Samples
LP3872ESX-1.8	ACTIVE	DDPAK/ TO-263	KTT	5	500	TBD	Call TI	Call TI	-40 to 125	LP3872ES -1.8	Samples
LP3872ESX-1.8/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LP3872ES -1.8	Samples
LP3872ESX-2.5	ACTIVE	DDPAK/ TO-263	KTT	5	500	TBD	Call TI	Call TI	-40 to 125	LP3872ES -2.5	Samples
LP3872ESX-2.5/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LP3872ES -2.5	Samples
LP3872ESX-3.3	ACTIVE	DDPAK/ TO-263	KTT	5	500	TBD	Call TI	Call TI	-40 to 125	LP3872ES -3.3	Samples
LP3872ESX-3.3/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LP3872ES -3.3	Samples
LP3872ESX-5.0	ACTIVE	DDPAK/ TO-263	KTT	5	500	TBD	Call TI	Call TI	-40 to 125	LP3872ES -5.0	Samples
LP3872ESX-5.0/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LP3872ES -5.0	Samples
LP3875EMP-1.8	ACTIVE	SOT-223	NDC	5	1000	TBD	Call TI	Call TI	-40 to 125	LHLB	Samples
LP3875EMP-1.8/NOPB	ACTIVE	SOT-223	NDC	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LHLB	Samples
LP3875EMP-2.5	ACTIVE	SOT-223	NDC	5	1000	TBD	Call TI	Call TI	-40 to 125	LHNB	Samples
LP3875EMP-2.5/NOPB	ACTIVE	SOT-223	NDC	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LHNB	Samples
LP3875EMP-3.3	ACTIVE	SOT-223	NDC	5	1000	TBD	Call TI	Call TI	-40 to 125	LHPB	Samples
LP3875EMP-3.3/NOPB	ACTIVE	SOT-223	NDC	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LHPB	Samples
LP3875EMP-5.0	ACTIVE	SOT-223	NDC	5	1000	TBD	Call TI	Call TI	-40 to 125	LHRB	Samples
LP3875EMP-5.0/NOPB	ACTIVE	SOT-223	NDC	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LHRB	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LP3875ES-1.8	ACTIVE	DDPAK/ TO-263	KTT	5	45	TBD	Call TI	Call TI	-40 to 125	LP3875ES -1.8	Samples
LP3875ES-1.8/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LP3875ES -1.8	Samples
LP3875ES-2.5	ACTIVE	DDPAK/ TO-263	KTT	5	45	TBD	Call TI	Call TI	-40 to 125	LP3875ES -2.5	Samples
LP3875ES-2.5/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LP3875ES -2.5	Samples
LP3875ES-3.3	ACTIVE	DDPAK/ TO-263	KTT	5	45	TBD	Call TI	Call TI	-40 to 125	LP3875ES -3.3	Samples
LP3875ES-3.3/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LP3875ES -3.3	Samples
LP3875ESX-1.8	ACTIVE	DDPAK/ TO-263	KTT	5	500	TBD	Call TI	Call TI	-40 to 125	LP3875ES -1.8	Samples
LP3875ESX-1.8/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LP3875ES -1.8	Samples
LP3875ESX-2.5	ACTIVE	DDPAK/ TO-263	KTT	5	500	TBD	Call TI	Call TI	-40 to 125	LP3875ES -2.5	Samples
LP3875ESX-2.5/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LP3875ES -2.5	Samples
LP3875ESX-3.3	ACTIVE	DDPAK/ TO-263	KTT	5	500	TBD	Call TI	Call TI	-40 to 125	LP3875ES -3.3	Samples
LP3875ESX-3.3/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LP3875ES -3.3	Samples
LP3875ET-3.3	ACTIVE	TO-220	NDH	5	45	TBD	Call TI	Call TI	-40 to 125	LP3875ET -3.3	Samples
LP3875ET-3.3/NOPB	ACTIVE	TO-220	NDH	5	45	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 125	LP3875ET -3.3	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

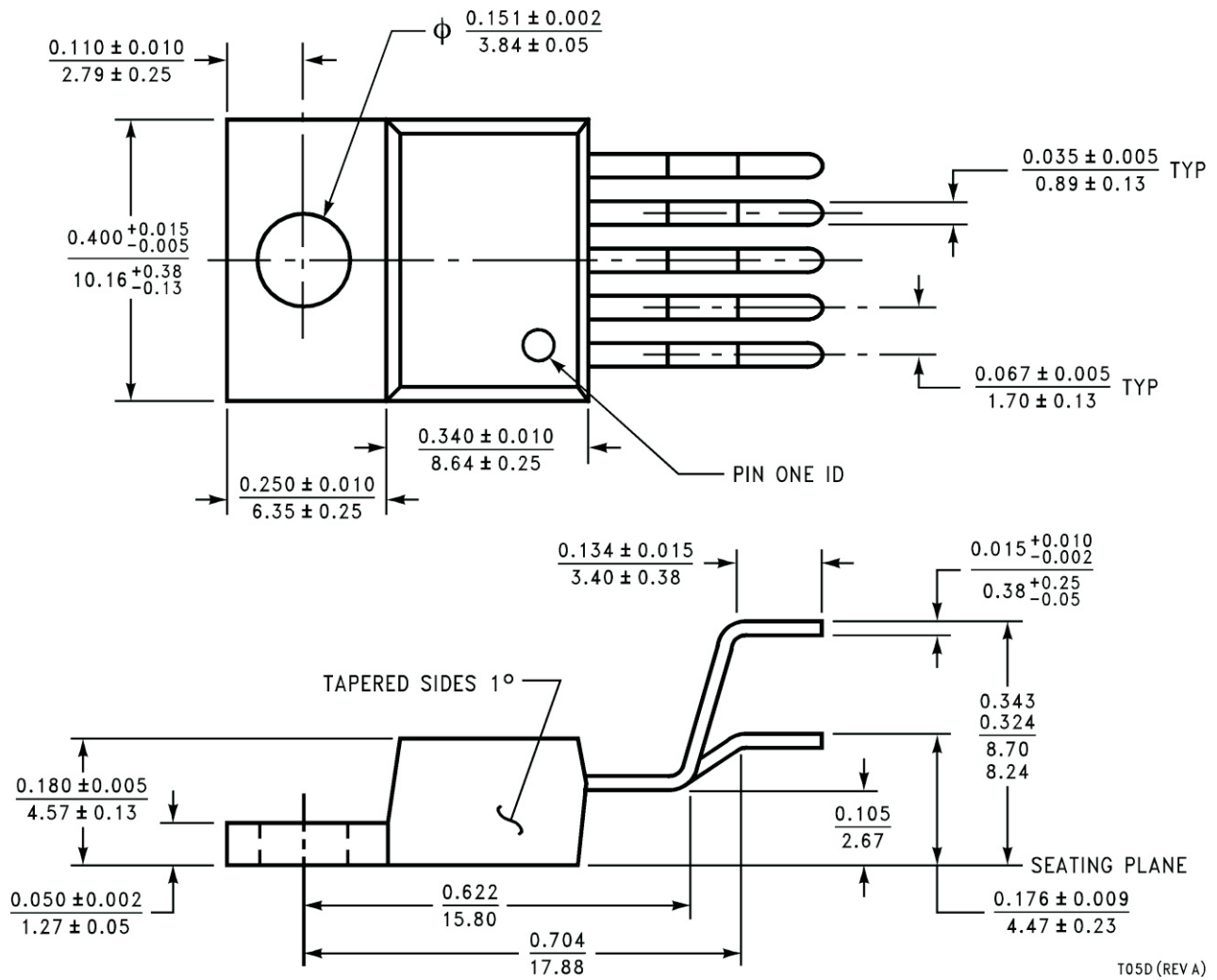
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

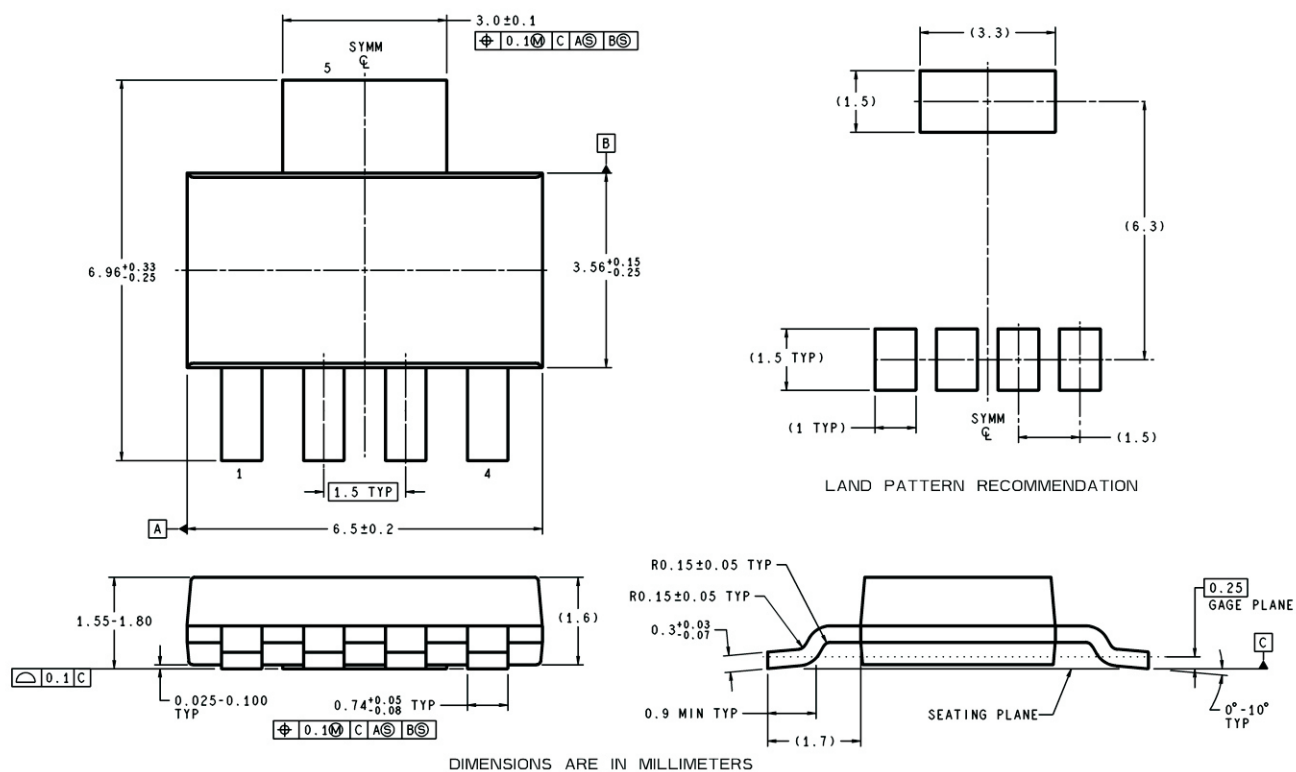
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

NDH0005D



NDC0005A



MP05A (Rev A)

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com