LP3991

LP3991 300mA Linear Voltage Regulator for Digital Applications

Literature Number: SNVS296G

National Semiconductor

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LP3991

300mA Linear Voltage Regulator for Digital Applications

General Description

Operating from a minimum input voltage of 1.65V, the LP3991 regulator has been designed to provide fixed stable output voltages for load currents up to 300mA. This device is suitable where accurate, low voltages are required from low input voltage sources and is therefore suitable for post regulation of switched mode regulators. In such applications, significant improvements in performance and EMI can be realized, with little reduction in overall efficiency. The LP3991 will provide fixed outputs as low as 1.2V from a wide input range of 1.65V to 4.0V Using the enable pin, the device may be controlled to provide a shutdown state, in which negligible supply current is drawn.

The LP3991 is designed to be stable with space saving ceramic capacitors as small as 0402 case size.

Performance is specified for a -40°C to 125°C junction temperature range.

For output voltage options please contact your local NSC sales office.

Features

- Operation from 1.65V to 4.0V Input
- 1% accuracy at room temperature
- Output Voltage from 1.2V to 2.8V
- 125mV Dropout at 300mA load
- 50µA Quiescent Current at 1mA Load
- Inrush Current controlled to 600mA
- PSRR 65dB at 1kHz
- 100µs Start-Up time for 1.5V V_{OUT}
- Stable with Ceramic Capacitors as small as 0402
- Thermal-Overload and Short-Circuit Protection

Package

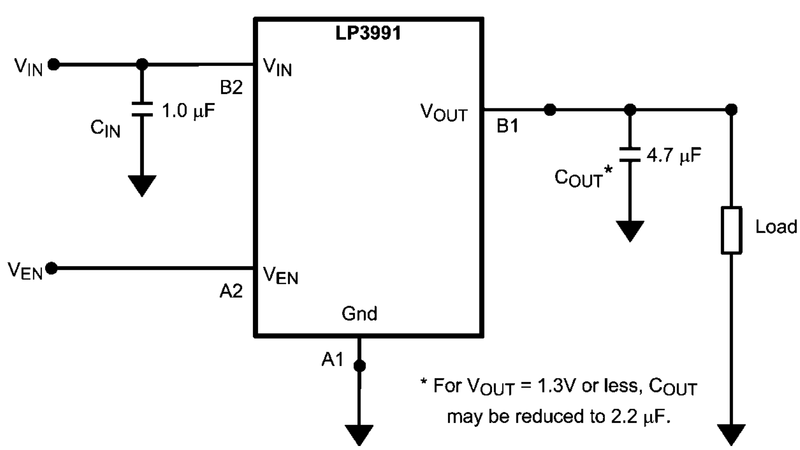
4 pin micro SMD (0.963mm x 1.446mm)

For other package options contact your NSC sales office.

Applications

- Post DC/DC Regulator
- Battery Operated Devices
- Hand-Held Information Appliances

Typical Application Circuit



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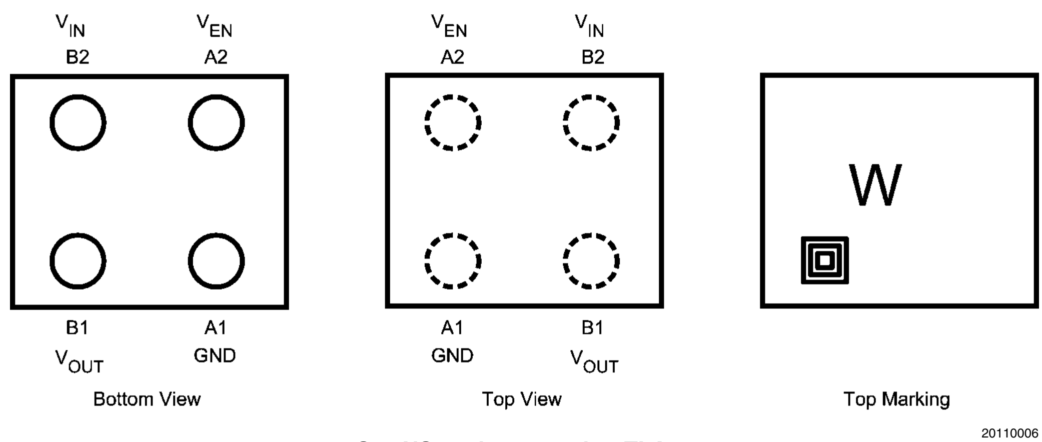
Pin Descriptions

Packages

Pin No.	Symbol	Name and Function
B1	V_{OUT}	Voltage output. A Low ESR Ceramic Capacitor should be connected from this pin to GND. (See Application Information) Connect this output to the load circuit.
A1	GND	Common Ground. Connect to Pad.
A2	V_{EN}	Enable Input; Enables the Regulator when ≥ 0.95V. Disables the Regulator when ≤ 0.4V. Enable Input has an internal 1.2MΩ pull-down resistor to GND.
B2	V_{IN}	Voltage Supply Input. A 1.0µF capacitor should be connected from this pin to GND.

Connection Diagram

4 Bump Thin Micro SMD, Large Bump



See NS package number TLA04

Ordering Information (4-Bump Micro SMD)

Only available as Lead Free.

Output Voltage (V)	Grade	LP3991 Supplied as 250 Units, Tape and Reel	LP3991 Supplied as 3000 Units, Tape and Reel
0.8	STD	LP3991TL-0.8	LP3991TLX-0.8
1.2	STD	LP3991TL-1.2	LP3991TLX-1.2
1.3	STD	LP3991TL-1.3	LP3991TLX-1.3
1.5	STD	LP3991TL-1.5	LP3991TLX-1.5
1.55	STD	LP3991TL-1.55	LP3991TLX-1.55
1.7	STD	LP3991TL-1.7	LP3991TLX-1.7
1.8	STD	LP3991TL-1.8	LP3991TLX-1.8
2.0	STD	LP3991TL-2.0	LP3991TLX-2.0
2.5	STD	LP3991TL-2.5	LP3991TLX-2.5
2.8	STD	LP3991TL-2.8	LP3991TLX-2.8
3.0	STD	LP3991TL-3.0	LP3991TLX-3.0

* Contact your local NSC Sales Office for availability

Absolute Maximum Ratings

(Note 1, Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{IN}, V_{OUT}, Pins: Voltage to GND	-0.3 to 6.5V
V_{EN} Pin: Voltage to GND	-0.3 to (V_{IN} + 0.3V) to 6.5V (max)
Junction Temperature	150°C
Lead/Pad Temp. (Note 3)	
Micro SMD	260°C
Storage Temperature	-65 to 150°C
Continuous Power Dissipation (Note 4)	Internally Limited
ESD (Note 5)	
Human Body Model	2KV
Machine Model	200V

Operating Ratings (Note 1)

Input Voltage Range	1.65 to 4.0V
Recommended Load Current	300mA
Junction Temperature	-40°C to 125°C
Ambient Temperature T_ARange (Note 6)	-40°C to 85°C

Thermal Properties (Note 1)

Junction To Ambient Thermal Resistance(Note 7)	
θ_{JA} JEDEC Board (Note 8)	88°C/W
θ_{JA} 4 Layer Board	160°C/W

Electrical Characteristics

Unless otherwise noted, V_{EN} =950mV, V_{IN} = V_{OUT} + 0.5V, or 1.8V, whichever is higher. C_{IN} = 1µF, I_{OUT} = 1.0mA, C_{OUT} =4.7µF.

Typical values and limits appearing in normal type apply for T_A = 25°C. Limits appearing in **boldface** type apply over the full junction temperature range for operation, –40 to +125°C. (Note 9)

Symbol	Parameter	Conditions		Typ	Limit		Units
					Min	Max	
V_{IN}	Input Voltage	(Note 10)			1.65	3.6	V
		(Note 16)				4.0	
ΔV_{OUT}	Output Voltage Tolerance	V_{IN} = $V_{IN(NOM)}$ to 3.6V I_{LOAD} = 1 to 300mA			-1.0 **-3.0**	1.0 **3.0**	%
			Temperature (T_J)= -25°C to +85°C		-2.5	2.5	
	Line Regulation Error	V_{IN} = $V_{OUT(NOM)}$ +0.5V to 3.6V, I_{OUT} = 1mA 0.8V ≤ V_{OUT} ≤ 2.8V		0.05		**1**	%/V
	Load Regulation Error	I_{OUT} = 1mA to 300mA		10		**60**	µV/mA
V_{DO}	Dropout Voltage(Note 11)	1.8 ≤ V_{OUT} ≤ 2.5V	I_{OUT} = 150mA	55		**90**	mV
			I_{OUT} = 300mA	110		**180**	
		V_{OUT} > 2.5V	I_{OUT} = 150mA	40		**80**	
			I_{OUT} = 300mA	75		**160**	
I_{LOAD}	Minimum Load Current	(Note 12)			0		mA
I_Q	Quiescent Current	V_{EN} = 950mV, I_{OUT} = 0mA		50		**100**	µA
		V_{EN} = 950mV, I_{OUT} = 300mA		120		**225**	
		V_{EN} = 0.4V		0.001		**1.0**	
I_{SC}	Short Circuit Current Limit	V_{IN} = 3.6V (Note 13)		550		**900**	mA
I_{OUT}	Maximum Output Current				**300**		mA
PSRR	Power Supply Rejection Ratio (Note 14)	f = 1kHz, I_{OUT} = 1mA to 300mA		65			dB
e_n	Output noise Voltage (Note 14)	BW = 10Hz to 100kHz, V_{IN} = 4.2V, C_{OUT} = 4.7µF		280			μV_{RMS}
$T_{SHUTDOWN}$	Thermal Shutdown	Temperature		160			°C
		Hysteresis		20			

Electrical Characteristics con't.

Unless otherwise noted, V_{EN} =950mV, V_{IN} = V_{OUT} + 0.5V, or 1.8V, whichever is higher. C_{IN} = 1µF, I_{OUT} = 1.0mA, C_{OUT} =4.7µF.

Typical values and limits appearing in normal type apply for T_A = 25°C. Limits appearing in **boldface** type apply over the full junction temperature range for operation, −40 to +125°C. (Note 9)

Symbol	Parameter	Conditions		Typ	Limit		Units
					Min	Max	
Enable Control Characteristics							
I_{EN} (Note 15)	Maximum Input Current at V_{EN} Input	V_{EN} = 0V, V_{IN} = 3.6V		0.001			µA
		V_{EN} = V_{IN} = 3.6V		3		**5.5**	
V_{IL}	Low Input Threshold	V_{IN} = 1.65V to 3.6V				**0.4**	V
V_{IH}	High Input Threshold	V_{IN} = 1.65V to 3.6V			**0.95**		V
Timing Characteristics							
T_{ON}	Turn On Time (Note 14)	To 95% Level $V_{IN(MIN)}$ to 3.6V	V_{OUT} ≤ 2.0V	100			µs
			V_{OUT} > 2.0V	140			
	Line Transient Response $\lvert\delta V_{OUT}\rvert$	T_{rise} = T_{fall} = 30µs (Note 14) δV_{IN} = 600mV		6			mV (pk - pk)
Transient Response	Load Transient Response $\lvert\delta V_{OUT}\rvert$	T_{rise} = T_{fall} = 1µs (Note 14)	I_{OUT} = 0 mA to 300mA	140			mV
			I_{OUT} = 1mA to 300mA	110			
			I_{OUT} = 300mA to 1mA	80			
			I_{OUT} = 0mA to 200mA	110			
			I_{OUT} = 1mA to 200mA	80			
			I_{OUT} = 200mA to 1mA	60			
			I_{OUT} = 0mA to 150mA	100			
			I_{OUT} = 1mA to 150mA	70			
			I_{OUT} = 150mA to 1mA	50			
	Overshoot on Start-up			0		**2**	%
I_{IR}	In-Rush Current (Note 14)			600		**1000**	mA

Note 1: Absolute Maximum Ratings are limits beyond which damage can occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

Note 2: All Voltages are with respect to the potential at the GND pin.

Note 3: For further information on these packages please refer to the following application notes,AN-1112 Micro SMD Wafer Level Chip Scale Package.

Note 4: Internal thermal shutdown circuitry protects the device from permanent damage.

Note 5: The human body model is 100pF discharged through a 1.5kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin.

Note 6: The maximum ambient temperature ($T_{A(max)}$) is dependant on the maximum operating junction temperature ($T_{J(max-op)}$ = 125°C), the maximum power dissipation of the device in the application ($P_{D(max)}$), and the junction to ambient thermal resistance of the part / package in the application (θ_{JA}), as given by the following equation: $T_{A(max)} = T_{J(max-op)} - (\theta_{JA} \times P_{D(max)})$.

Note 7: Junction to ambient thermal resistance is dependant on the application and board layout. In applications where high maximum power dissipation is possible, special care must be paid to thermal dissipation issues in board design.

Note 8: Full details can be found in JESD61-7

Note 9: All limits are guaranteed. All electrical characteristics having room-temperature limits are tested during production at T_J = 25°C or correlated using Statistical Quality Control methods. Operation over the temperature specification is guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

Note 10: $V_{IN(MIN)}$ = $V_{OUT(NOM)}$ + 0.5V or 1.65V, whichever is greater. (See post DC/DC convertor example in application information section).

Note 11: Dropout voltage is voltage difference between input and output at which the output voltage drops to 100mV below its nominal value. This parameter is only specified for output voltages above 1.8V.

Note 12: The device maintains the regulated output voltage without a load.

Note 13: Short circuit current is measured with V_{OUT} pulled to 0V.

Note 14: This electrical specification is guaranteed by design.

Note 15: Enable Pin has an internal 1.2MΩ typical, resistor connected to GND.

Note 16: The device will operate with input voltages up to 4.0V. However special care should be taken in relation to thermal dissipation and the need to derate the maximum allowable ambient temperature. See (Note 6, Note 7)

Output Capacitor, Recommended Specifications

	Parameter	Conditions		Typ	Limit		Units
					Min	Max	
C_{OUT}	Output Capacitor	Capacitance (*Note 17*)	$V_{OUT} \geq 1.5V$	4.7	**2**		µF
			$V_{OUT} < 1.5V$ (*Note 18*)	2.2	**1.6**		
		ESR			**5**	**500**	mΩ

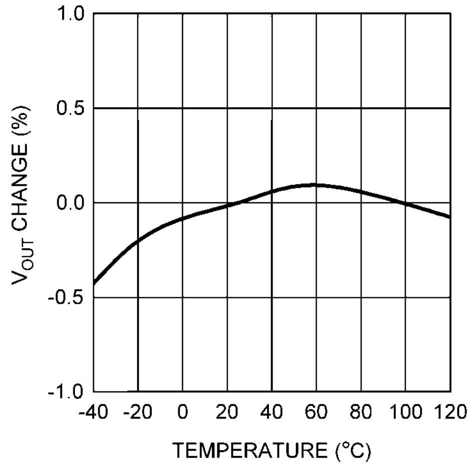
Note 17: The capacitor tolerance should be 30% or better over temperature. The full operating conditions for the application should be considered when selecting a suitable capacitor to ensure that the minimum value of capacitance is always met. Recommended capacitor type is X7R or X5R. (See capacitor section in Applications Hints)

Note 18: On lower voltage options, 2.2µF output capacitor may be used but some degradation in load transient (10 -15%) can be expected, compared to a 4.7µF.

Typical Performance Characteristics.

Unless otherwise specified, C_{IN} = 1.0µF Ceramic, C_{OUT} = 4.7µF Ceramic, $V_{IN} = V_{OUT(NOM)}$ + 0.5V or 1.8V whichever is greater, T_A = 25°C, $V_{OUT(NOM)}$ = 1.5V , Shutdown pin is tied to V_{IN}.

Output Voltage Change vs Temperature



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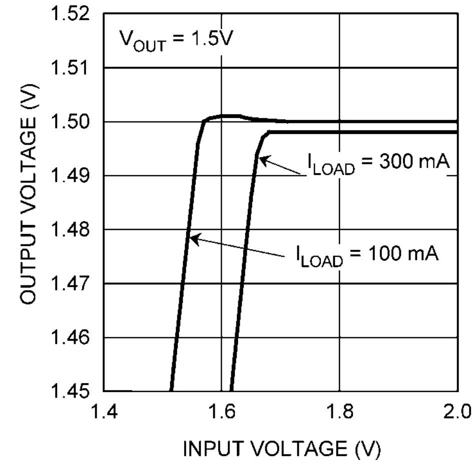
Output Voltage vs Minimum Input Voltage



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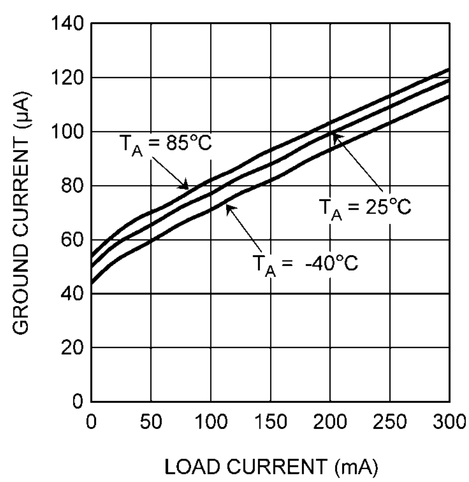
Ground Current vs Load Current



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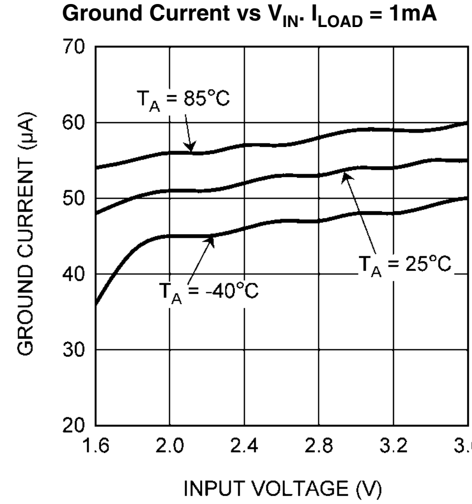
Ground Current vs V_{IN}. I_{LOAD} = 1mA



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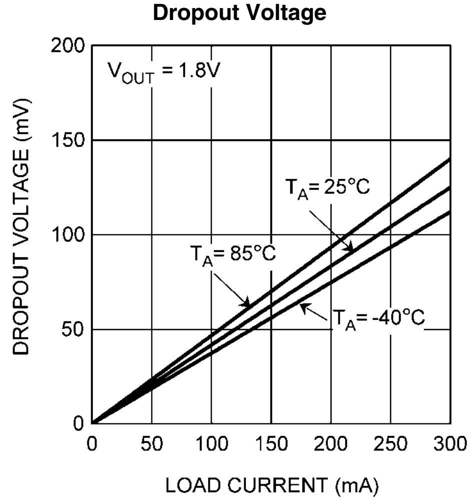
Dropout Voltage



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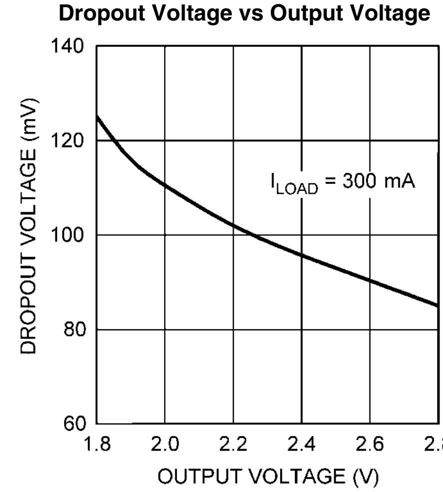
Dropout Voltage vs Output Voltage



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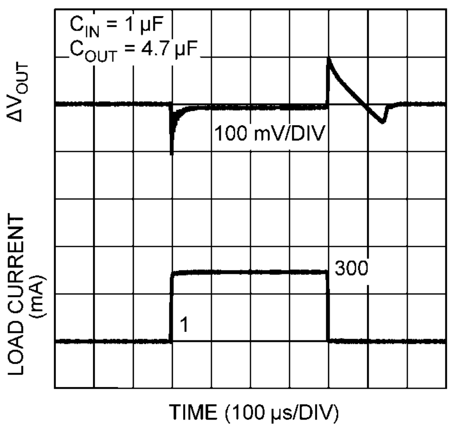
Typical Performance Characteristics con't.

Unless otherwise specified, C_{IN} = 1.0µF Ceramic, C_{OUT} = 4.7µF Ceramic, V_{IN} = $V_{OUT(NOM)}$ + 0.5V or 1.8V whichever is greater, T_A = 25°C, $V_{OUT(NOM)}$ = 1.5V , Shutdown pin is tied to V_{IN}.

Load Transient, V_{OUT} = 1.5V



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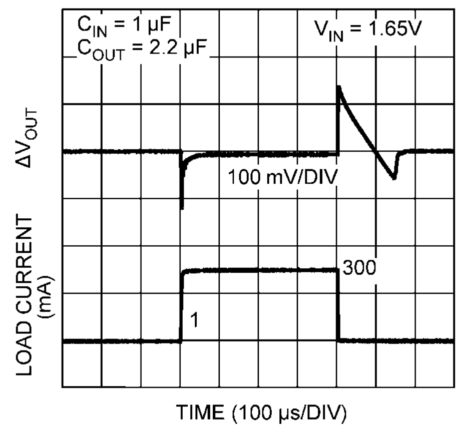
Load Transient, V_{OUT} = 1.2V



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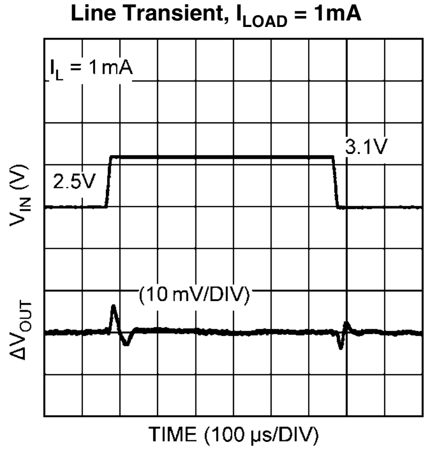
Line Transient, I_{LOAD} = 1mA



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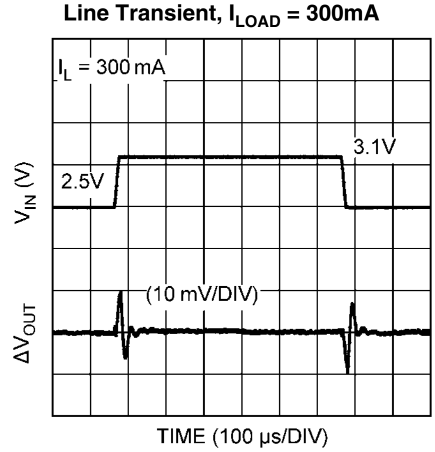
Line Transient, I_{LOAD} = 300mA



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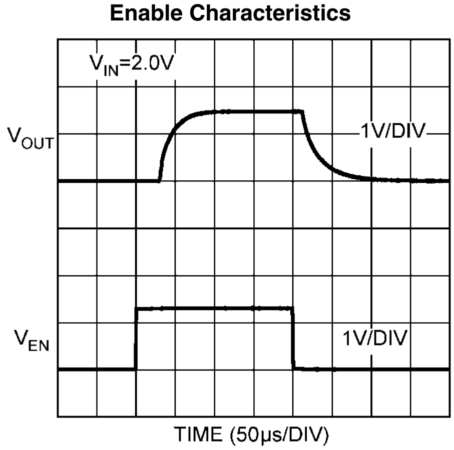
Enable Characteristics



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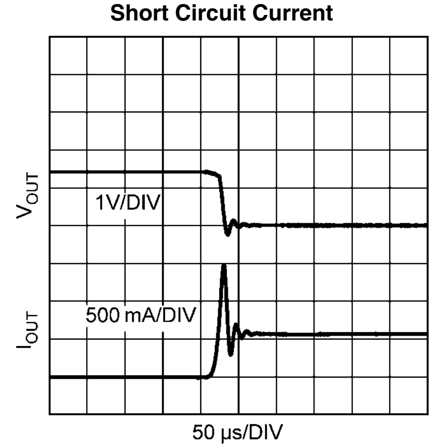
Short Circuit Current



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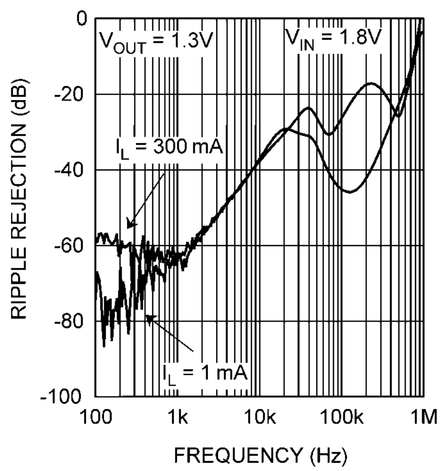
Typical Performance Characteristics con't.

Unless otherwise specified, C_{IN} = 1.0µF Ceramic, C_{OUT} = 4.7µF Ceramic, V_{IN} = $V_{OUT(NOM)}$ + 0.5V or 1.8V whichever is greater, T_A = 25°C, $V_{OUT(NOM)}$ = 1.5V , Shutdown pin is tied to V_{IN}.

Power Supply Rejection Ratio



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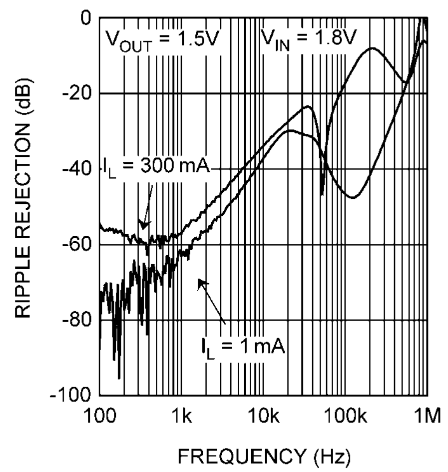
Power Supply Rejection Ratio



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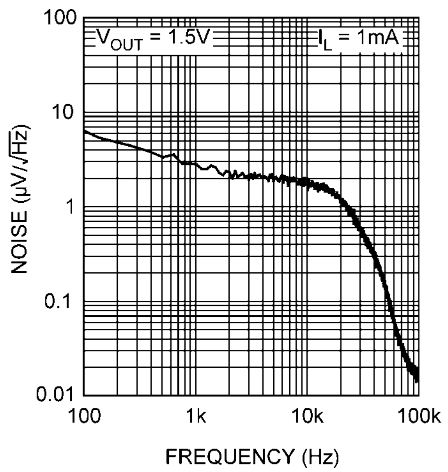
Noise Density



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Application Information

EXTERNAL CAPACITORS

In common with most regulators, the LP3991 requires external capacitors for regulator stability. The LP3991 is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

INPUT CAPACITOR

An input capacitor is required for stability. It is recommended that a 1.0µF capacitor be connected between the LP3991 input pin and ground (this capacitance value may be increased without limit).

This capacitor must be located a distance of not more than 1cm from the input pin and returned to a clean analogue ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

Important: Tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be guaranteed by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for the ESR (Equivalent Series Resistance) on the input capacitor, but tolerance, temperature, and voltage coefficients must be considered when selecting the capacitor to ensure the capacitance will remain ≅ 1.0µF over the entire operating temperature range.

OUTPUT CAPACITOR

Correct selection of the output capacitor is critical to ensure stable operation in the intended application.

The output capacitor must meet all the requirements specified in the recommended capacitor table over all conditions in the application. these conditions include DC bias, frequency and temperature. Unstable operation will result if the capacitance drops below the minimum specified value.

The LP3991 is designed specifically to work with very small ceramic output capacitors. For voltage options of 1.5V and higher, A 4.7µF ceramic capacitor (dielectric type X7R or X5R) with an ESR between 5mΩ to 500mΩ, is suitable in the LP3991 application circuit. However, on lower V_{OUT} options a 2.2µF may be employed with only a small increase in load transient.

Other ceramic types such as Y5V and Z5U are less suitable owing to their inferior temperature characteristics. (See section on Capacitor Characteristics).

It is also recommended that the output capacitor is placed within 1cm of the output pin and returned to a clean, low impedance, ground connection.

It is possible to use tantalum or film capacitors at the device output, V_{OUT}, but these are not as attractive for reasons of size and cost (see the section Capacitor Characteristics).

NO-LOAD STABILITY

The LP3991 will remain stable and in regulation with no external load. This is an important consideration in some circuits, for example CMOS RAM keep-alive applications.

CAPACITOR CHARACTERISTICS

The LP3991 is designed to work with ceramic capacitors on the input and output to take advantage of the benefits they offer. For capacitance values around 4.7µF, ceramic capacitors give the circuit designer the best design options in terms of low cost and minimal area.

For both input and output capacitors, careful interpretation of the capacitor specification is required to ensure correct device operation. The capacitor value can change greatly dependant on the conditions of operation and capacitor type.

In particular, to ensure stability, the output capacitor selection should take account of all the capacitor parameters, to ensure that the specification is met within the application. Capacitance value can vary with DC bias conditions as well as temperature and frequency of operation. Capacitor values will also show some decrease over time due to aging. The capacitor parameters are also dependant on the particular case size with smaller sizes giving poorer performance figures in general.

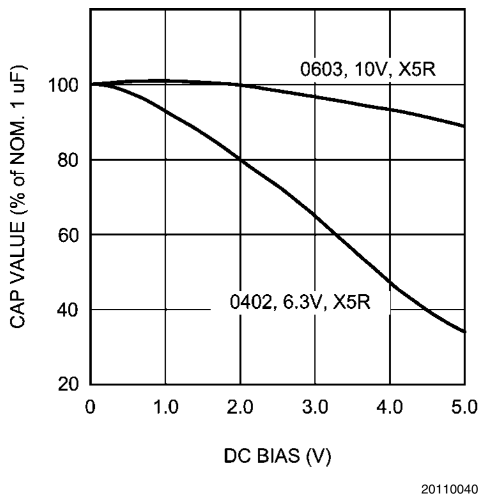


FIGURE 1. Effect of DC bias on Capacitance Value.

As an example *Figure 1* shows a typical graph showing a comparison of capacitor case sizes in a Capacitance vs. DC Bias plot. As shown in the graph, as a result of the DC Bias condition, the capacitance value may drop below the minimum capacitance value given in the recommended capacitor table. Note that the graph shows the capacitance out of spec for the 0402 case size capacitor at higher bias voltages. It is therefore recommended that the capacitor manufacturers' specifications for the nominal value capacitor are consulted for all conditions as some capacitor sizes (e.g. 0402) may not be suitable in the actual application. Ceramic capacitors have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 4.7µF ceramic capacitor is in the range of 20mΩ to 40mΩ, which easily meets the ESR requirement for stability for the LP3991. The temperature performance of ceramic capacitors varies by type. Capacitor type X7R is specified with a tolerance of ±15% over the temperature range -55°C to +125°C. The X5R has a similar tolerance over the reduced temperature range of -55°C to +85°C. Some large value ceramic capacitors (4.7µF) are manufactured with Z5U or Y5V temperature characteristics, which can result in the capacitance dropping by more than 50% as the temperature varies from 25°C to 85°C. Therefore X7R or X5R types are recommended in applications where the temperature will change significantly above or below 25°C.

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the

1µF to 4.7µF range. Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25°C down to -40°C, so some guard band must be allowed.

ENABLE CONTROL

The LP3991 features an active high Enable pin, V_{EN}, which turns the device on when pulled high. When not enabled the regulator output is off and the device typically consumes 2nA.

If the application does not require the Enable switching feature, the V_{EN} pin should be tied to V_{IN} to keep the regulator output permanently on.

To ensure proper operation, the signal source used to drive the V_{EN} input must be able to swing above and below the specified turn-on/off voltage thresholds listed in the Electrical Characteristics section under V_{IL} and V_{IH}.

micro SMD MOUNTING

The micro SMD package requires specific mounting techniques which are detailed in the National Semiconductor Application Note (AN-1112). Referring to the section *Surface Mount Technology (SMT) Assenbly Considerations*, it should be noted that the pad style which must be used with the 4 pin package is NSMD (non-solder mask defined) type.

For best results during assembly, alignment ordinals on the PCB may be used to facilitate placement of the micro SMD device.

micro SMD LIGHT SENSITIVITY

Exposing the micro SMD device to direct sunlight may cause mis-operation of the device. Light sources such as halogen lamps can affect the electrical performance if brought near to the device.

The wavelengths which have most detrimental effect are reds and infra-reds, which means that fluorescent lighting, used inside most buildings will have little effect on performance.

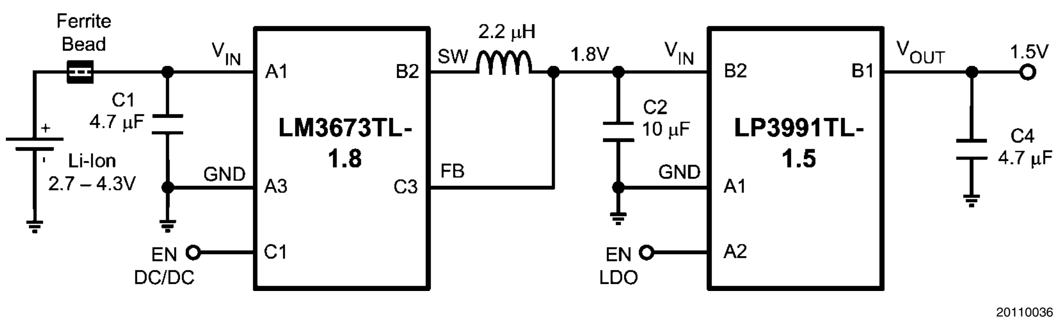


FIGURE 2. LP3991 Used as a Post DC/DC regulator

POST-BUCK REGULATOR

Linear Post-Regulation can be an effective way to reduce ripple and switching noise from DC/DC convertors while still maintaining a reasonably high overall efficiency.

The LP3991 is particularly suitable for this role due to its low input voltage requirements. In addition, there is often no need for a separate input capacitor for the LP3991 as it can share the output cap of the DC/DC convertor.

Care of PCB layouts involving switching regulators is paramount. In particular, the ground paths for the LDO should be routed separately from the switcher ground and star connected close to the battery. Routing of the switch pin of the DC/DC convertor must be kept short to minimize radiated EMI. A low pass filter such as a ferrite bead or common mode choke on the battery input leads can further reduce radiated EMI.

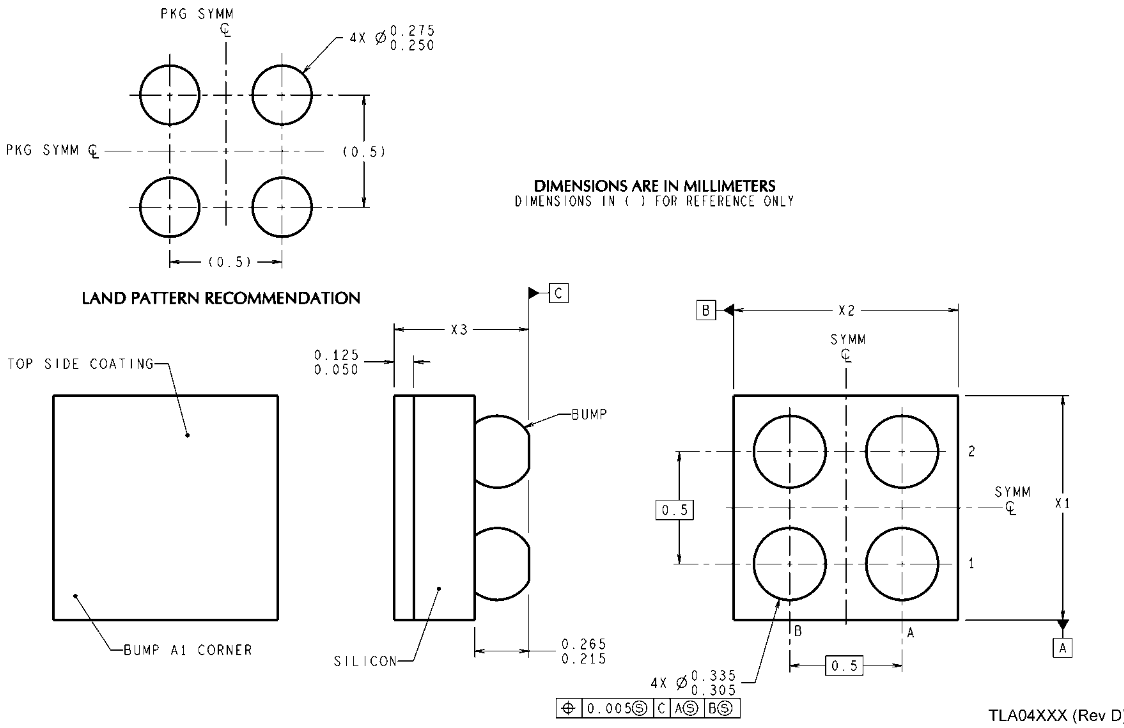
Figure 2 shows a typical example using an LM3673, 350mA DC/DC buck regulator with a nominal output of 1.8V and a 1.5V LP3991. The overall efficiency will be greater than 70% over the full Li-Ion battery voltage range. Maximum efficiency is achieved by minimizing the difference between V_{IN} and V_{OUT} of the LP3991. The LP3991-1.5 will remain in regulation down to an input voltage of 1.65V, so, in this case, a 1.8V buck with 5% tolerance is adequate for all conditions of temperature and load.

MAXIMUM SUPPLY VOLTAGE AND THERMAL CONSIDERATIONS

Maximum recommended input voltage is 3.6V. The device may be operated at 4.0V V_{IN} if proper care is given to the board design in regard to thermal dissipation. As a guide please refer to the following table for ambient temperature at 2 input voltages and 2 load currents for the example board types.

θ_{JA}	V_{IN}	V_{OUT}	I_{OUT}	P_D	Ambient Temp.
88ºC/W	3.6V	2.8V	160mA	0.130W	113ºC
			250mA	0.200W	107ºC
	4.0V	2.8V	160mA	0.190W	108ºC
			250mA	0.300W	98ºC
160ºC/W	3.6V	2.8V	160mA	0.130W	104ºC
			250mA	0.200W	93ºC
	4.0V	2.8V	160mA	0.190W	94ºC
			250mA	0.300W	77ºC

Physical Dimensions inches (millimeters) unless otherwise noted



4 Bump Thin micro SMD, Large Bump
NS Package Number TLA04ZTA
The Dimensions for X1, X2 and X3 as given as:
X1 = 0.963mm ± 0.030mm
X2 = 1.446mm ± 0.03mm
X3 = 0.60mm ± 0.075mm

Notes

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