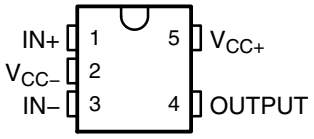
LPV321 SINGLE, LPV358 DUAL, LPV324 QUAD GENERAL-PURPOSE, LOW-VOLTAGE, LOW-POWER, RAIL-TO-RAIL OUTPUT OPERATIONAL AMPLIFIERS

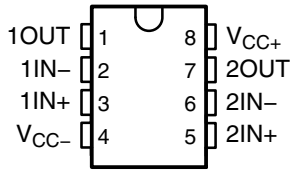
SLOS433I – FEBRUARY 2004 – REVISED MARCH 2005

- 2.7-V and 5-V Performance
- –40°C to 125°C Specification at 5 V
- No Crossover Distortion
- Gain Bandwith of 152 kHz
- Low Supply Current
  - LPV321 . . . 9 μA
  - LPV358 . . . 15 μA
  - LPV324 . . . 28 μA
- Rail-to-Rail Output Swing at 100-kΩ Load
  - V_{CC+} – 3.5 mV
  - V_{CC-} + 90 mV
- V_{ICR} . . . –0.2 V to V_{CC+} – 0.8 V
- Stable With Capacitive Load of 1000 pF
- Applications
  - Active Filters
  - General-Purpose, Low-Voltage Applications
  - Low-Power and/or Portable Applications
- Latch-Up Performance Exceeds 100 mA per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

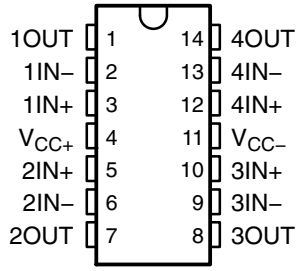
LPV321 . . . DBV OR DCK PACKAGE
(TOP VIEW)



LPV358 . . . D, DDU, OR DGK PACKAGE
(TOP VIEW)



LPV324 . . . D OR PW PACKAGE
(TOP VIEW)



description/ordering information

The LPV321/358/324 devices are low-power (9 μA per channel at 5 V) versions of the LMV321/358/324 operational amplifiers. These are additions to the LMV321/358/324 family of commodity operational amplifiers.

The LPV321/358/324 devices are the most cost-effective solutions for applications where low voltage, low-power operation, space saving, and low price are needed. These devices have rail-to-rail output-swing capability, and the input common-mode voltage range includes ground. They all exhibit excellent speed-power ratios, achieving 152 kHz of bandwidth, with a supply current of only 9 μA typical.

The LPV321, LPV358, and LPV324 are characterized for operation from –40°C to 85°C. The LPV321I, LPV358I, and LPV324I are characterized for operation from –40°C to 125°C.

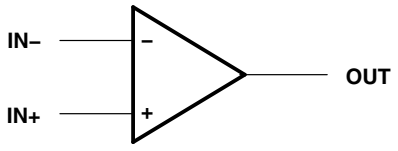
description/ordering information (continued)

ORDERING INFORMATION

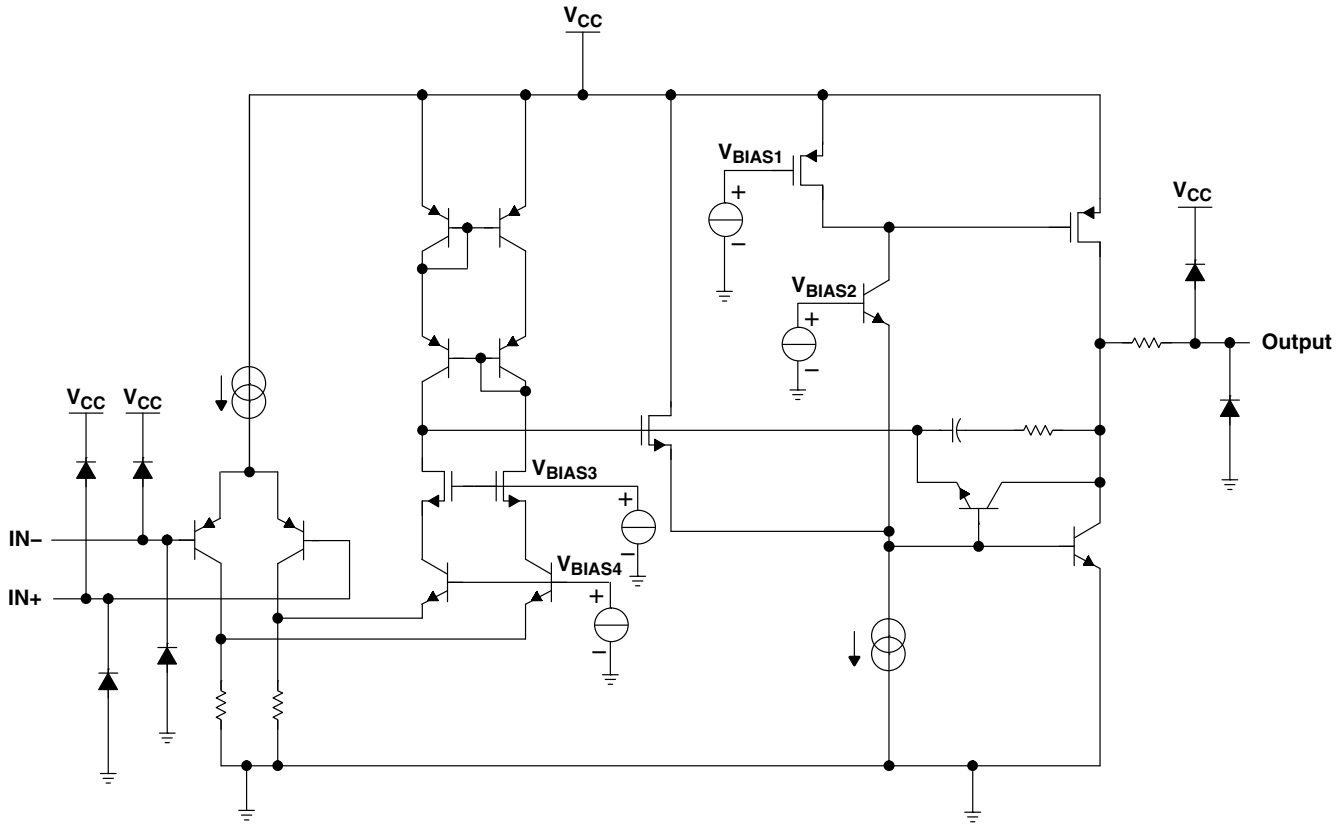
T_A	PACKAGE†			ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	Single	SOT23-5 (DBV)	Reel of 3000	LPV321DBVR	5C7_
			Reel of 250	LPV321DBVT	PREVIEW
		SC-70 (DCK)	Reel of 3000	LPV321DCKR	52_
			Reel of 250	LPV321DCKT	PREVIEW
	Dual	SOIC-8 (D)	Tube of 75	LPV358D	PV358
			Reel of 2500	LPV358DR	
		VSSOP-8 (DDU)	Reel of 3000	LPV358DDUR	5A56
		VSSOP-8 (DGK)	Reel of 2500	LPV358DGKR	546
			Reel of 250	LPV358DGKT	PREVIEW
	Quad	SOIC-14 (D)	Tube of 50	LPV324D	LPV324
			Reel of 2500	LPV324DR	
		TSSOP-14 (PW)	Tube of 90	LPV324PW	PV324
			Reel of 2000	LPV324PWR	
–40°C to 125°C	Single	SOT23-5 (DBV)	Reel of 3000	LPV321IDBVR	5C1_
			Reel of 250	LPV321IDBVT	PREVIEW
		SC-70 (DCK)	Reel of 3000	LPV321IDCKR	53_
			Reel of 250	LPV321IDCKT	PREVIEW
	Dual	SOIC-8 (D)	Tube of 75	LPV358ID	PV358I
			Reel of 2500	LPV358IDR	
		VSSOP-8 (DDU)	Reel of 3000	LPV358IDDUR	5AE6
		VSSOP-8 (DGK)	Reel of 2500	LPV358IDGKR	556
			Reel of 250	LPV358IDGKT	PREVIEW
	Quad	SOIC-14 (D)	Tube of 50	LPV324ID	LPV324I
			Reel of 2500	LPV324IDR	
		TSSOP-14 (PW)	Tube of 90	LPV324IPW	PV324I
			Reel of 2000	LPV324IPWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
‡ DBV/DCK: The actual top-side marking has one additional character that designates the assembly/test site.

symbol (each amplifier)



LPV324 simplified schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC+} - V_{CC-}$ (see Note 1)		5.5 V
Differential input voltage, V_{ID} (see Note 2)		$\pm V_{CC}$
Input voltage range, V_I (either input)		V_{CC-} to $V_{CC+} - 1$ V
Package thermal impedance, θ_{JA} (see Notes 3 and 4):	5-pin DBV package	206°C/W
	5-pin DCK package	252°C/W
	8-pin D package	97°C/W
	8-pin DDU package	TBD°C/W
	8-pin DGK package	172°C/W
	14-pin D package	86°C/W
	14-pin PW package	113°C/W
Maximum junction temperature, T_J		150°C
Storage temperature range, T_{stg}		–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltage values, except differential voltages and V_{CC} specified for the measurement of I_{OS}, are with respect to the network GND.
2. Differential voltages are at IN+ with respect to IN–.
3. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Selecting the maximum of 150°C can affect reliability.
4. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	5	V
T_A	Operating free-air temperature	LPV3xx	–40	85	°C
		LPV3xxI	–40	125	

ESD protection

TEST CONDITIONS	TYP	UNIT
Human-Body Model	2	kV
Machine model	200	V
Charged-Device Model	1	kV

2.7-V electrical characteristics

T_A = 25°C, V_{CC+} = 2.7 V, V_{CC-} = 0 V, V_{IC} = 1 V, V_O = V_{CC+}/2, and R_L > 1 MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IO}	Input offset voltage				1.2	7	mV
α_{VIO}	Average temperature coefficient of input offset voltage				4		μV/°C
I_{IB}	Input bias current				1.7	50	nA
I_{IO}	Input offset current				0.6	40	nA
CMRR	Common-mode rejection ratio	0 ≤ V_{IC} ≤ 1.7 V		50	70		dB
k_{SVR}	Supply-voltage rejection ratio	2.7 V ≤ V_{CC+} ≤ 5 V, V_{IC} = 1 V, V_O = 1 V		50	65		dB
V_{ICR}	Common-mode input voltage range	CMRR ≥ 50 dB		0 to 1.7	–0.2 to 1.9		V
V_O	Output swing	R_L = 100 kΩ to 1.35 V	High level	V_{CC+} – 0.100	V_{CC+} – 0.003		V
			Low level		0.080	0.180	
I_{CC}	Supply current	LPV321			4	8	μA
		LPV358 (both amplifiers)			8	16	
		LPV324 (all four amplifiers)			16	24	
SR	Slew rate‡				0.1		V/μs
GBW	Gain bandwidth product	C_L = 22 pF (see Note 5)			205		kHz
Φ_m	Phase margin	C_L = 22 pF (see Note 5)			71		deg
	Gain margin	C_L = 22 pF (see Note 5)			11		dB
V_n	Equivalent input noise voltage	f = 1 kHz			178		nV/√Hz
I_n	Equivalent input noise current	f = 1 kHz			0.5		pA/√Hz

† All typical values are at V_{CC} = 2.7 V, T_A = 25°C.
‡ Number specified is the slower of the positive and negative slew rates.
NOTE 5: Closed-loop gain = 18 dB, V_{IC} = V_{CC+}/2

5-V electrical characteristics

T_A = 25°C, V_{CC+} = 5 V, V_{CC-} = 0 V, V_{IC} = 2 V, V_O = V_{CC+}/2, and R_L > 1 MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP†	MAX	UNIT
V_{IO}	Input offset voltage			25°C		1.5	7	mV
				–40°C to 85°C			10	
				–40°C to 125°C			11	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C		4		µV/°C
I_{IB}	Input bias current			25°C		2	50	nA
				–40°C to 85°C			60	
				–40°C to 125°C			65	
CMRR	Common-mode rejection ratio	0 ≤ V_{IC} ≤ 4 V		25°C	50	71		dB
k_{SVR}	Supply-voltage rejection ratio	2.7 V ≤ V_{CC+} ≤ 5 V, V_{IC} = 1 V, V_O = 1 V		25°C	50	65		dB
V_{ICR}	Common-mode input voltage range	CMRR ≥ 50 dB		25°C	0 to 4	–0.2 to 4.2		V
I_{IO}	Input offset current			25°C		0.6	40	nA
				–40°C to 85°C			50	
				–40°C to 125°C			55	
V_O	Output swing	R_L = 100 kΩ to 2.5 V	High level	25°C	V_{CC+} – 0.100	V_{CC+} – 0.0035		V
				–40°C to 85°C	V_{CC+} – 0.200			
				–40°C to 125°C	V_{CC+} – 0.225			
			Low level	25°C		0.090	0.180	
				–40°C to 85°C			0.220	
				–40°C to 125°C			0.240	
I_{OS}	Output short-circuit current	Sourcing, V_O = 0 V		25°C	2	17		mA
		Sinking, V_O = 5 V			20	72		
I_{CC}	Supply current	LPV321		25°C		9	12	µA
				–40°C to 85°C			15	
				–40°C to 125°C			40	
		LPV358 (both amplifiers)		25°C		15	20	
				–40°C to 85°C			24	
				–40°C to 125°C			80	
		LPV324 (all four amplifiers)		25°C		28	42	
				–40°C to 85°C			46	
				–40°C to 125°C			125	
A_V‡	Large-signal voltage gain	R_L = 100 kΩ		25°C	15	100		V/mV
				–40°C to 85°C	10			
				–40°C to 125°C	10			
SR§	Slew rate			25°C		0.1		V/µs

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ R_L is connected to V_{CC-}. The output voltage is 0.5 V ≤ V_O ≤ 4.5 V.
§ Number specified is the slower of the positive and negative slew rates. Connected as a voltage follower with 3-V step input.

5-V electrical characteristics
T_A = 25°C, V_{CC+} = 5 V, V_{CC-} = 0 V, V_{IC} = 2 V, V_O = V_{CC+}/2, and R_L > 1 MΩ (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP†	MAX	UNIT
GBW	Gain bandwidth product	C_L = 22 pF (see Note 5)	25°C		237		kHz
Φ_m	Phase margin	C_L = 22 pF (see Note 5)	25°C		74		deg
	Gain margin	C_L = 22 pF (see Note 5)	25°C		12		dB
V_n	Equivalent input noise voltage	f = 1 kHz	25°C		146		nV/√Hz
I_n	Equivalent input noise current	f = 1 kHz	25°C		0.3		pA/√Hz

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 5: Closed-loop gain = 18 dB, V_{IC} = V_{CC+}/2

SUPPLY CURRENT
vs
SUPPLY VOLTAGE
(LPV324 – All Channels)

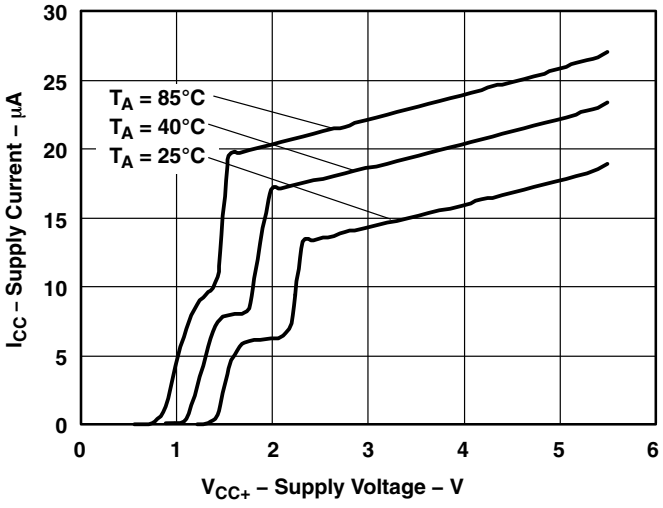


Figure 1

INPUT BIAS CURRENT
vs
TEMPERATURE

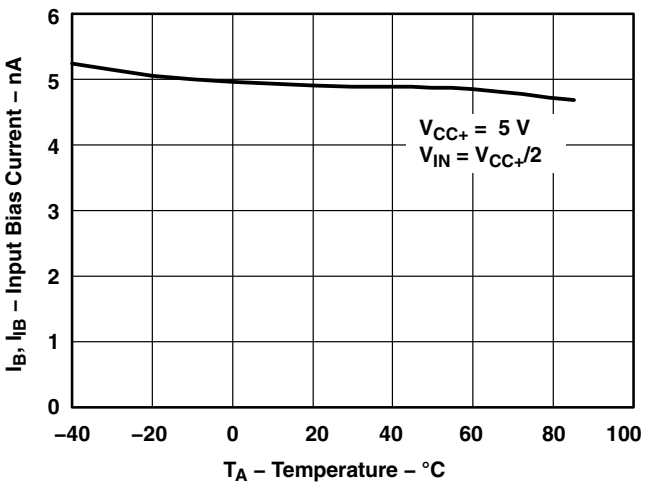


Figure 2

SOURCING CURRENT
vs
OUTPUT VOLTAGE

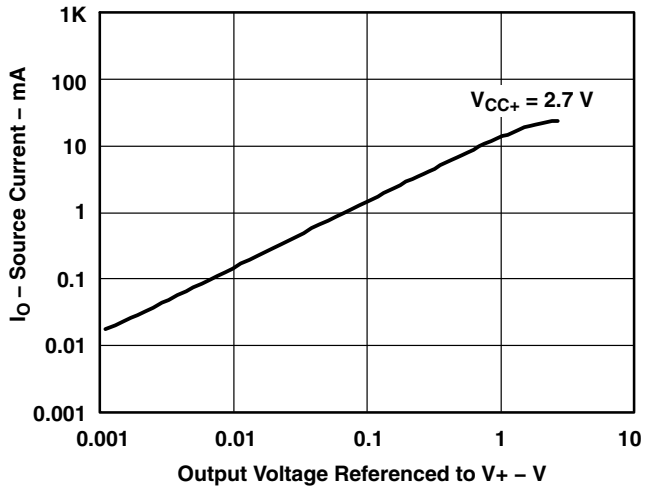


Figure 3

SOURCING CURRENT
vs
OUTPUT VOLTAGE

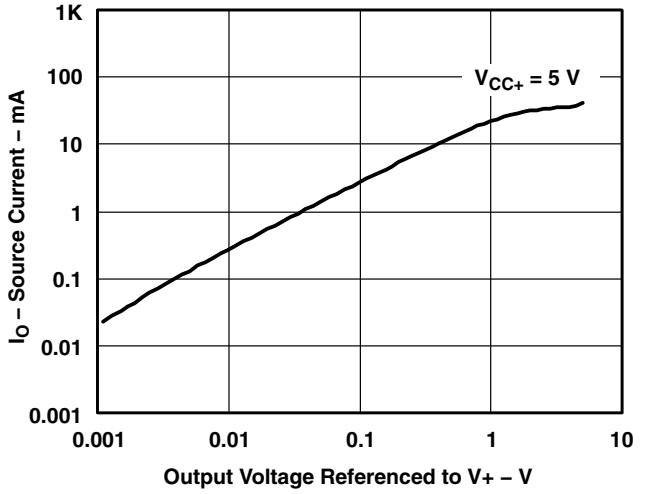


Figure 4

SINKING CURRENT
vs
OUTPUT VOLTAGE

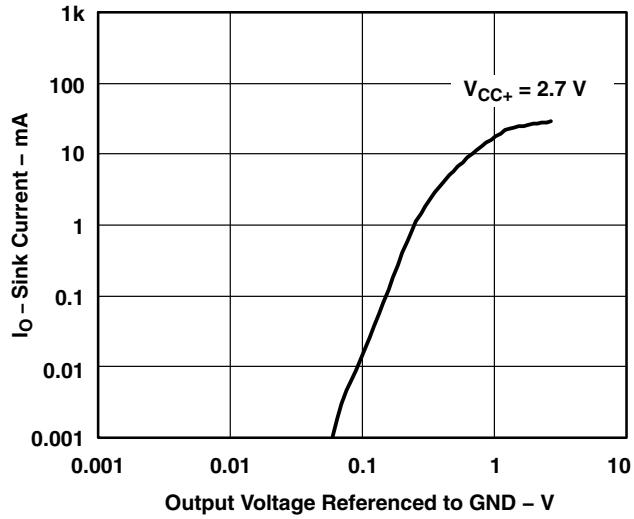


Figure 5

SINKING CURRENT
vs
OUTPUT VOLTAGE

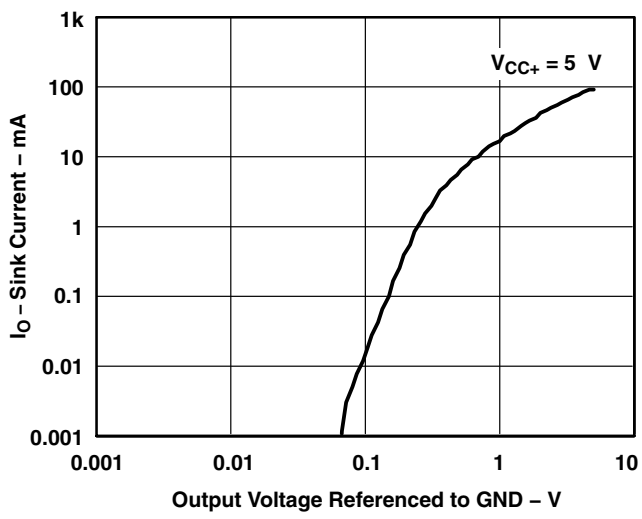


Figure 6

OUTPUT VOLTAGE SWING
vs
SUPPLY VOLTAGE

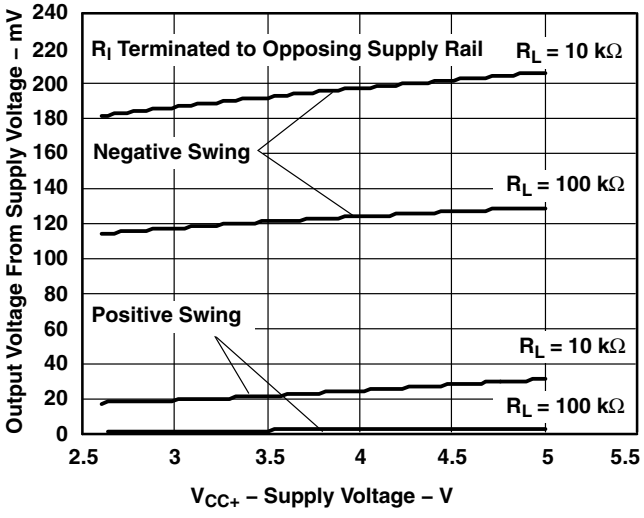


Figure 7

INPUT VOLTAGE NOISE
vs
FREQUENCY

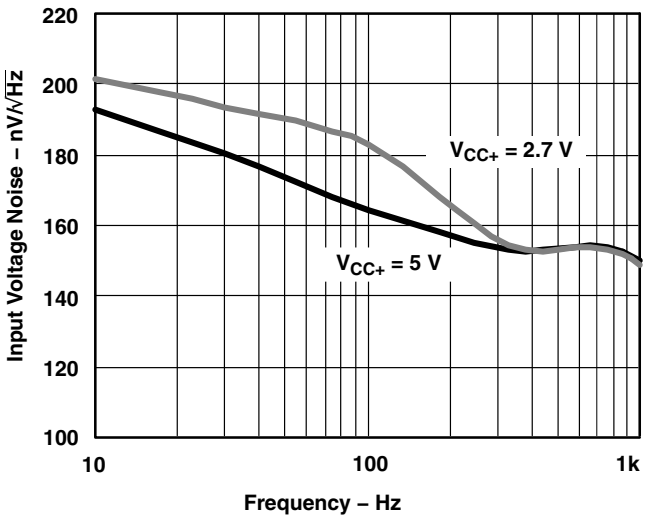


Figure 8

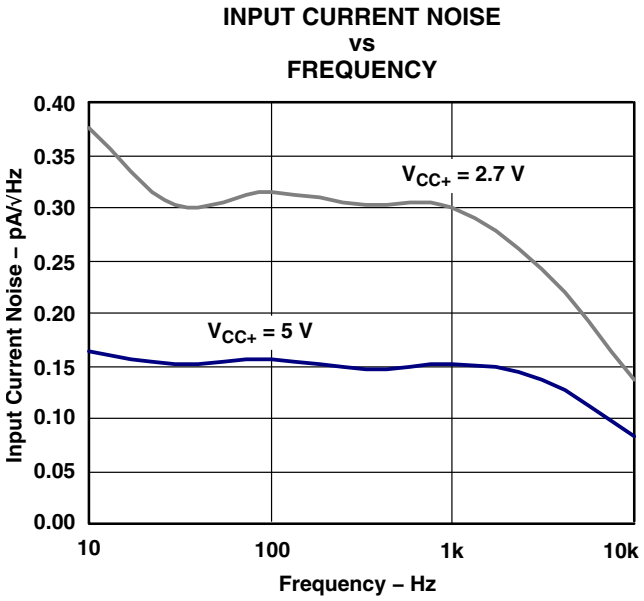


Figure 9

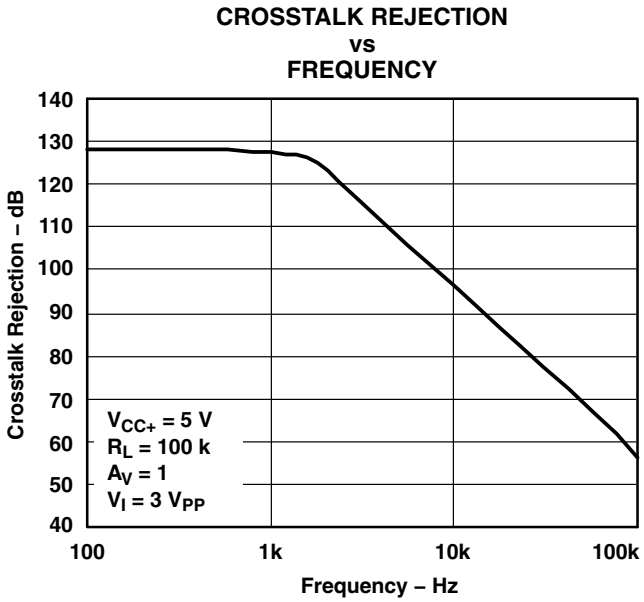


Figure 10

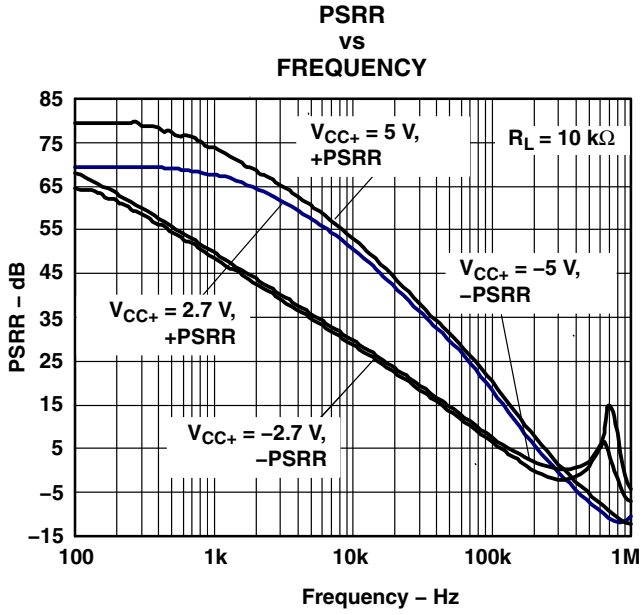


Figure 11

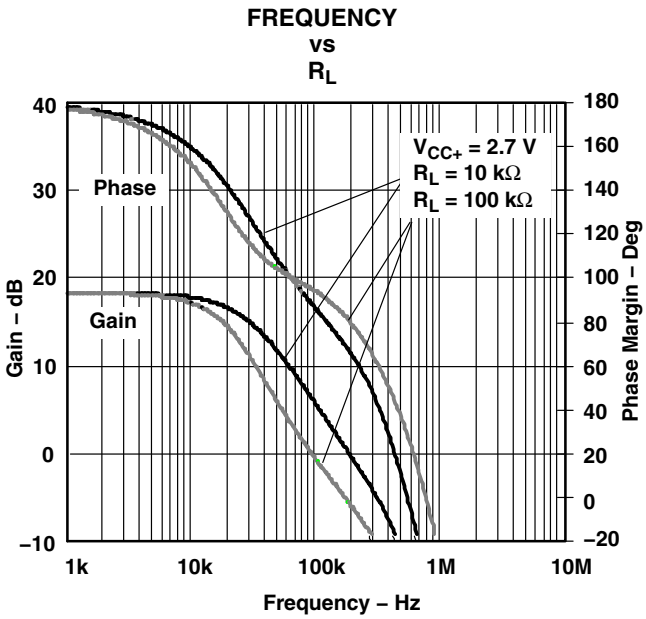


Figure 12

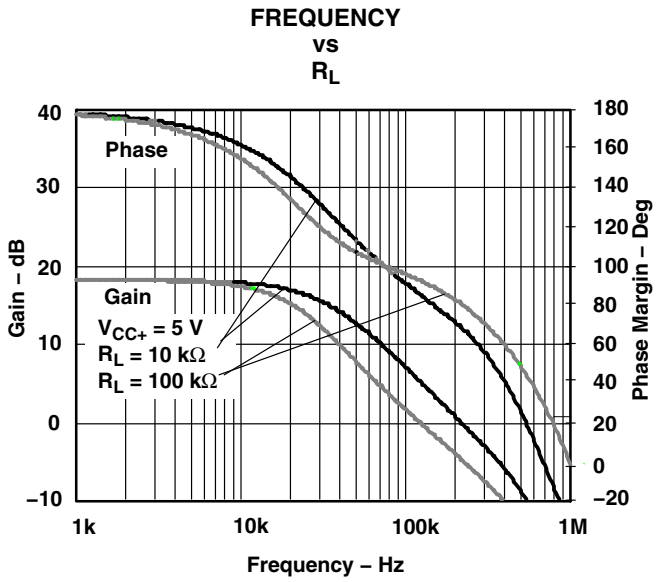


Figure 13

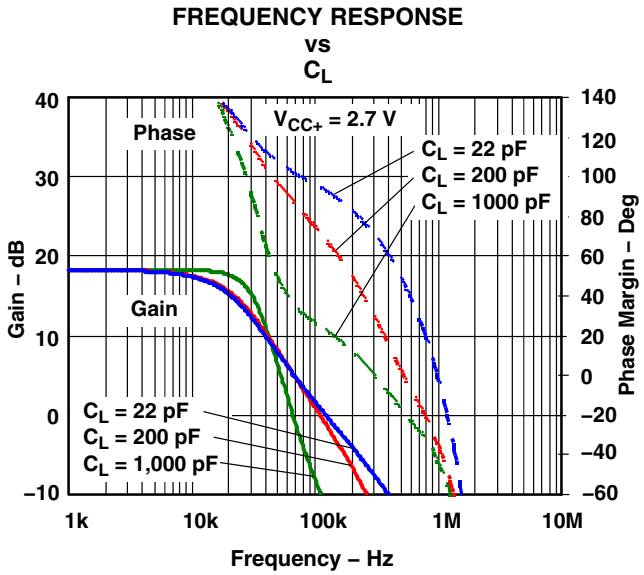


Figure 14

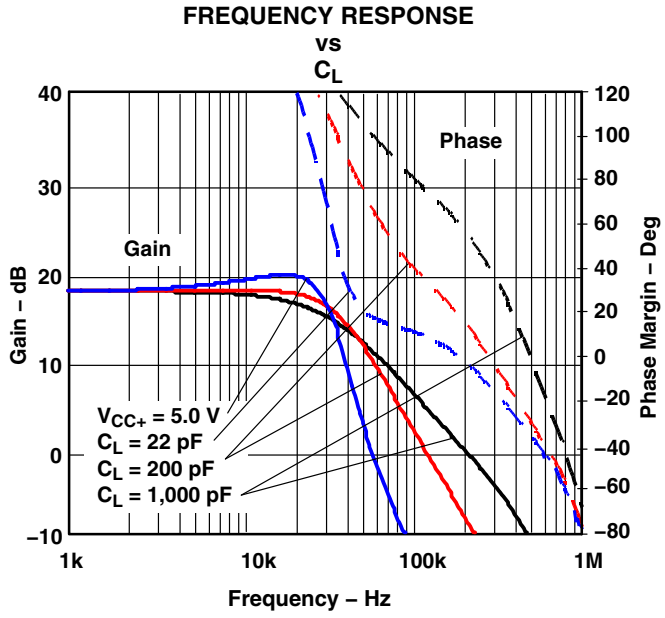


Figure 15

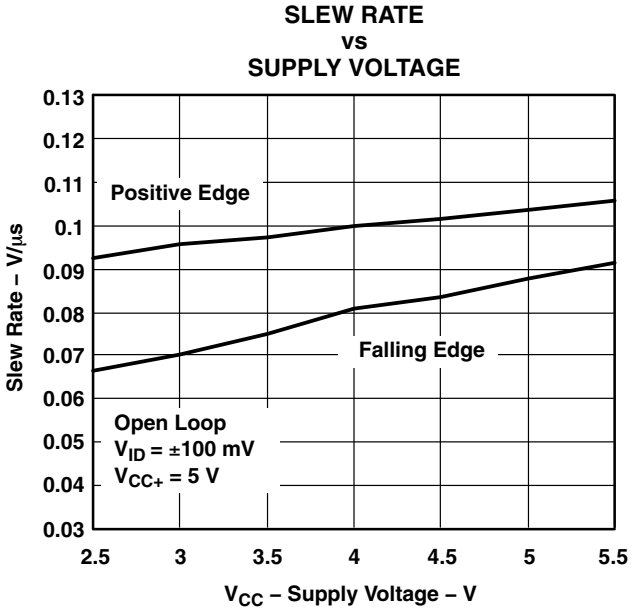


Figure 16

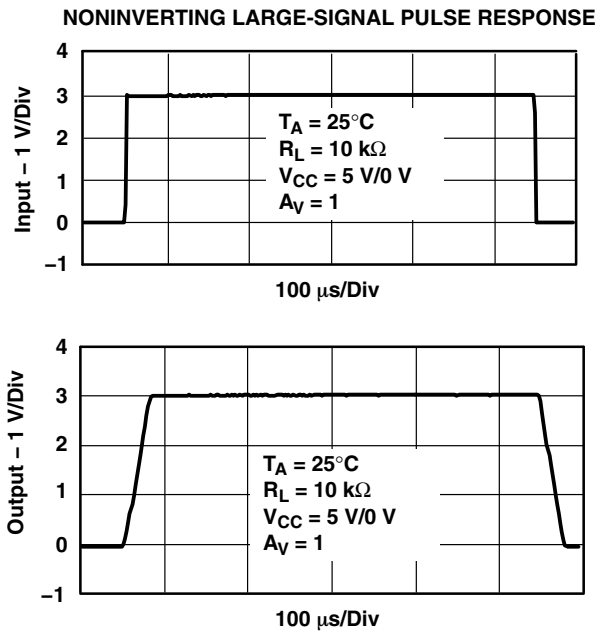


Figure 17

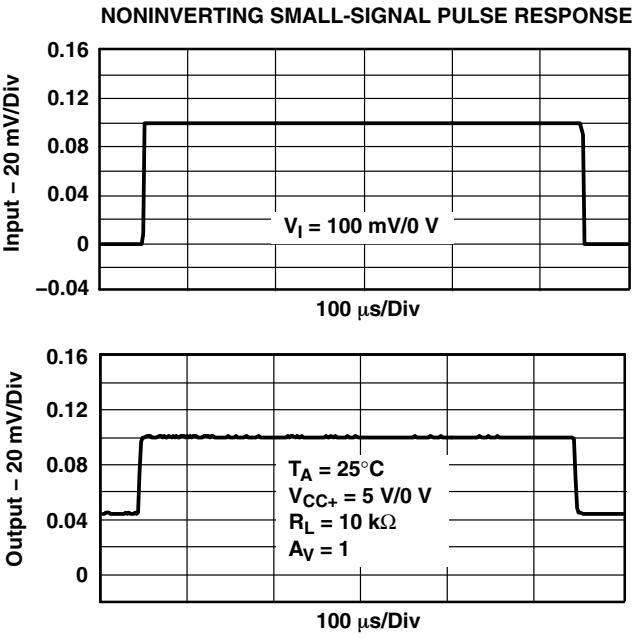


Figure 18

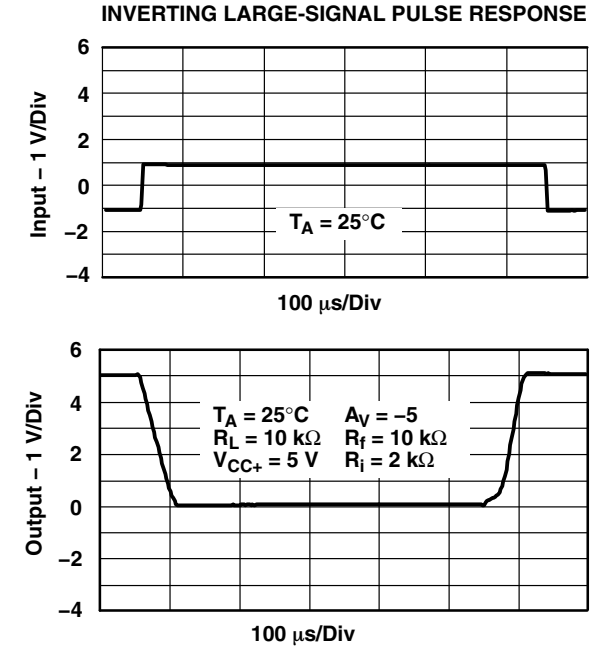


Figure 19

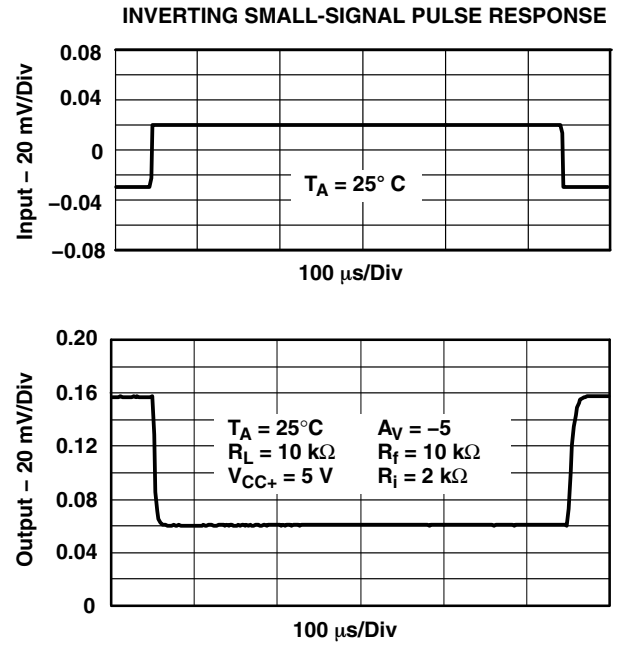


Figure 20

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
LPV321DBVR	NRND	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV321DBVRE4	NRND	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV321DBVRG4	NRND	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV321DCKR	NRND	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV321DCKRE4	NRND	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV321DCKRG4	NRND	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV321IDBVR	NRND	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV321IDBVRE4	NRND	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV321IDBVRG4	NRND	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV321IDCKR	NRND	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV321IDCKRE4	NRND	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV321IDCKRG4	NRND	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV324D	NRND	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV324DE4	NRND	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV324DG4	NRND	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV324DR	NRND	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV324DRE4	NRND	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
LPV324DRG4	NRND	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV324ID	NRND	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV324IDE4	NRND	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV324IDG4	NRND	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV324IDR	NRND	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV324IDRE4	NRND	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV324IDRG4	NRND	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV324IPW	NRND	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV324IPWE4	NRND	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV324IPWG4	NRND	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV324IPWR	NRND	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV324IPWRE4	NRND	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV324IPWRG4	NRND	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV324PW	NRND	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV324PWE4	NRND	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV324PWG4	NRND	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV324PWR	NRND	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV324PWRE4	NRND	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
LPV324PWRG4	NRND	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV358D	NRND	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV358DDUR	NRND	VSSOP	DDU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV358DDURE4	NRND	VSSOP	DDU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV358DDURG4	NRND	VSSOP	DDU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV358DE4	NRND	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV358DG4	NRND	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV358DGKR	NRND	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV358DGKRG4	NRND	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV358DR	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV358DRE4	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV358DRG4	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV358ID	NRND	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV358IDDUR	NRND	VSSOP	DDU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV358IDDURE4	NRND	VSSOP	DDU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV358IDDURG4	NRND	VSSOP	DDU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV358IDE4	NRND	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV358IDG4	NRND	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
LPV358IDGKR	NRND	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV358IDGKRG4	NRND	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV358IDR	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV358IDRE4	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV358IDRG4	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

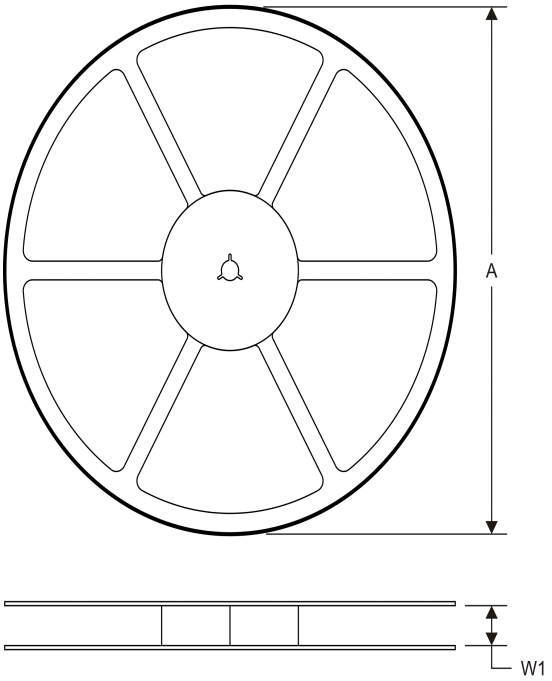
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

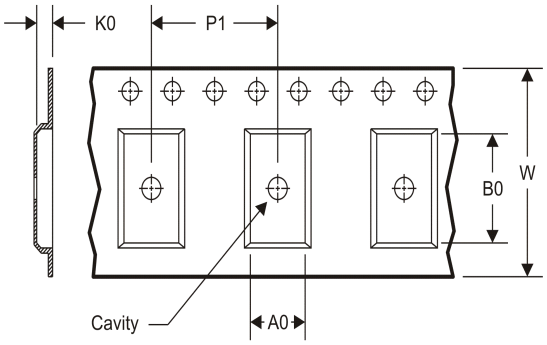
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



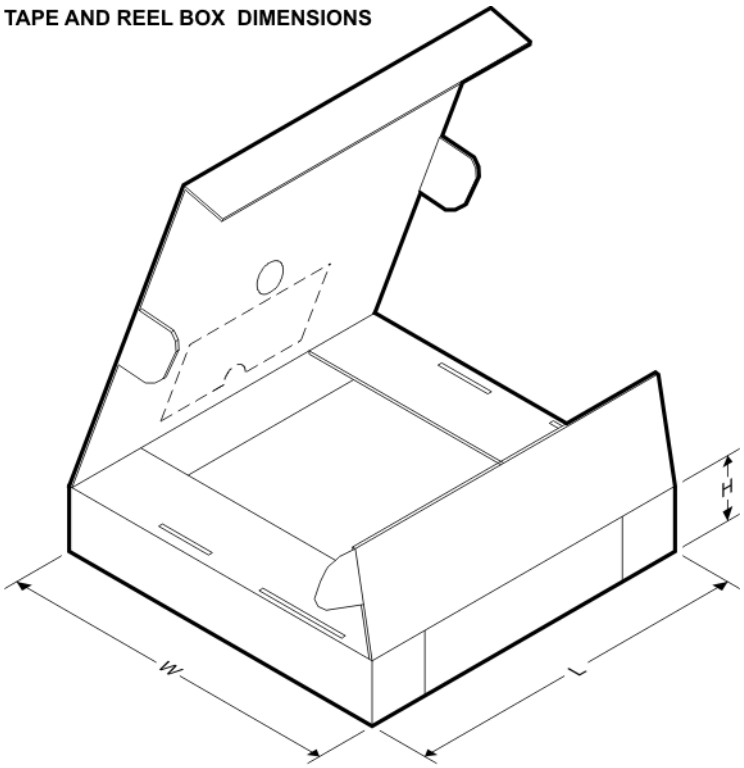
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LPV321DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
LPV321DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
LPV321IDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
LPV321IDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
LPV324DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LPV324IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LPV324IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LPV324PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LPV358DDUR	VSSOP	DDU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
LPV358DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LPV358DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LPV358IDDUR	VSSOP	DDU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
LPV358IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LPV358IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

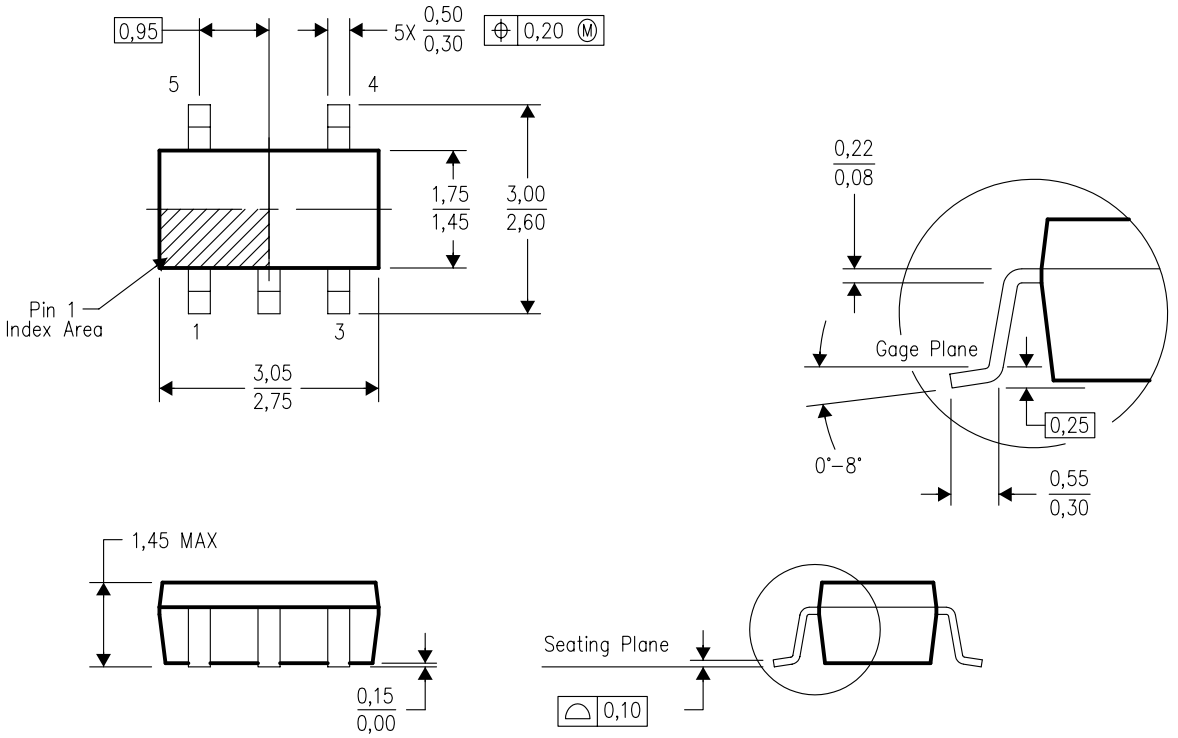
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LPV321DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
LPV321DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
LPV321IDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
LPV321IDCKR	SC70	DCK	5	3000	180.0	180.0	18.0
LPV324DR	SOIC	D	14	2500	367.0	367.0	38.0
LPV324IDR	SOIC	D	14	2500	367.0	367.0	38.0
LPV324IPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
LPV324PWR	TSSOP	PW	14	2000	367.0	367.0	35.0
LPV358DDUR	VSSOP	DDU	8	3000	202.0	201.0	28.0
LPV358DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
LPV358DR	SOIC	D	8	2500	340.5	338.1	20.6
LPV358IDDUR	VSSOP	DDU	8	3000	202.0	201.0	28.0
LPV358IDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
LPV358IDR	SOIC	D	8	2500	340.5	338.1	20.6

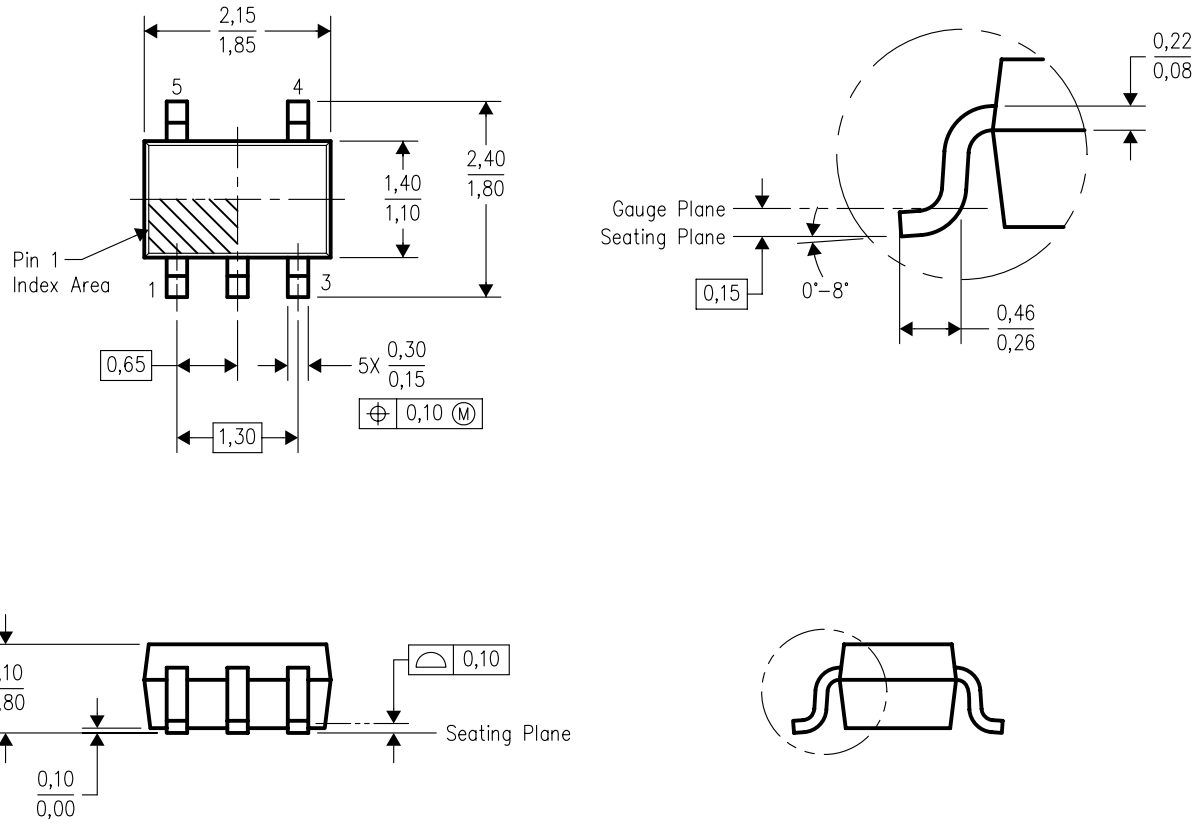
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/K 03/2006

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

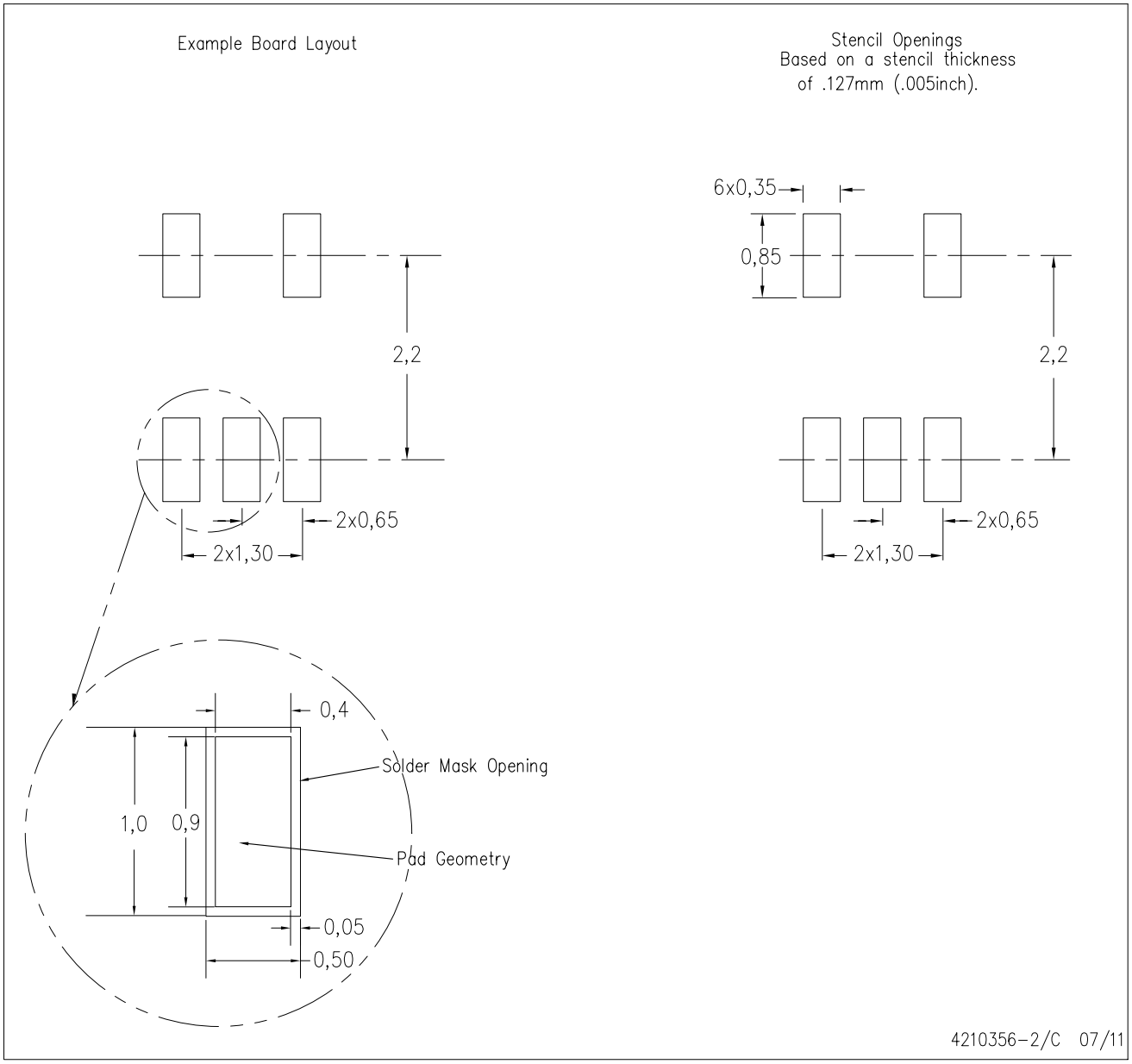
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

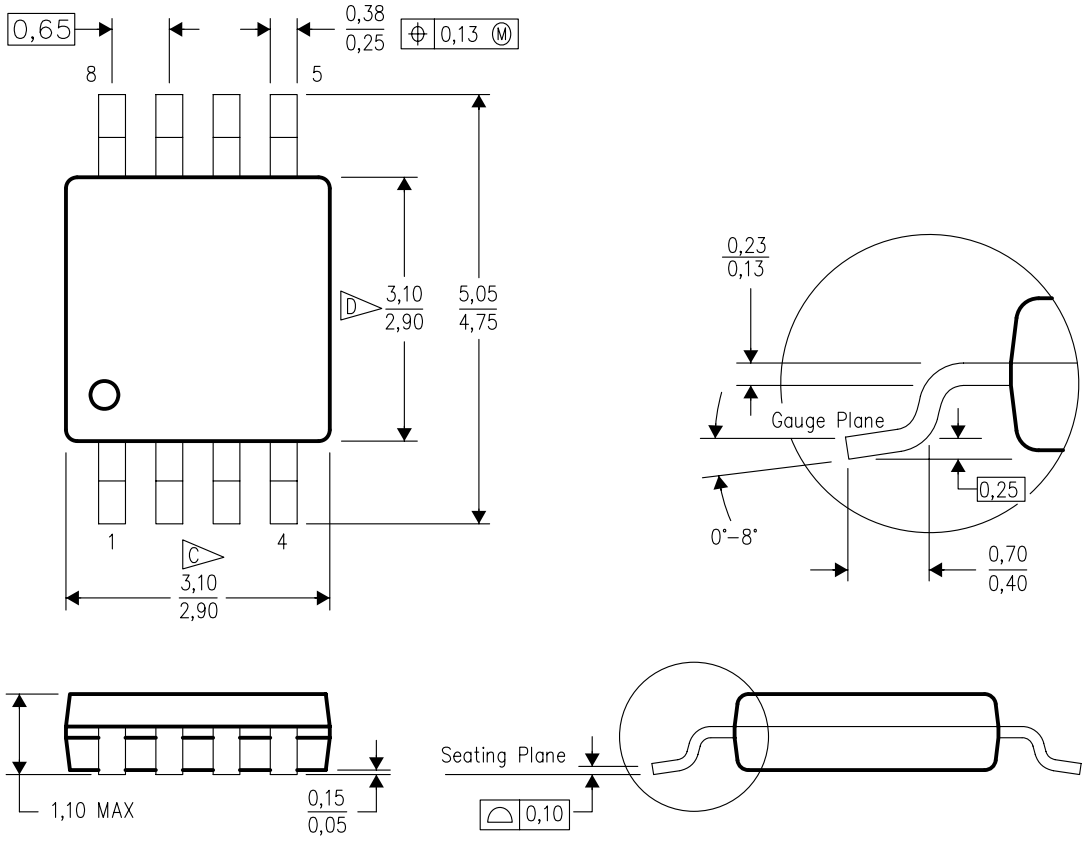
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

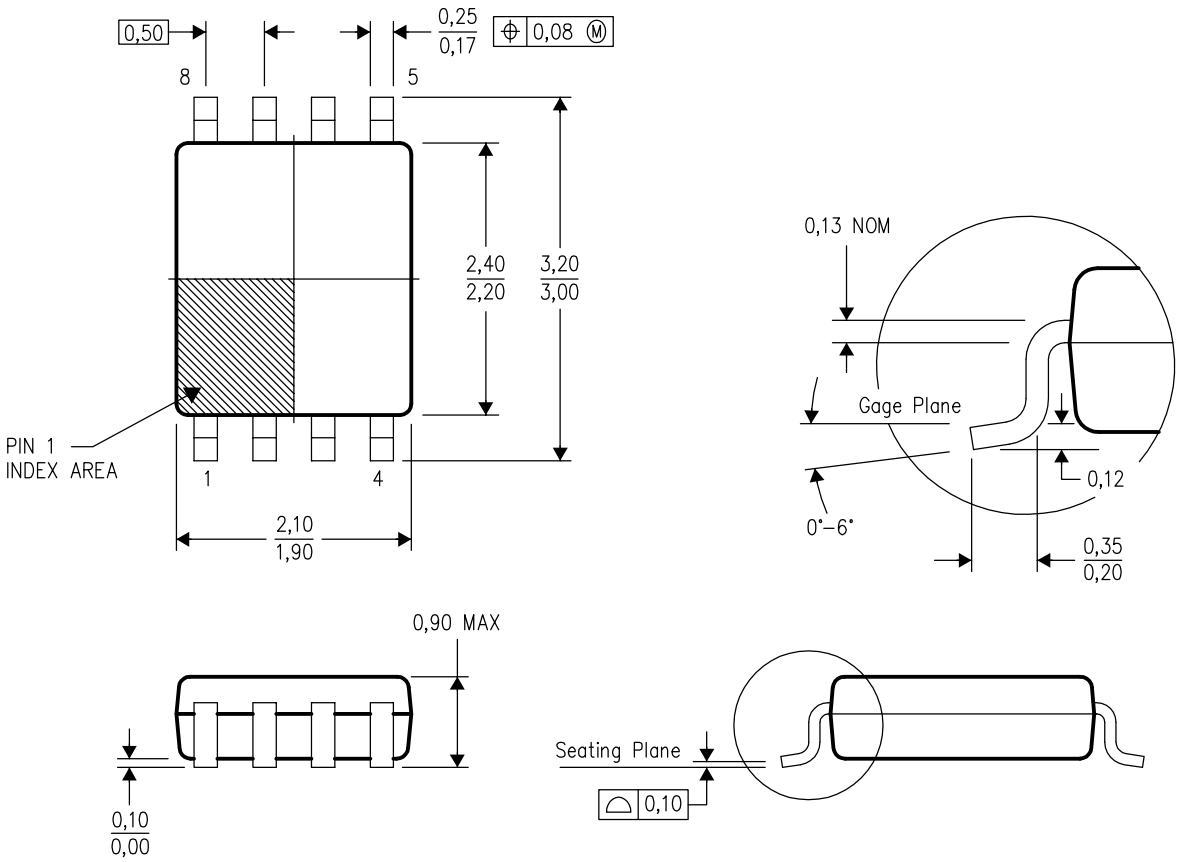
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

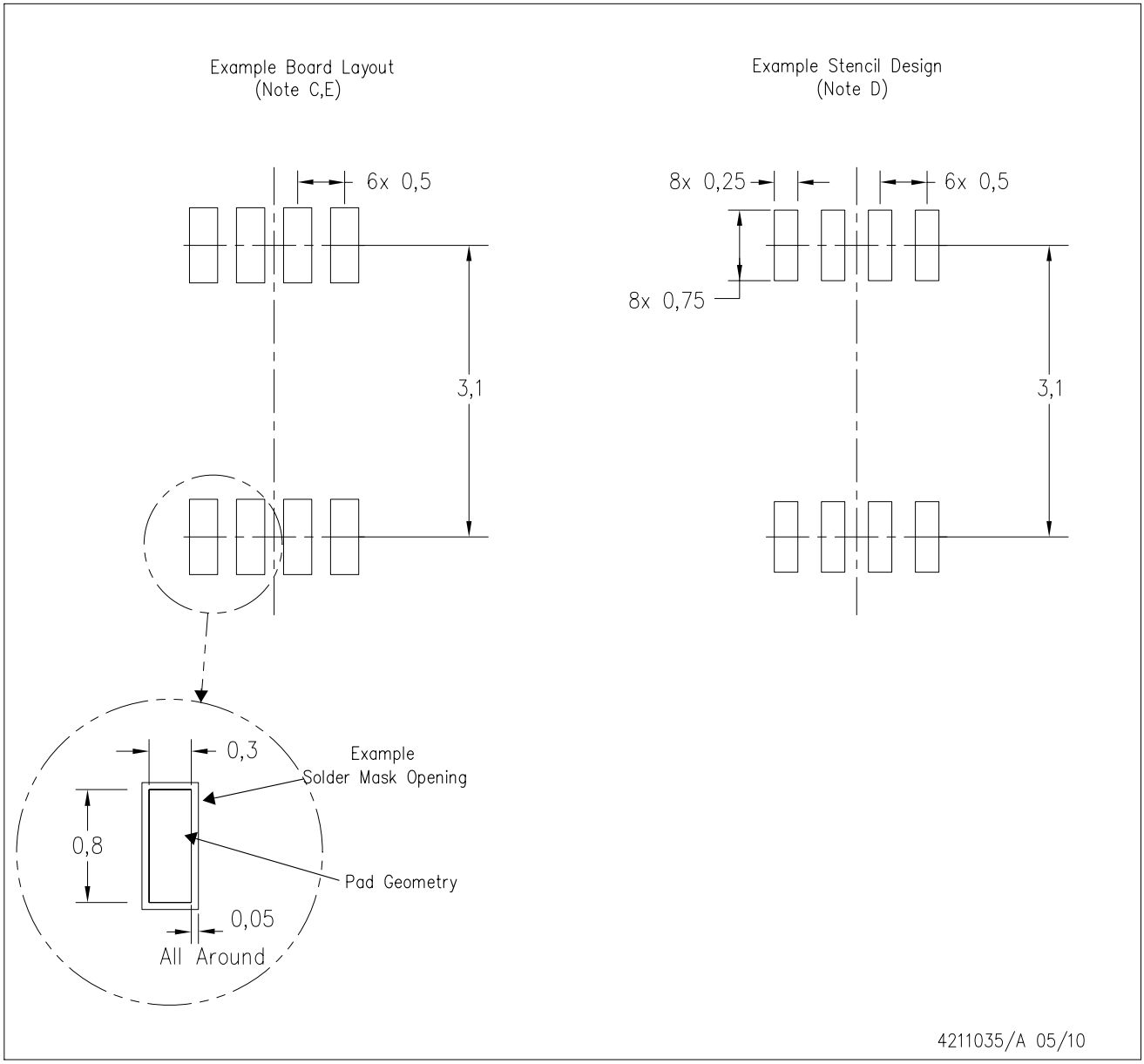
DDU (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4205140/A 05/03

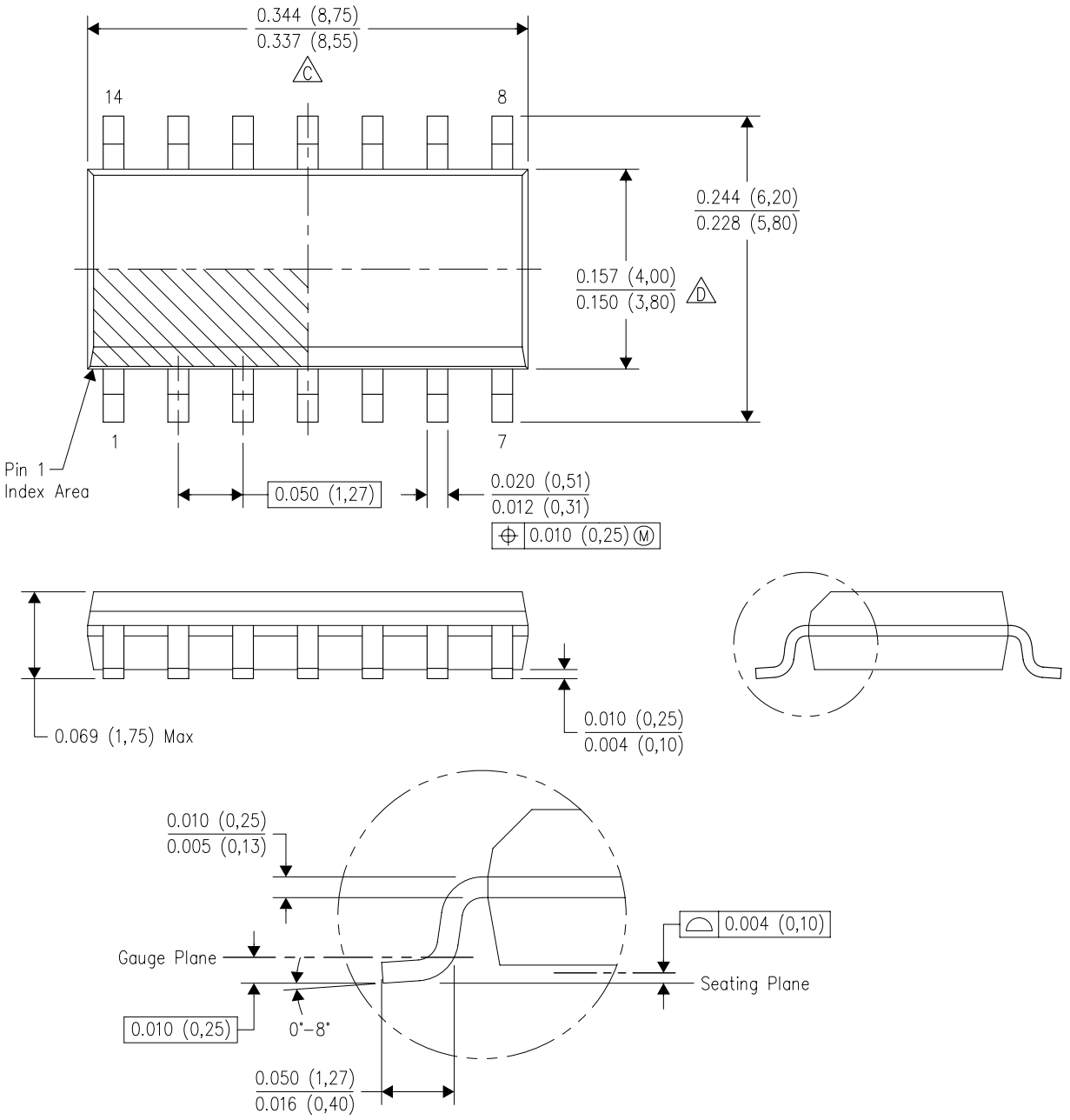
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation CA.

DDU (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE (DIE UP)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

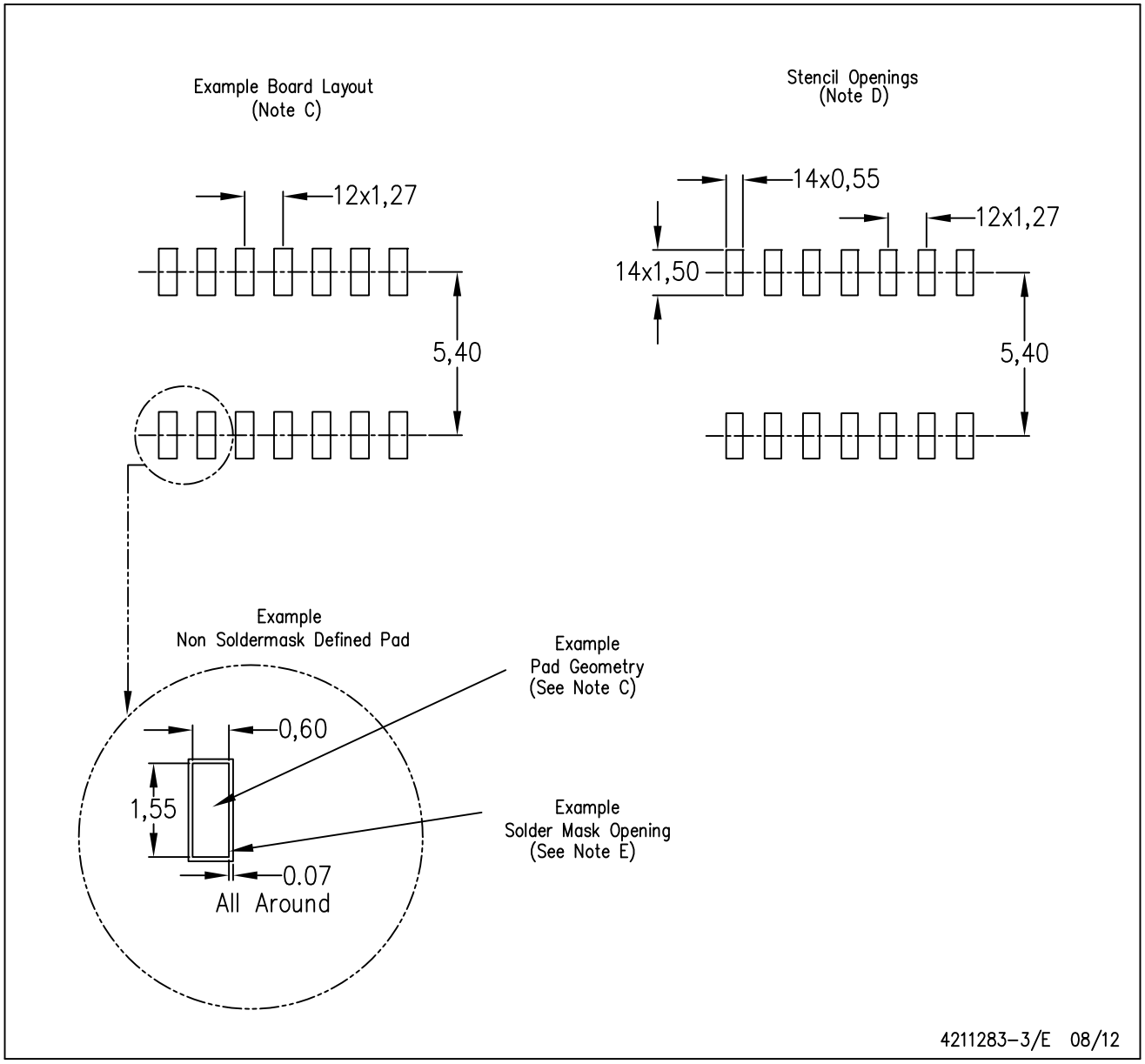
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

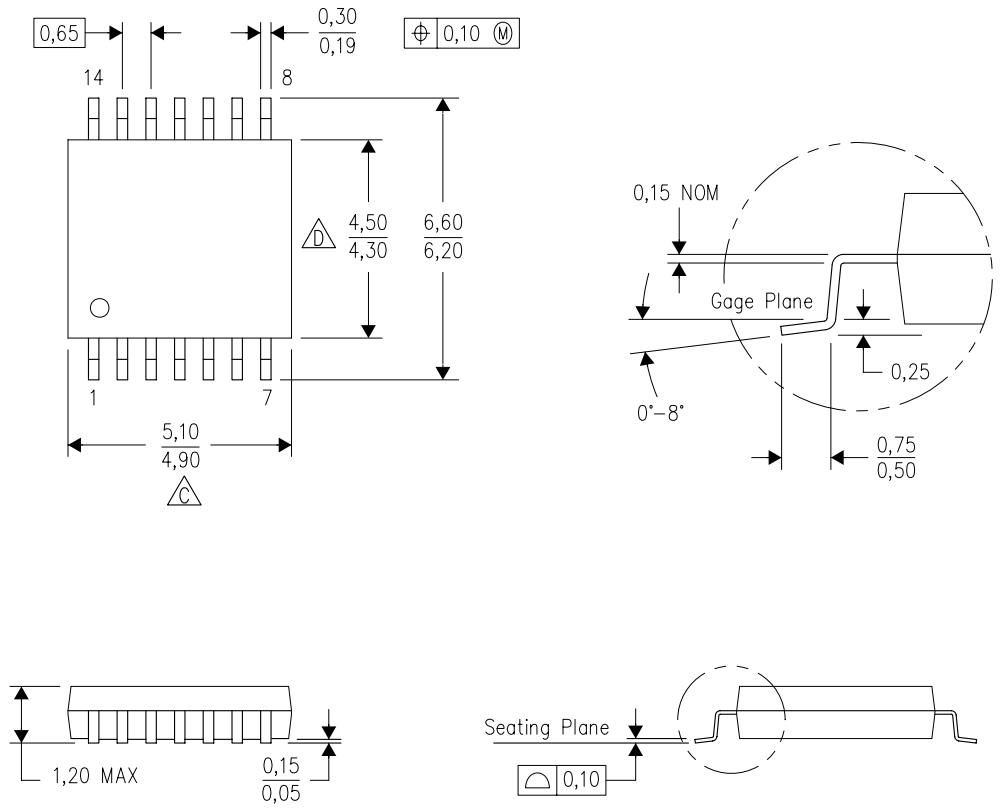
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

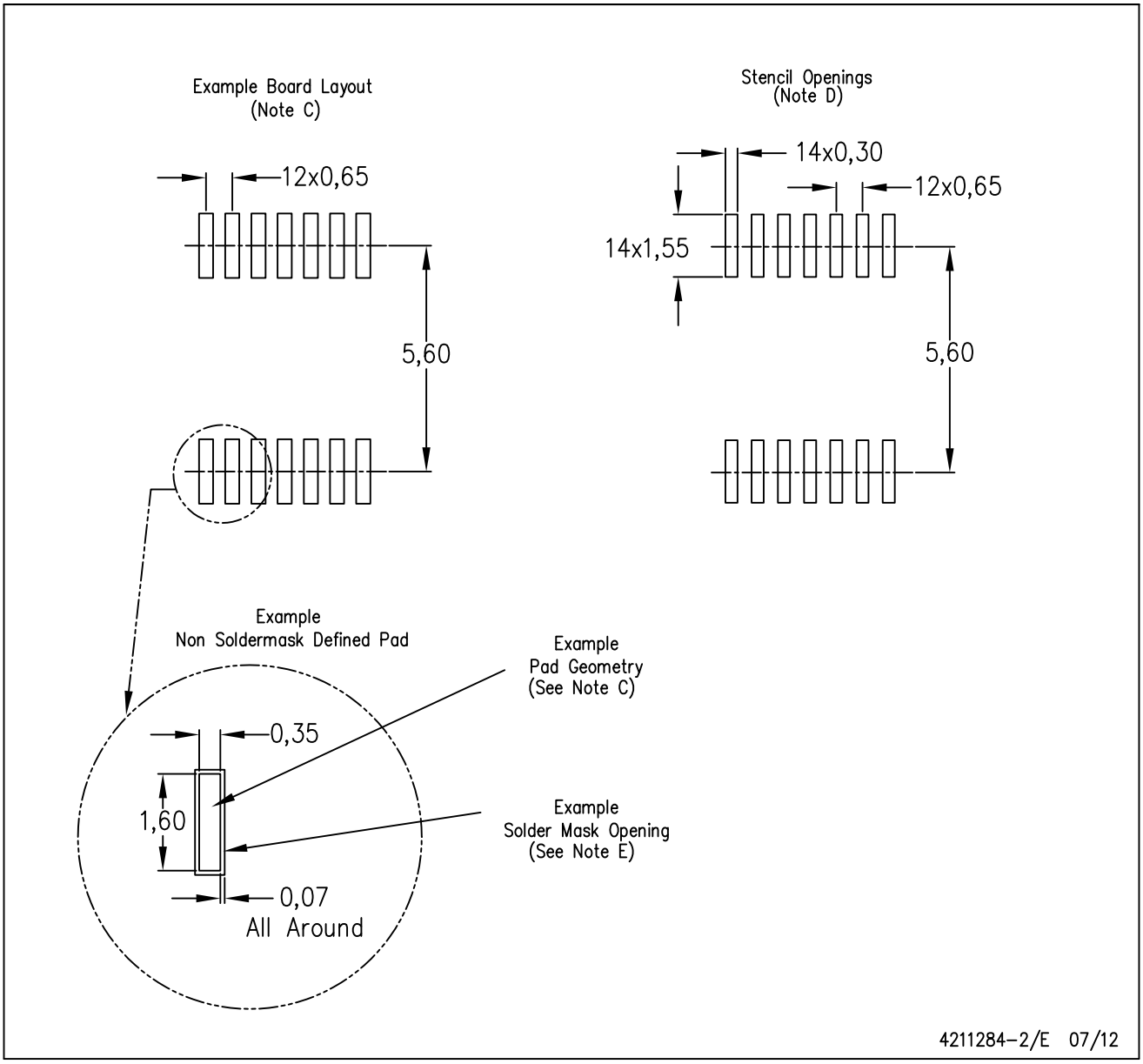
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

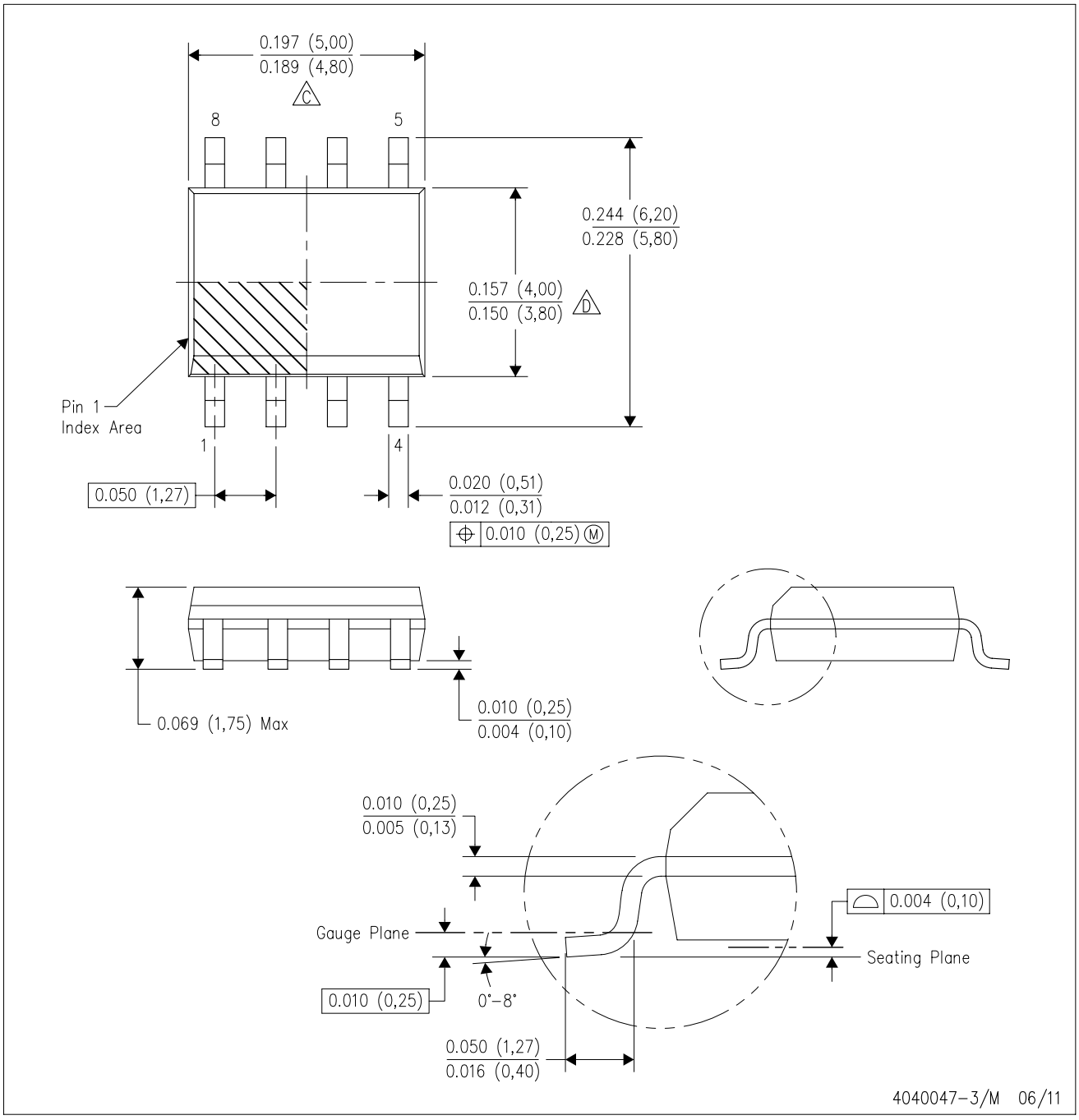
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



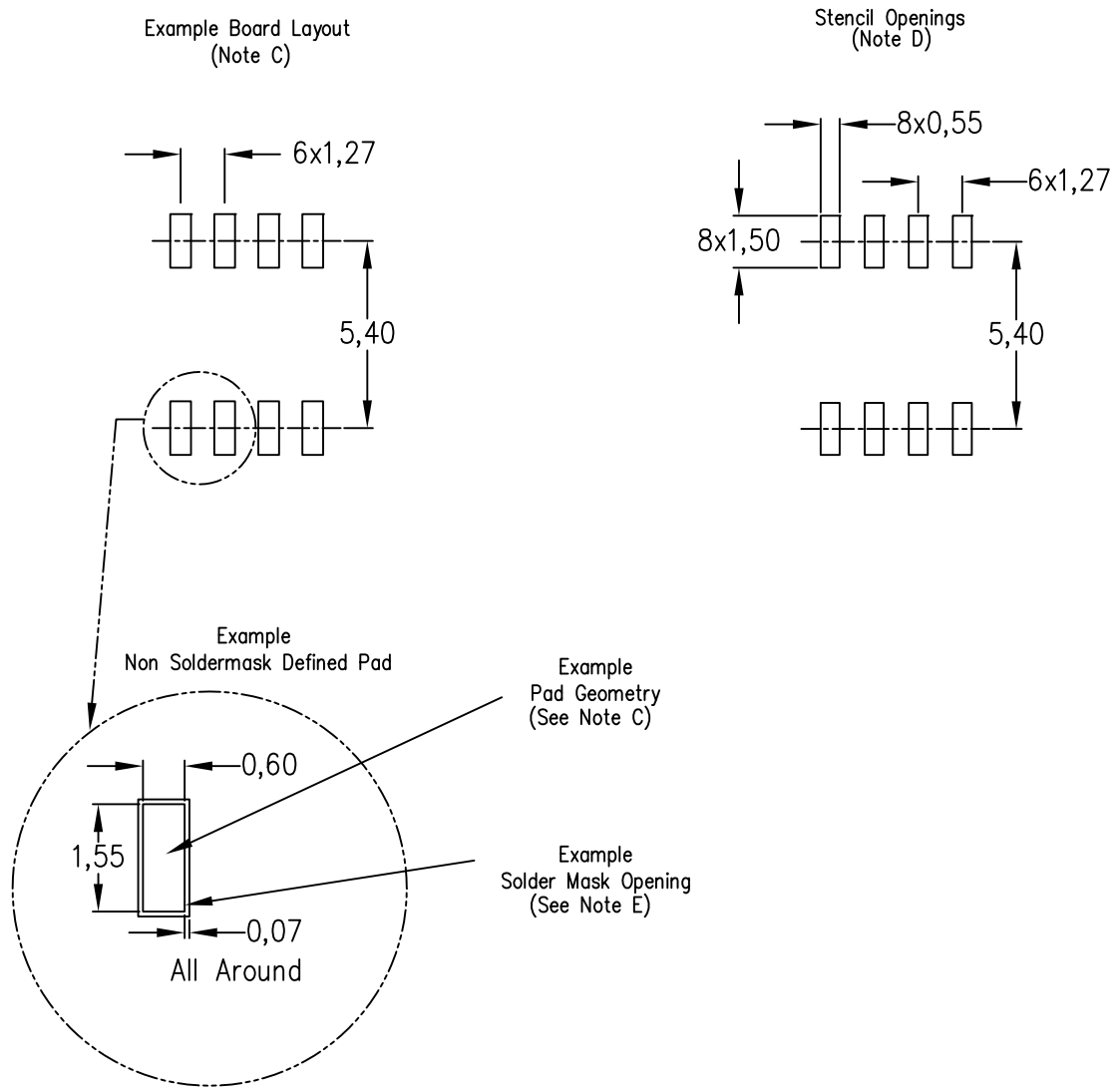
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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