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Jameco Part Number 1352892

FEATURES

- ESD Protection for RS-232 Bus Pins
 - ± 15 -kV Human-Body Model (HBM)
 - ± 8 -kV IEC61000-4-2, Contact Discharge
 - ± 15 -kV IEC61000-4-2, Air-Gap Discharge
- Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU v.28 Standards
- Operates With 3-V to 5.5-V V_{CC} Supply
- Operates up to 500 kbit/s
- Two Drivers and Two Receivers
- Low Standby Current . . . 1 μ A Typ
- External Capacitors . . . $4 \times 0.1 \mu$ F
- Accepts 5-V Logic Input With 3.3-V Supply
- Alternative High-Speed Pin-Compatible Device (1 Mbit/s) for SNx5C3222E

APPLICATIONS

- Battery-Powered Systems
- PDAs
- Notebooks
- Laptops
- Palmtop PCs
- Hand-Held Equipment

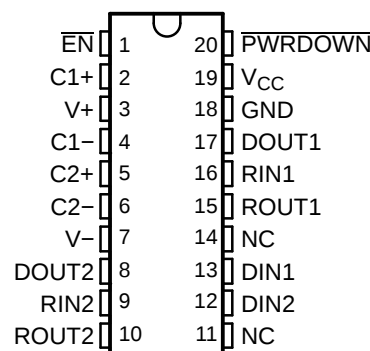
DESCRIPTION/ORDERING INFORMATION

The MAX3222E consists of two line drivers, two line receivers, and a dual charge-pump circuit with ± 15 -kV ESD protection pin to pin (serial-port connection pins, including GND).

The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The device operates at typical data signaling rates up to 500 kbit/s and a maximum of 30-V/ μ s driver output slew rate.

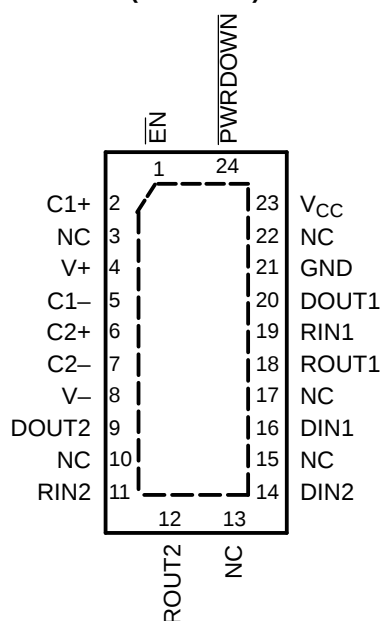
The MAX3222E can be placed in the power-down mode by setting the power-down ($\overline{\text{PWRDOWN}}$) input low, which draws only 1 μ A from the power supply. When the device is powered down, the receivers remain active while the drivers are placed in the high-impedance state. Also, during power down, the onboard charge pump is disabled; $V+$ is lowered to V_{CC} , and $V-$ is raised toward GND. Receiver outputs also can be placed in the high-impedance state by setting enable ($\overline{\text{EN}}$) high.

DB, DW, OR PW PACKAGE
(TOP VIEW)



NC – No internal connection

RHL PACKAGE
(TOP VIEW)



NC – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

MAX3222E
3-V TO 5.5-V MULTICHANNEL RS-232 LINE DRIVER/RECEIVER
WITH ± 15 -kV ESD PROTECTION

SLLS708 – JANUARY 2006

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	SOIC – DW	Tube of 25	MAX3222ECDW	MAX3222EC
		Reel of 2000	MAX3222ECDWR	
	SSOP – DB	Tube of 70	MAX3222ECDB	MP222EC
		Reel of 2000	MAX3222ECDBR	
	TSSOP – PW	Tube of 70	MAX3222ECPW	MP222EC
		Reel of 2000	MAX3222ECPWR	
–40°C to 85°C	SOIC – DW	Tube of 25	MAX3222EIDW	MAX3222EI
		Reel of 2000	MAX3222EIDWR	
	SSOP – DB	Tube of 70	MAX3222EIDB	MP222EI
		Reel of 2000	MAX3222EIDBR	
	TSSOP – PW	Tube of 70	MAX3222EIPW	MP222EI
		Reel of 2000	MAX3222EIPWR	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLES

EACH DRIVER⁽¹⁾

INPUTS		OUTPUT DOUT
DIN	PWRDOWN	
X	L	Z
L	H	H
H	H	L

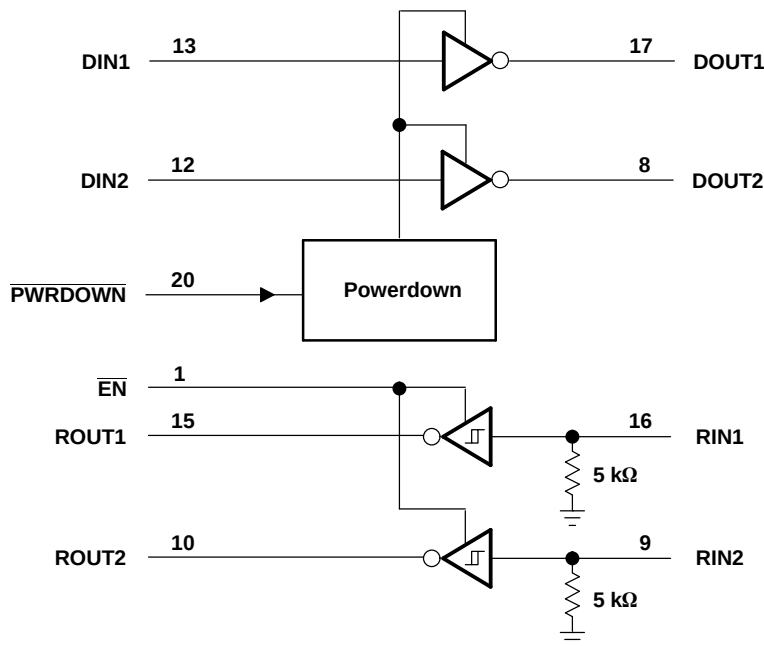
(1) H = high level, L = low level, X = irrelevant, Z = high impedance

EACH RECEIVER⁽¹⁾

INPUTS		OUTPUT ROUT
RIN	$\overline{EN}$	
L	L	H
H	L	L
X	H	Z
Open	L	H

(1) H = high level, L = low level, X = irrelevant,
Z = high impedance (off),
Open = input disconnected or connected driver off

LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers are for the DB, DW, and PW packages.

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range ⁽²⁾		-0.3	6	V
V_{+}	Positive-output supply voltage range ⁽²⁾		-0.3	7	V
V_{-}	Negative-output supply voltage range ⁽²⁾		0.3	-7	V
$V_{+} - V_{-}$	Supply voltage difference ⁽²⁾			13	V
V_I	Input voltage range	Driver ($\overline{EN}$, $\overline{PWRDOWN}$)	-0.3	6	V
		Receiver	-25	25	
V_O	Output voltage range	Driver	-13.2	13.2	V
		Receiver	-0.3	$V_{CC} + 0.3$	
θ_{JA}	Package thermal impedance ⁽³⁾⁽⁴⁾	DB package		70	°C/W
		DW package		58	
		PW package		83	
		RHL package		TBD	
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature range		-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network GND.
- (3) Maximum power dissipation is a function of $T_J(\max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

MAX3222E

3-V TO 5.5-V MULTICHANNEL RS-232 LINE DRIVER/RECEIVER

WITH ± 15 -kV ESD PROTECTION

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Recommended Operating Conditions⁽¹⁾

See [Figure 5](#)

			MIN	NOM	MAX	UNIT
Supply voltage		$V_{CC} = 3.3\text{ V}$	3	3.3	3.6	V
		$V_{CC} = 5\text{ V}$	4.5	5	5.5	
V_{IH}	Driver and control high-level input voltage	$\overline{DIN}$, $\overline{EN}$, $\overline{PWRDOWN}$	$V_{CC} = 3.3\text{ V}$		2	V
			$V_{CC} = 5\text{ V}$		2.4	
V_{IL}	Driver and control low-level input voltage	$\overline{DIN}$, $\overline{EN}$, $\overline{PWRDOWN}$			0.8	V
V_I	Driver and control input voltage	$\overline{DIN}$, $\overline{EN}$, $\overline{PWRDOWN}$	0		5.5	V
V_I	Receiver input voltage		–25		25	V
T_A	Operating free-air temperature	MAX3222EC	0		70	°C
		MAX3222EI	–40		85	

(1) Test conditions are $C1$ – $C4 = 0.1\text{ }\mu\text{F}$ at $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$; $C1 = 0.047\text{ }\mu\text{F}$, $C2$ – $C4 = 0.33\text{ }\mu\text{F}$ at $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$.

Electrical Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5](#))

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
I_I	Input leakage current ($\overline{EN}$, $\overline{PWRDOWN}$)		± 0.01		± 1	μA
I_{CC}	Supply current	No load, $\overline{PWRDOWN}$ at V_{CC}	0.3		1	mA
	Supply current (powered off)	No load, $\overline{PWRDOWN}$ at GND	1		10	μA

(1) Test conditions are $C1$ – $C4 = 0.1\text{ }\mu\text{F}$ at $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$; $C1 = 0.047\text{ }\mu\text{F}$, $C2$ – $C4 = 0.33\text{ }\mu\text{F}$ at $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$.

(2) All typical values are at $V_{CC} = 3.3\text{ V}$ or $V_{CC} = 5\text{ V}$, and $T_A = 25^\circ\text{C}$.

DRIVER SECTION

Electrical Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5](#))

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
V _{OH}	High-level output voltage	DOUT at R _L = 3 k Ω to GND, DIN = GND	5	5.4		V
V _{OL}	Low-level output voltage	DOUT at R _L = 3 k Ω to GND, DIN = V _{CC}	–5	–5.4		V
I _{IH}	High-level input current	V _I = V _{CC}		± 0.01	± 1	μ A
I _{IL}	Low-level input current	V _I at GND		± 0.01	± 1	μ A
I _{OS}	Short-circuit output current ⁽³⁾	V _{CC} = 3.6 V		± 35	± 60	mA
		V _{CC} = 5.5 V				
r _o	Output resistance	V _{CC} , V ₊ , and V _– = 0 V, V _O = ± 2 V	300	10M		Ω
I _{OZ}	Output leakage current	$\overline{\text{PWRDOWN}}$ = GND, V _{CC} = 3 V to 3.6 V, V _O = ± 12 V			± 25	μ A
		V _{CC} = 4.5 V to 5.5 V, V _O = ± 10 V			± 25	

(1) Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 3.3 V $\pm$ 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V_{CC} = 5 V $\pm$ 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(3) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

Switching Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5](#))

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
	Maximum data rate	C _L = 1000 pF, One DOUT switching, R _L = 3 k Ω , See Figure 1	250	500		kbit/s
t _{sk(p)}	Pulse skew ⁽³⁾	C _L = 150 pF to 2500 pF, R _L = 3 k Ω to 7 k Ω , See Figure 2		300		ns
SR(tr)	Slew rate, transition region (see Figure 1)	R _L = 3 k Ω to 7 k Ω , V _{CC} = 3.3 V, C _L = 150 pF to 1000 pF	6		30	V/ μ s
		C _L = 150 pF to 2500 pF	4		30	

(1) Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 3.3 V $\pm$ 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V_{CC} = 5 V $\pm$ 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(3) Pulse skew is defined as |t_{PLH} – t_{PHL}| of each channel of the same device.

MAX3222E

3-V TO 5.5-V MULTICHANNEL RS-232 LINE DRIVER/RECEIVER

WITH ± 15 -kV ESD PROTECTION

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RECEIVER SECTION

Electrical Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5](#))

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
V _{OH}	High-level output voltage	I _{OH} = –1 mA	V _{CC} – 0.6	V _{CC} – 0.1		V
V _{OL}	Low-level output voltage	I _{OL} = 1.6 mA			0.4	V
V _{IT+}	Positive-going input threshold voltage	V _{CC} = 3.3 V		1.5	2.4	V
		V _{CC} = 5 V		1.8	2.4	
V _{IT–}	Negative-going input threshold voltage	V _{CC} = 3.3 V	0.6	1.2		V
		V _{CC} = 5 V	0.8	1.5		
V _{hys}	Input hysteresis (V _{IT+} – V _{IT–})			0.3		V
I _{OZ}	Output leakage current	$\overline{\text{EN}} = 1$		±0.05	±10	μA
r _i	Input resistance	V _I = ±3 V to ±25 V	3	5	7	kΩ

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

Switching Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

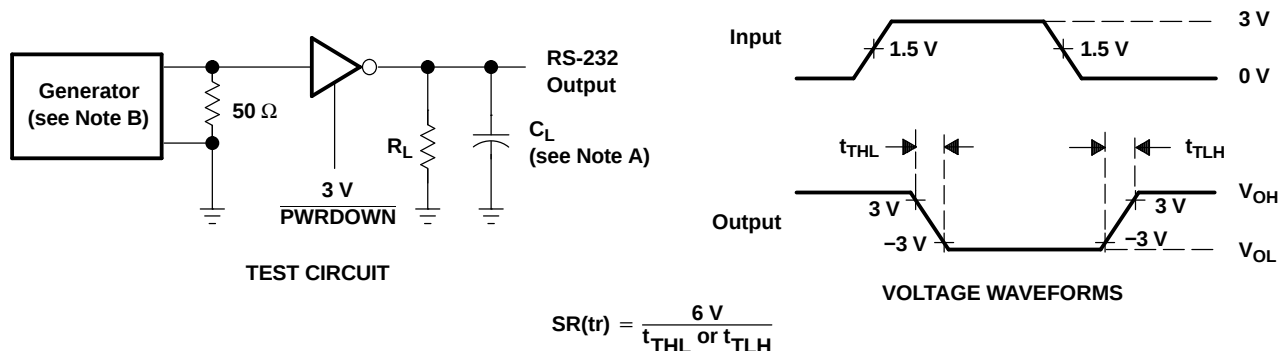
PARAMETER		TEST CONDITIONS	TYP ⁽²⁾	UNIT
t _{PLH}	Propagation delay time, low- to high-level output	C _L = 150 pF, See Figure 3	300	ns
t _{PHL}	Propagation delay time, high- to low-level output	C _L = 150 pF, See Figure 3	300	ns
t _{en}	Output enable time	C _L = 150 pF, R _L = 3 kΩ, See Figure 4	200	ns
t _{dis}	Output disable time	C _L = 150 pF, R _L = 3 kΩ, See Figure 4	200	ns
t _{sk(p)}	Pulse skew ⁽³⁾	See Figure 3	300	ns

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

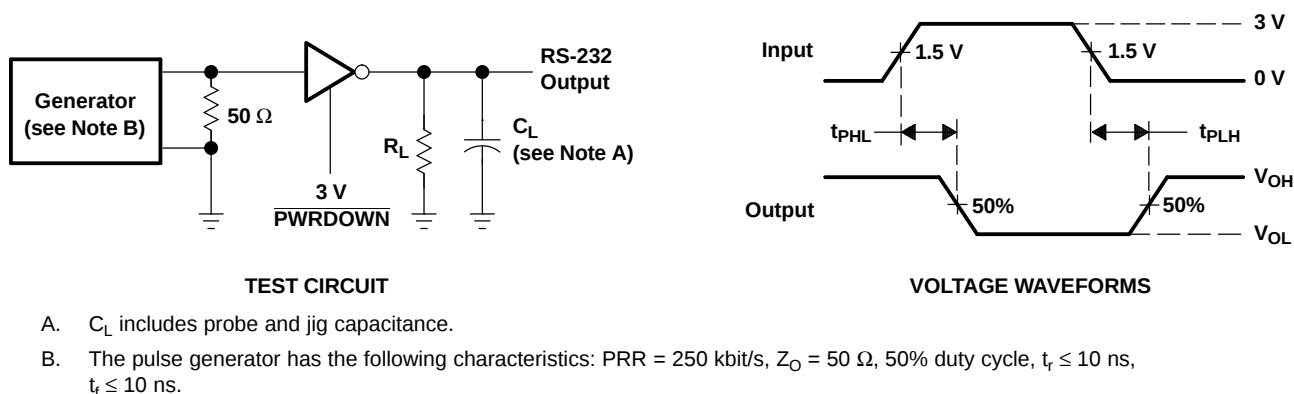
(3) Pulse skew is defined as |t_{PLH} – t_{PHL}| of each channel of the same device.

PARAMETER MEASUREMENT INFORMATION



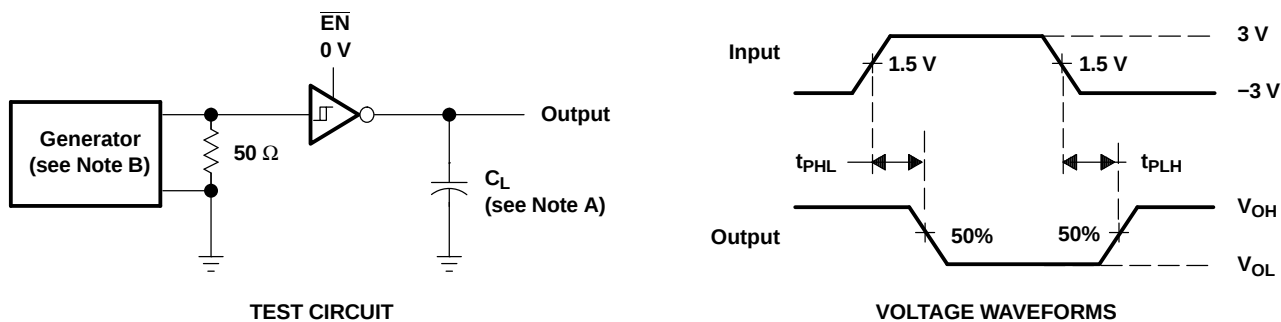
- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

Figure 1. Driver Slew Rate



- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

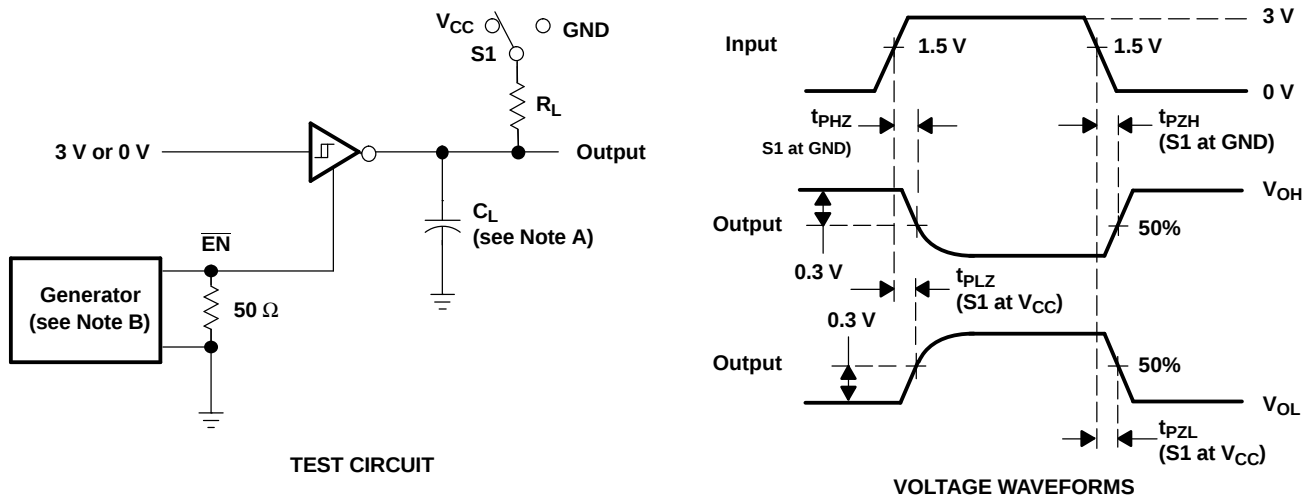
Figure 2. Driver Pulse Skew



- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

Figure 3. Receiver Propagation Delay Times

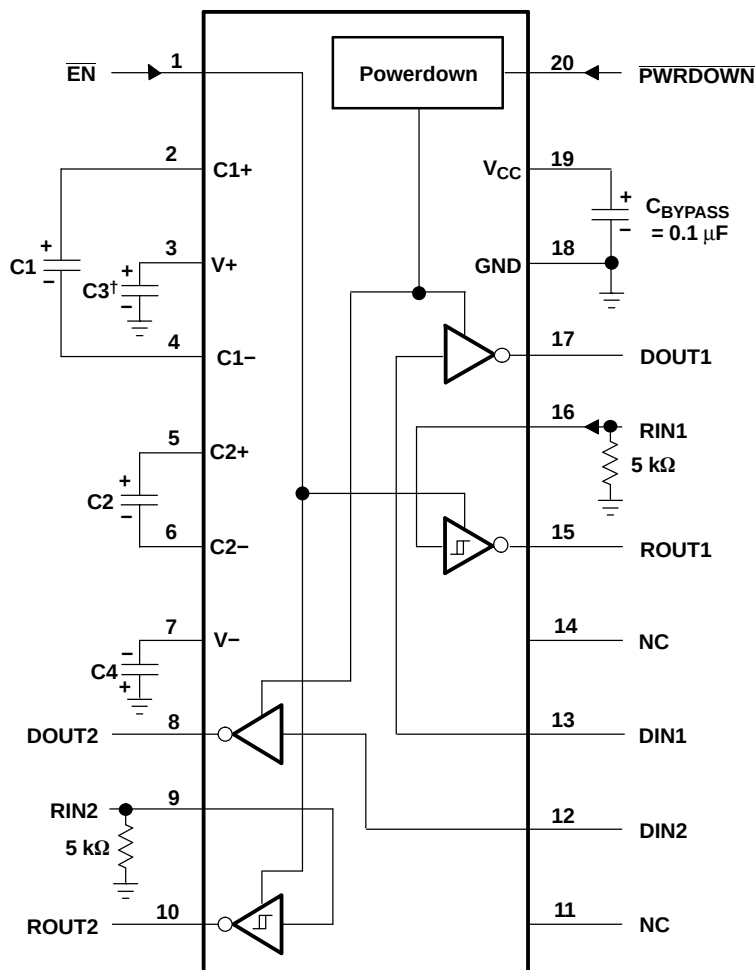
PARAMETER MEASUREMENT INFORMATION (continued)



- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

Figure 4. Receiver Enable and Disable Times

APPLICATION INFORMATION



[†] C3 can be connected to V_{CC} or GND.

NOTES: A. Resistor values shown are nominal.

B. NC – No internal connection

C. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

V_{CC} vs CAPACITOR VALUES

V_{CC}	C1	C2, C3, and C4
3.3 V $\pm$ 0.3 V	0.1 μ F	0.1 μ F
5 V $\pm$ 0.5 V	0.047 μ F	0.33 μ F
3 V to 5.5 V	0.1 μ F	0.47 μ F

Figure 5. Typical Operating Circuit and Capacitor Values

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
MAX3222ECDB	ACTIVE	SSOP	DB	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3222ECDBG4	ACTIVE	SSOP	DB	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3222ECDBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3222ECDBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3222ECDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3222ECDWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3222ECDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3222ECDWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3222ECPW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3222ECPWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3222ECPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3222ECPWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3222ECRHLR	PREVIEW	QFN	RHL	24	1000	TBD	Call TI	Call TI
MAX3222EIDB	ACTIVE	SSOP	DB	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3222EIDBG4	ACTIVE	SSOP	DB	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3222EIDBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3222EIDBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3222EIDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3222EIDWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3222EIDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3222EIDWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3222EIPW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3222EIPWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3222EIPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3222EIPWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
MAX3222EIRHLR	PREVIEW	QFN	RHL	24	1000	TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

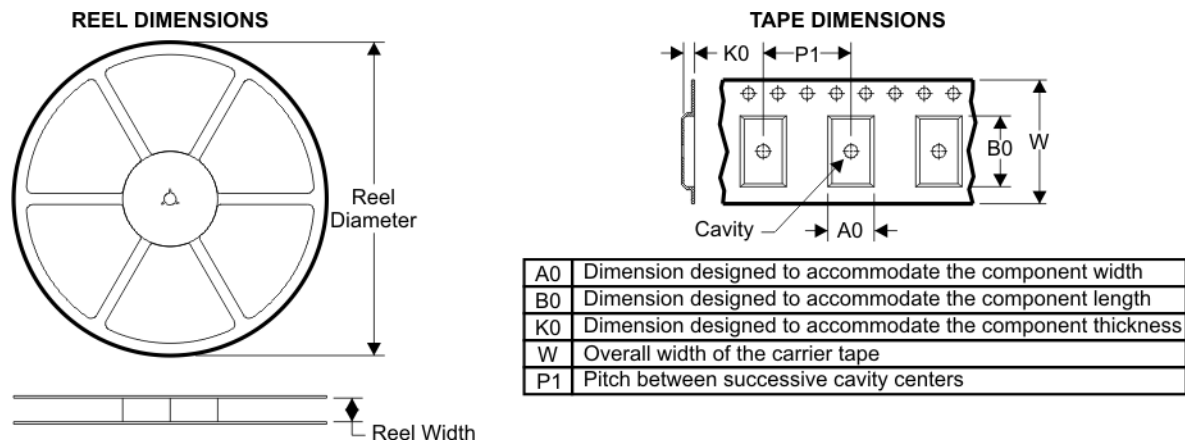
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

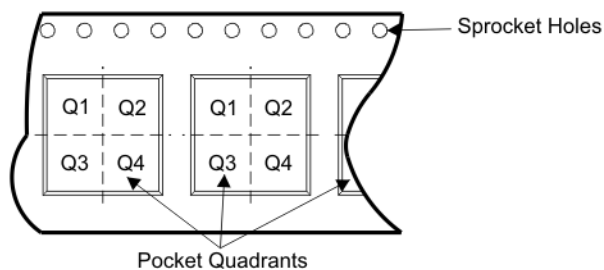
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TAPE AND REEL BOX INFORMATION

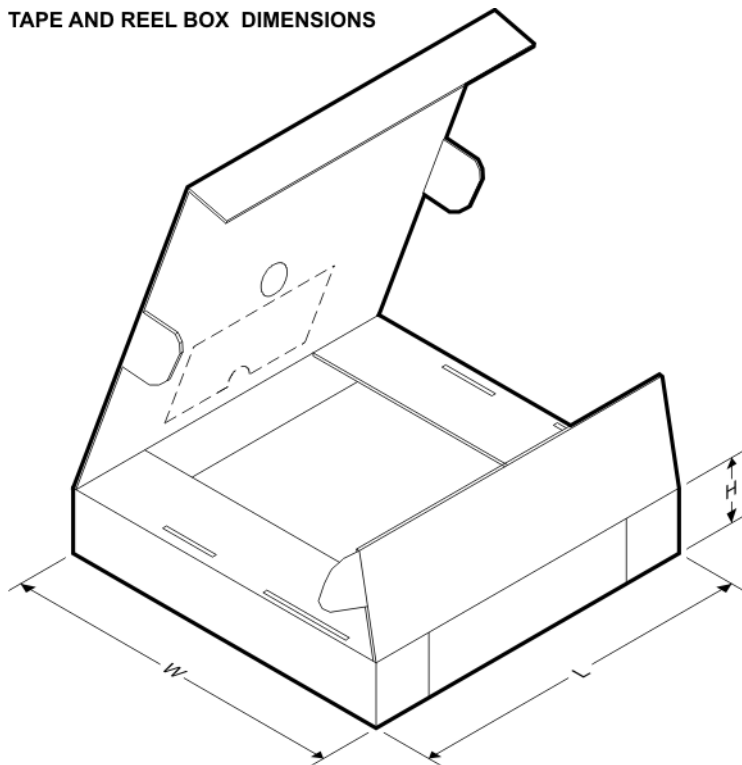


QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MAX3222ECDBR	DB	20	SITE 41	330	16	8.0	8.0	3.0	12	16	Q1
MAX3222ECDWR	DW	20	SITE 41	330	24	11.0	13.0	3.0	12	24	Q1
MAX3222ECPWR	PW	20	SITE 41	330	16	7.0	7.0	2.0	8	16	Q1
MAX3222EIDBR	DB	20	SITE 41	330	16	8.0	8.0	3.0	12	16	Q1
MAX3222EIDWR	DW	20	SITE 41	330	24	11.0	13.0	3.0	12	24	Q1
MAX3222EIPWR	PW	20	SITE 41	330	16	7.0	7.0	2.0	8	16	Q1

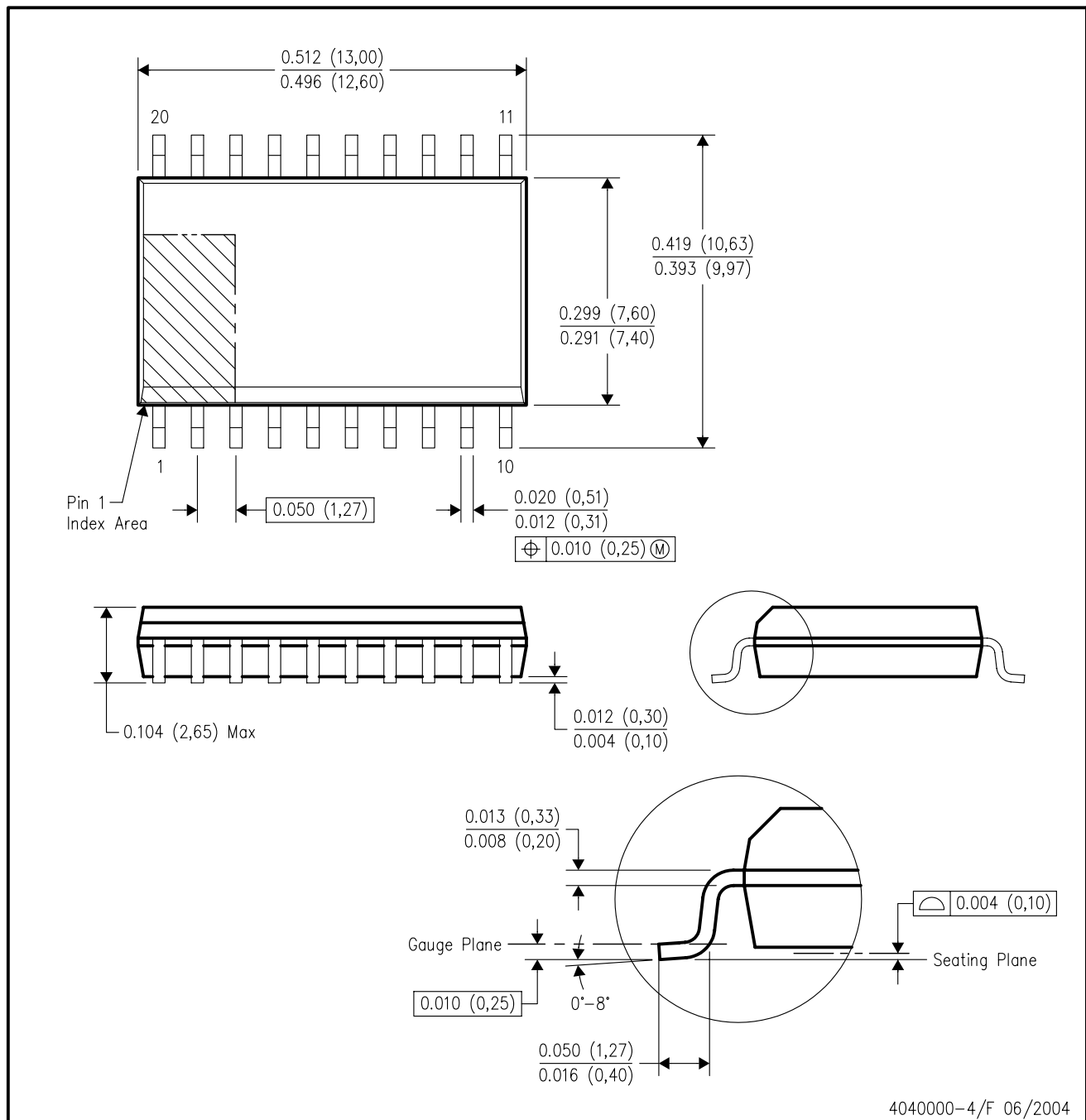
TAPE AND REEL BOX DIMENSIONS



Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
MAX3222ECDBR	DB	20	SITE 41	346.0	346.0	33.0
MAX3222ECDWR	DW	20	SITE 41	346.0	346.0	41.0
MAX3222ECPWR	PW	20	SITE 41	346.0	346.0	33.0
MAX3222EIDBR	DB	20	SITE 41	346.0	346.0	33.0
MAX3222EIDWR	DW	20	SITE 41	346.0	346.0	41.0
MAX3222EIPWR	PW	20	SITE 41	346.0	346.0	33.0

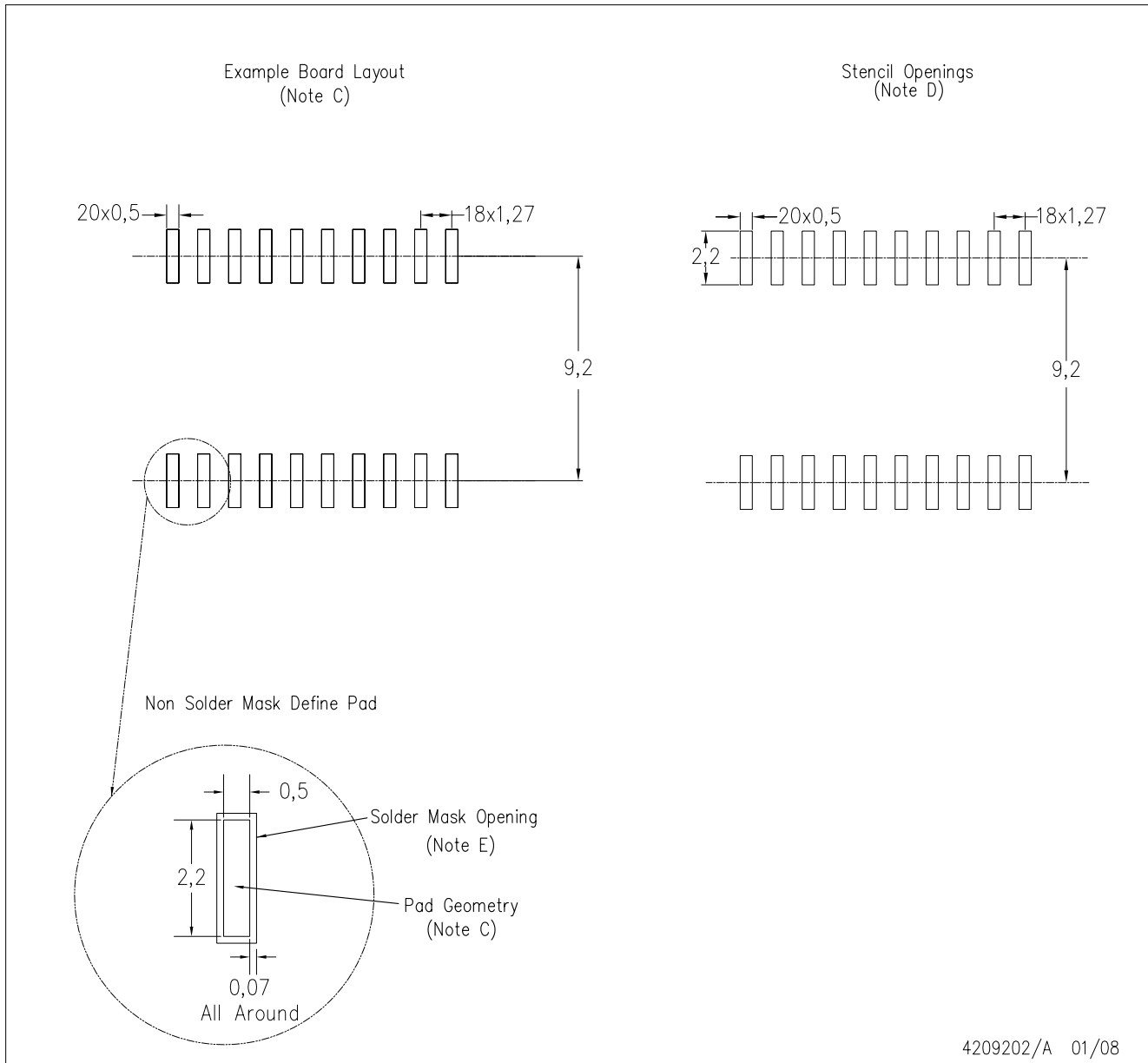
DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AC.

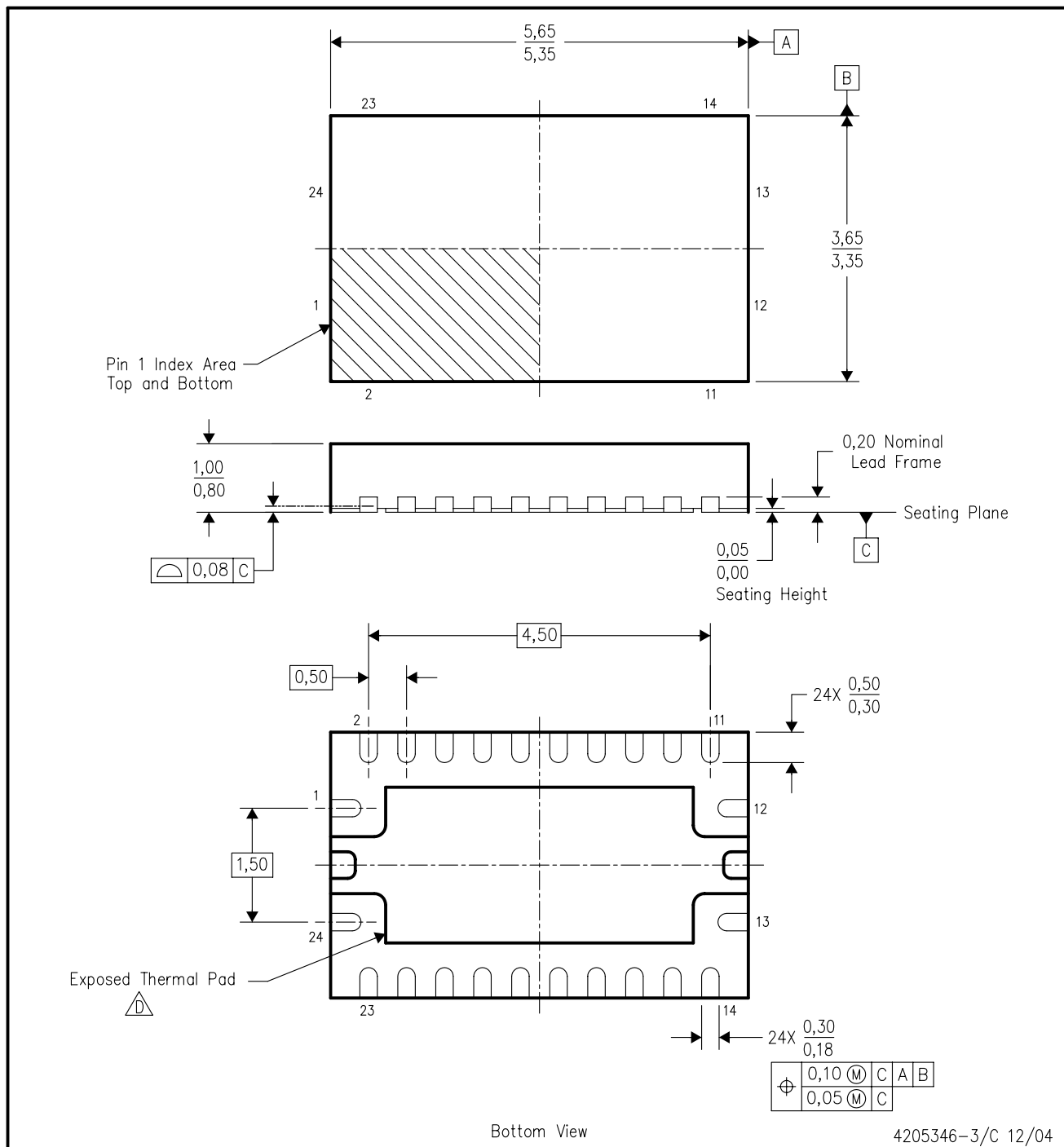
DW (R-PDSO-G20)



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RHL (R-PQFP-N24)

PLASTIC QUAD FLATPACK



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
 - JEDEC MO-241 package registration pending.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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