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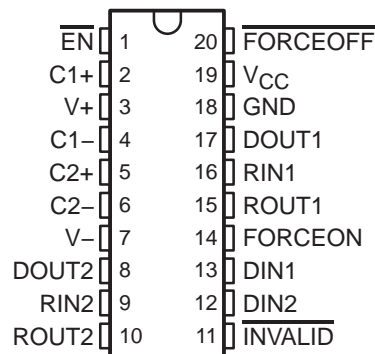
Jameco Part Number 1353019

3-V TO 5.5-V MULTICHANNEL RS-232 LINE DRIVER/RECEIVER WITH ± 15 -kV ESD PROTECTION

SLLS409K – JANUARY 2000 – REVISED MARCH 2004

- RS-232 Bus-Pin ESD Protection Exceeds ± 15 kV Using Human-Body Model (HBM)
- Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU v.28 Standards
- Operates With 3-V to 5.5-V V_{CC} Supply
- Operates Up To 250 kbit/s
- Two Drivers and Two Receivers
- Low Standby Current . . . 1 μ A Typical
- External Capacitors . . . $4 \times 0.1 \mu$ F
- Accepts 5-V Logic Input With 3.3-V Supply
- Alternative High-Speed Pin-Compatible Device (1 Mbit/s)
 - SNx5C3223
- Applications
 - Battery-Powered Systems, PDAs, Notebooks, Laptops, Palmtop PCs, and Hand-Held Equipment

DB, DW, OR PW PACKAGE
(TOP VIEW)



description/ordering information

The MAX3223 consists of two line drivers, two line receivers, and a dual charge-pump circuit with ± 15 -kV ESD protection pin to pin (serial-port connection pins, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The device operates at data signaling rates up to 250 kbit/s and a maximum of 30-V/ μ s driver output slew rate.

ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–0°C to 70°C	SOIC (DW)	Tube of 25	MAX3223CDW	MAX3223C
		Reel of 2000	MAX3223CDWR	
	SSOP (DB)	Tube of 70	MAX3223CDB	MA3223C
		Reel of 2000	MAX3223CDBR	
	TSSOP (PW)	Tube of 70	MAX3223CPW	MA3223C
		Reel of 2000	MAX3223CPWR	
–40°C to 85°C	SOIC (DW)	Tube of 25	MAX3223IDW	MAX3223I
		Reel of 2000	MAX3223IDWR	
	SSOP (DB)	Tube of 70	MAX3223IDB	MB3223I
		Reel of 2000	MAX3223IDBR	
	TSSOP (PW)	Tube of 70	MAX3223IPW	MB3223I
		Reel of 2000	MAX3223IPWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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MAX3223

3-V TO 5.5-V MULTICHANNEL RS-232 LINE DRIVER/RECEIVER

WITH ± 15 -kV ESD PROTECTION

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description/ordering information (continued)

Flexible control options for power management are available when the serial port is inactive. The auto-powerdown feature functions when FORCEON is low and $\overline{\text{FORCEOFF}}$ is high. During this mode of operation, if the device does not sense a valid RS-232 signal, the driver outputs are disabled. If $\overline{\text{FORCEOFF}}$ is set low and $\overline{\text{EN}}$ is high, both drivers and receivers are shut off, and the supply current is reduced to 1 μA . Disconnecting the serial port or turning off the peripheral drivers causes auto-powerdown to occur. Auto-powerdown can be disabled when FORCEON and $\overline{\text{FORCEOFF}}$ are high. With auto-powerdown enabled, the device is activated automatically when a valid signal is applied to any receiver input. The $\overline{\text{INVALID}}$ output is used to notify the user if an RS-232 signal is present at any receiver input. $\overline{\text{INVALID}}$ is high (valid data) if any receiver input voltage is greater than 2.7 V or less than -2.7 V, or has been between -0.3 V and 0.3 V for less than 30 μs . $\overline{\text{INVALID}}$ is low (invalid data) if the receiver input voltage is between -0.3 V and 0.3 V for more than 30 μs . Refer to Figure 4 for receiver input levels.

Function Tables

EACH DRIVER

INPUTS				OUTPUT DOUT	DRIVER STATUS
DIN	FORCEON	$\overline{\text{FORCEOFF}}$	VALID RIN RS-232 LEVEL		
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with auto-powerdown disabled
H	H	H	X	L	
L	L	H	Yes	H	Normal operation with auto-powerdown enabled
H	L	H	Yes	L	
L	L	H	No	Z	Powered off by auto-powerdown feature
H	L	H	No	Z	

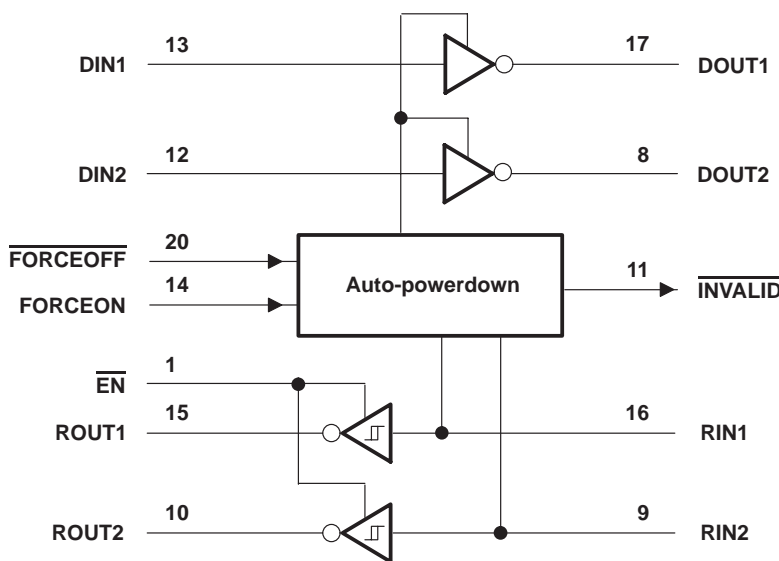
H = high level, L = low level, X = irrelevant, Z = high impedance

EACH RECEIVER

INPUTS			OUTPUT ROUT
RIN	$\overline{\text{EN}}$	VALID RIN RS-232 LEVEL	
L	L	X	H
H	L	X	L
X	H	X	Z
Open	L	No	H

H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)	–0.3 V to 6 V
Positive output supply voltage range, $V+$ (see Note 1)	–0.3 V to 7 V
Negative output supply voltage range, $V-$ (see Note 1)	0.3 V to –7 V
Supply voltage difference, $V+ - V-$ (see Note 1)	13 V
Input voltage range, V_I : Driver, FORCEOFF, FORCEON, \overline{EN}	–0.3 V to 6 V
Receiver	–25 V to 25 V
Output voltage range, V_O : Driver	–13.2 V to 13.2 V
Receiver, INVALID	–0.3 V to $V_{CC} + 0.3$ V
Package thermal impedance, θ_{JA} (see Notes 2 and 3): DB package	70°C/W
DW package	58°C/W
PW package	83°C/W
Operating virtual junction temperature, T_J	150°C
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltages are with respect to network GND.
 2. Maximum power dissipation is a function of $T_J(\max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.

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recommended operating conditions (see Note 4 and Figure 6)

			MIN	NOM	MAX	UNIT
Supply voltage		$V_{CC} = 3.3\text{ V}$	3	3.3	3.6	V
		$V_{CC} = 5\text{ V}$	4.5	5	5.5	
V_{IH}	Driver and control high-level input voltage	DIN, \overline{EN} , $\overline{FORCEOFF}$, FORCEON	$V_{CC} = 3.3\text{ V}$	2		V
			$V_{CC} = 5\text{ V}$	2.4		
V_{IL}	Driver and control low-level input voltage	DIN, \overline{EN} , $\overline{FORCEOFF}$, FORCEON			0.8	V
V_I	Driver and control input voltage	DIN, \overline{EN} , $\overline{FORCEOFF}$, FORCEON	0		5.5	V
	Receiver input voltage		-25		25	
T_A	Operating free-air temperature	MAX3223C	0		70	°C
		MAX3223I	-40		85	

NOTE 4: Test conditions are C1–C4 = 0.1 μF at $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$; C1 = 0.047 μF , C2–C4 = 0.33 μF at $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$.**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 6)**

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
I_I	Input leakage current	\overline{EN} , $\overline{FORCEOFF}$, FORCEON			± 0.01	± 1	μA
I_{CC}	Supply current	Auto-powerdown disabled	$V_{CC} = 3.3\text{ V or } 5\text{ V}$, $T_A = 25^\circ\text{C}$	No load, $\overline{FORCEOFF}$ and FORCEON at V_{CC}	0.3	1	mA
	Powered off	No load, $\overline{FORCEOFF}$ at GND		1	10	μA	
	Auto-powerdown enabled	No load, $\overline{FORCEOFF}$ at V_{CC} , FORCEON at GND, All RIN are open or grounded		1	10		

† All typical values are at $V_{CC} = 3.3\text{ V}$ or $V_{CC} = 5\text{ V}$, and $T_A = 25^\circ\text{C}$.NOTE 4: Test conditions are C1–C4 = 0.1 μF at $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$; C1 = 0.047 μF , C2–C4 = 0.33 μF at $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$.

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WITH ±15-kV ESD PROTECTION
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DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 6)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V _{OH}	High-level output voltage	DOUT at R _L = 3 kΩ to GND	5	5.4		V
V _{OL}	Low-level output voltage	DOUT at R _L = 3 kΩ to GND	-5	-5.4		V
I _{IH}	High-level input current	V _I = V _{CC}		±0.01	±1	μA
I _{IL}	Low-level input current	V _I at GND		±0.01	±1	μA
I _{OS}	Short-circuit output current‡	V _{CC} = 3.6 V, V _O = 0 V		±35	±60	mA
		V _{CC} = 5.5 V, V _O = 0 V		±35	±60	
r _o	Output resistance	V _{CC} , V+, and V- = 0 V, V _O = ±2 V	300	10M		Ω
I _{off}	Output leakage current	FORCEOFF = GND	V _O = ±12 V, V _{CC} = 3 V to 3.6 V		±25	μA
			V _O = ±10 V, V _{CC} = 4.5 V to 5.5 V		±25	

† All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

‡ Short-circuit durations should be controlled to prevent exceeding the device absolute power-dissipation ratings, and not more than one output should be shorted at a time.

NOTE 4: Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 6)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Maximum data rate		C _L = 1000 pF, One DOUT switching, R _L = 3 kΩ, See Figure 1	250			kbit/s
t _{sk(p)}	Pulse skew§	C _L = 150 pF to 2500 pF, See Figure 2, R _L = 3 kΩ to 7 kΩ		100		ns
SR(tr)	Slew rate, transition region (See Figure 1)	V _{CC} = 3.3 V, R _L = 3 kΩ to 7 kΩ	C _L = 150 pF to 1000 pF	6	30	V/μs
			C _L = 150 pF to 2500 pF	4	30	

† All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

§ Pulse skew is defined as |t_{pLH} - t_{pHL}| of each channel of the same device.

NOTE 4: Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.



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RECEIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 6)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V _{OH}	High-level output voltage	I _{OH} = -1 mA	V _{CC} -0.6	V _{CC} -0.1		V
V _{OL}	Low-level output voltage	I _{OL} = 1.6 mA			0.4	V
V _{IT+}	Positive-going input threshold voltage	V _{CC} = 3.3 V		1.6	2.4	V
		V _{CC} = 5 V		1.9	2.4	
V _{IT-}	Negative-going input threshold voltage	V _{CC} = 3.3 V	0.6	1.1		V
		V _{CC} = 5 V	0.8	1.4		
V _{hys}	Input hysteresis (V _{IT+} - V _{IT-})			0.5		V
I _{off}	Output leakage current	$\overline{\text{EN}} = V_{\text{CC}}$		± 0.05	± 10	μA
r _i	Input resistance	V _I = ± 3 V to ± 25 V	3	5	7	k Ω

† All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

NOTE 4: Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V \pm 0.3 V; C1 = 0.047 μF , C2–C4 = 0.33 μF at V_{CC} = 5 V \pm 0.5 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t _{PLH}	Propagation delay time, low- to high-level output	C _L = 150 pF,	See Figure 3		150		ns
t _{PHL}	Propagation delay time, high- to low-level output	C _L = 150 pF,	See Figure 3		150		ns
t _{en}	Output enable time	C _L = 150 pF, See Figure 4	R _L = 3 k Ω ,		200		ns
t _{dis}	Output disable time	C _L = 150 pF, See Figure 4	R _L = 3 k Ω ,		200		ns
t _{sk(p)}	Pulse skew‡	See Figure 3			50		ns

† All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

‡ Pulse skew is defined as |t_{PLH} - t_{PHL}| of each channel of the same device.

NOTE 4: Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V \pm 0.3 V; C1 = 0.047 μF , C2–C4 = 0.33 μF at V_{CC} = 5 V \pm 0.5 V.

AUTO-POWERDOWN SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)

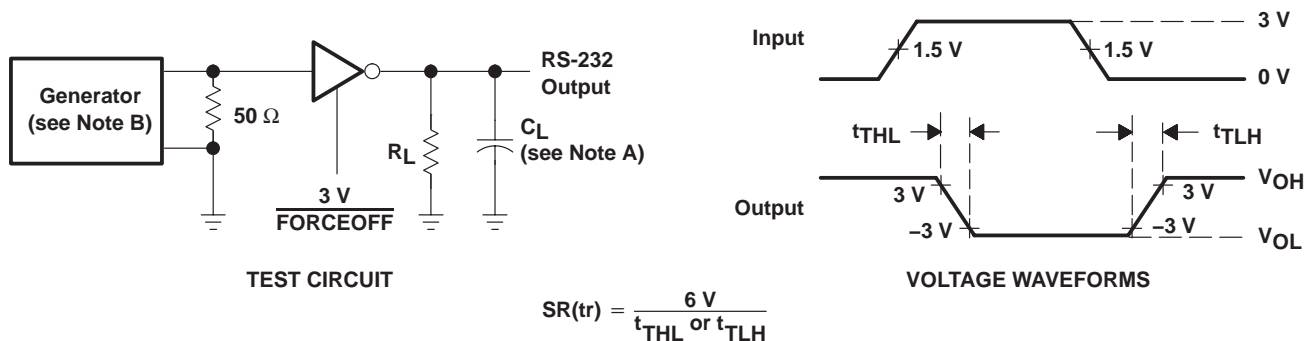
PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{T+}(\text{valid})$	Receiver input threshold for INVALID high-level output voltage	FORCEON = GND, $\overline{\text{FORCEOFF}} = V_{CC}$		2.7	V
$V_{T-}(\text{valid})$	Receiver input threshold for INVALID high-level output voltage	FORCEON = GND, $\overline{\text{FORCEOFF}} = V_{CC}$	-2.7		V
$V_{T}(\text{invalid})$	Receiver input threshold for INVALID low-level output voltage	FORCEON = GND, $\overline{\text{FORCEOFF}} = V_{CC}$	-0.3	0.3	V
V_{OH}	INVALID high-level output voltage	$I_{OH} = -1 \text{ mA}$, $\overline{\text{FORCEOFF}} = V_{CC}$	$V_{CC} - 0.6$		V
V_{OL}	INVALID low-level output voltage	$I_{OL} = 1.6 \text{ mA}$, $\overline{\text{FORCEOFF}} = V_{CC}$		0.4	V

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)

PARAMETER		TYP†	UNIT
t_{valid}	Propagation delay time, low- to high-level output	1	μs
t_{invalid}	Propagation delay time, high- to low-level output	30	μs
t_{en}	Supply enable time	100	μs

† All typical values are at $V_{CC} = 3.3 \text{ V}$ or $V_{CC} = 5 \text{ V}$, and $T_A = 25^\circ\text{C}$.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

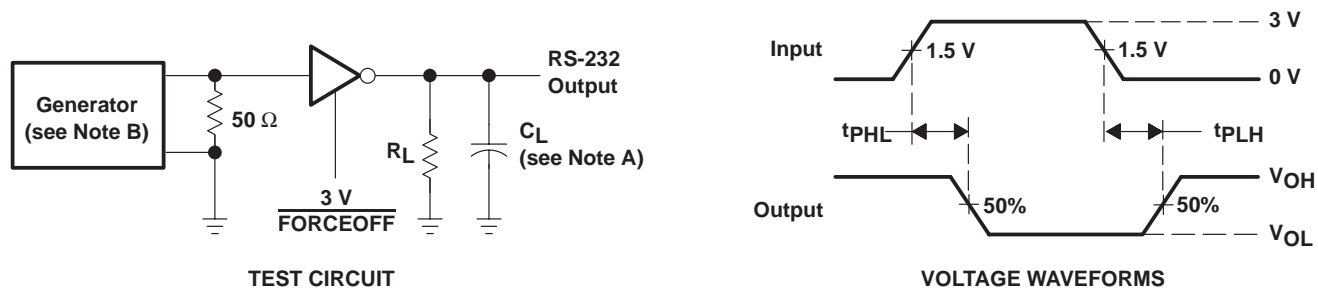
B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$.

Figure 1. Driver Slew Rate

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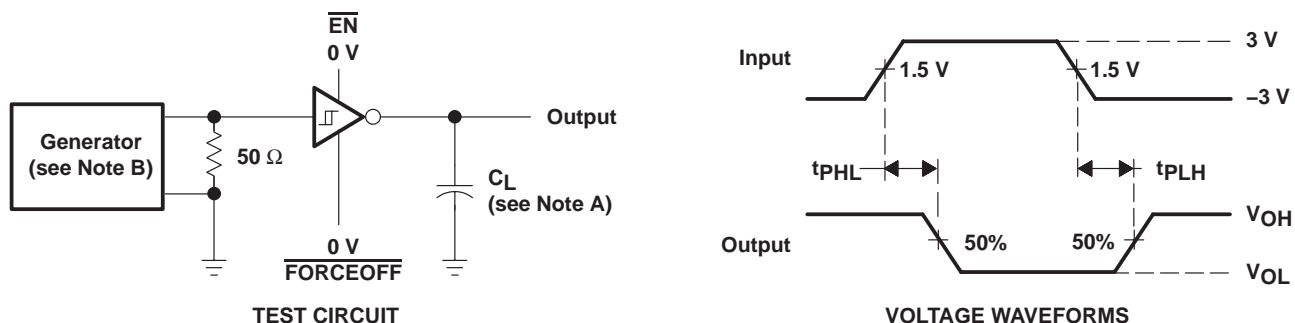
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PARAMETER MEASUREMENT INFORMATION



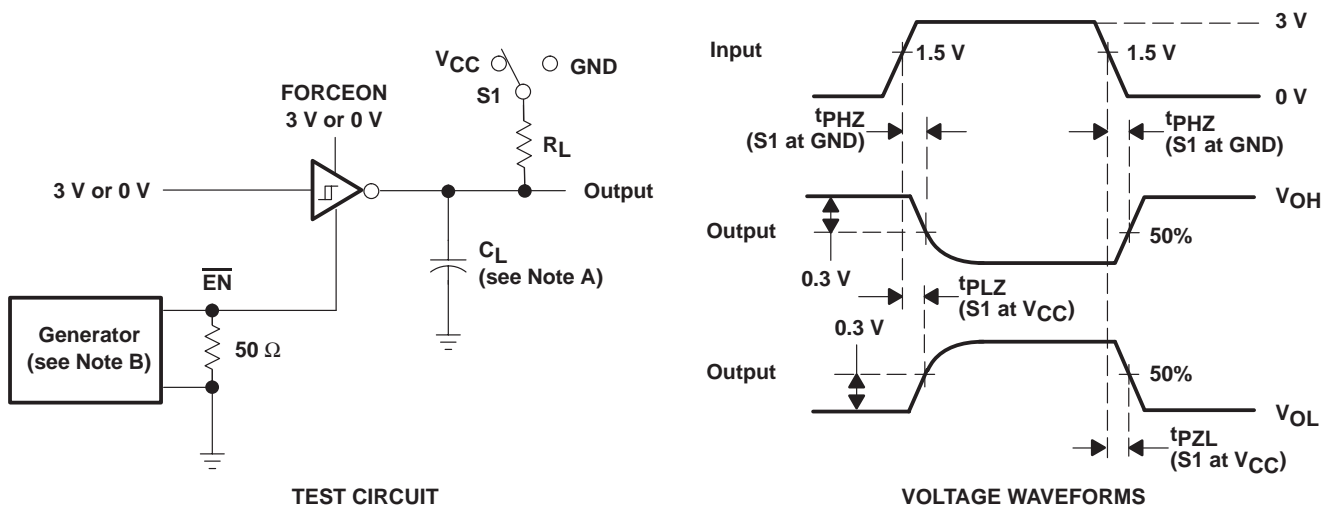
NOTES: A. C_L includes probe and jig capacitance.
 B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

Figure 2. Driver Pulse Skew



NOTES: A. C_L includes probe and jig capacitance.
 B. The pulse generator has the following characteristics: $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

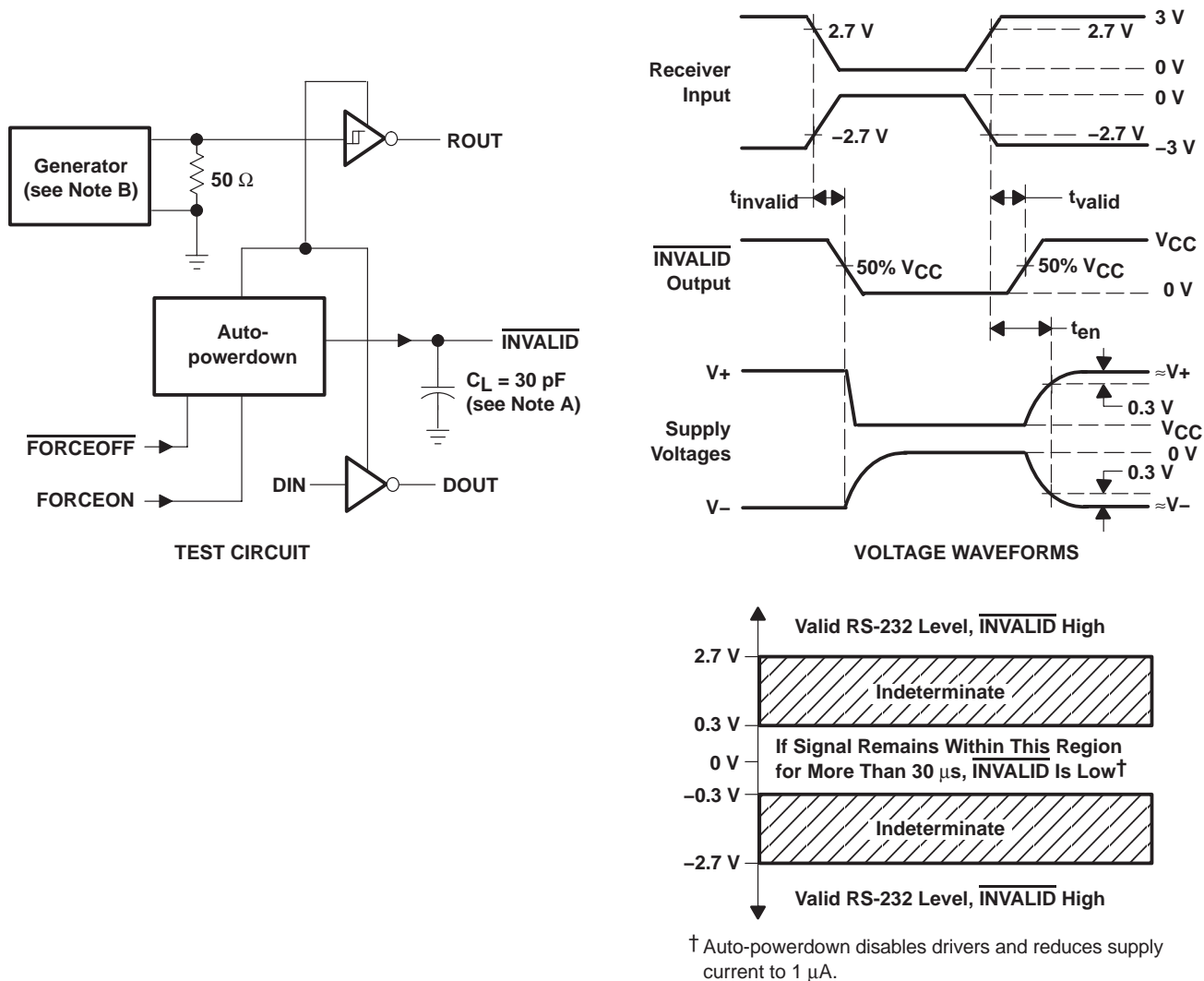
Figure 3. Receiver Propagation Delay Times



NOTES: A. C_L includes probe and jig capacitance.
 B. The pulse generator has the following characteristics: $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

Figure 4. Receiver Enable and Disable Times

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

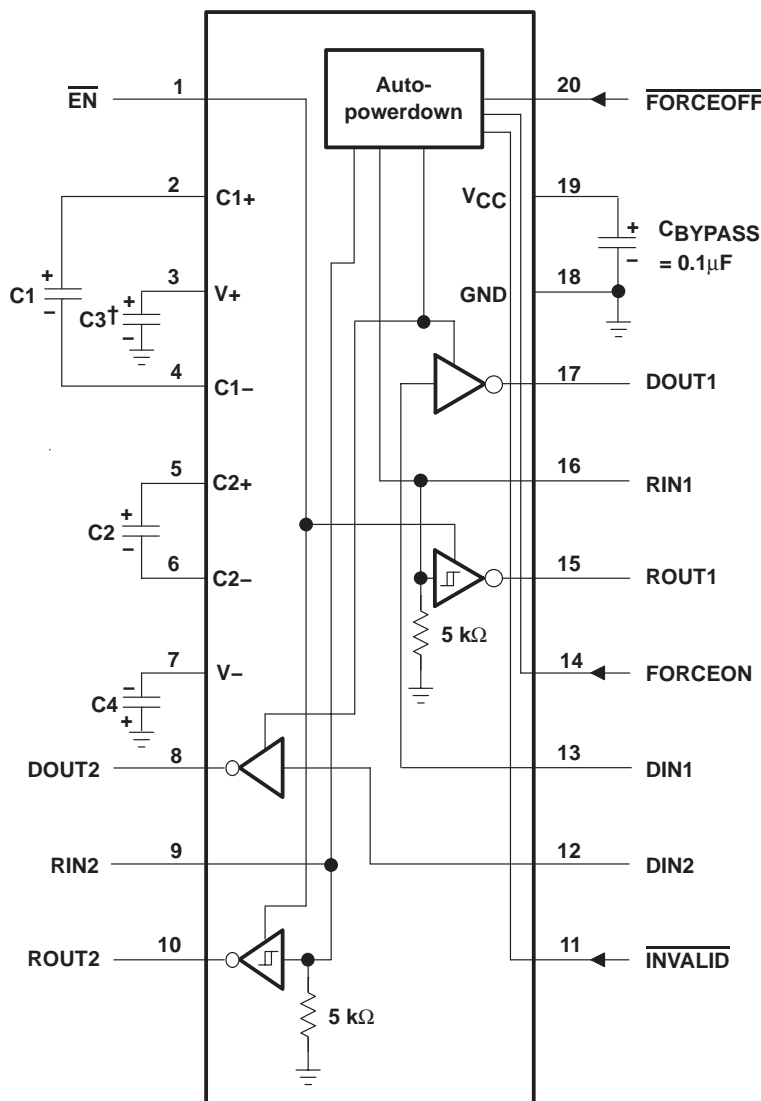
B. The pulse generator has the following characteristics: PRR = 5 kbit/s, $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$.

Figure 5. $\overline{\text{INVALID}}$ Propagation Delay Times and Supply Enabling Time

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APPLICATION INFORMATION



† C3 can be connected to V_{CC} or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

V_{CC} vs CAPACITOR VALUES

V _{CC}	C1	C2, C3, C4
3.3 V ± 0.3 V	0.1 μF	0.1 μF
5 V ± 0.5 V	0.047 μF	0.33 μF
3 V to 5.5 V	0.1 μF	0.47 μF

Figure 6. Typical Operating Circuit and Capacitor Values

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
MAX3223CDB	ACTIVE	SSOP	DB	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3223CDBE4	ACTIVE	SSOP	DB	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3223CDBG4	ACTIVE	SSOP	DB	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3223CDBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3223CDBRE4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3223CDBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3223CDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3223CDWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3223CDWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3223CDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3223CDWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3223CPW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3223CPWE4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3223CPWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3223CPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3223CPWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3223CPWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3223IDB	ACTIVE	SSOP	DB	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3223IDBE4	ACTIVE	SSOP	DB	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3223IDBG4	ACTIVE	SSOP	DB	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3223IDBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3223IDBRE4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3223IDBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3223IDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3223IDWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
MAX3223IDWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3223IDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3223IDWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3223IDWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3223IPW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3223IPWE4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3223IPWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3223IPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3223IPWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3223IPWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

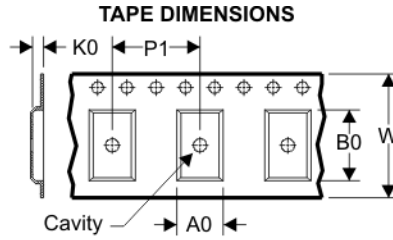
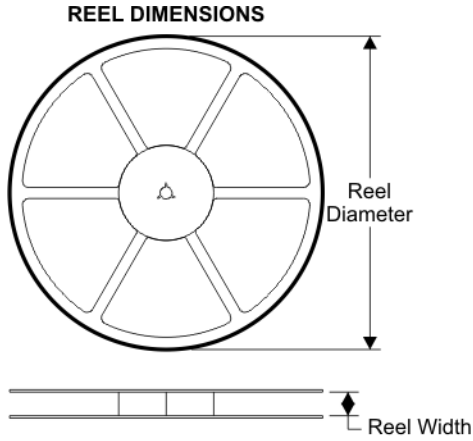
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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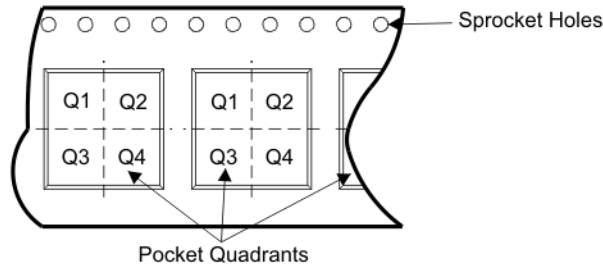
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TAPE AND REEL BOX INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MAX3223CDBR	DB	20	SITE 41	330	16	8.0	8.0	3.0	12	16	Q1
MAX3223CDWR	DW	20	SITE 41	330	24	11.0	13.0	3.0	12	24	Q1
MAX3223CPWR	PW	20	SITE 41	330	16	7.0	7.0	2.0	8	16	Q1
MAX3223IDBR	DB	20	SITE 41	330	16	8.0	8.0	3.0	12	16	Q1
MAX3223IDWR	DW	20	SITE 41	330	24	11.0	13.0	3.0	12	24	Q1
MAX3223IPWR	PW	20	SITE 41	330	16	7.0	7.0	2.0	8	16	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
MAX3223CDBR	DB	20	SITE 41	346.0	346.0	33.0
MAX3223CDWR	DW	20	SITE 41	346.0	346.0	41.0
MAX3223CPWR	PW	20	SITE 41	346.0	346.0	33.0
MAX3223IDBR	DB	20	SITE 41	346.0	346.0	33.0
MAX3223IDWR	DW	20	SITE 41	346.0	346.0	41.0
MAX3223IPWR	PW	20	SITE 41	346.0	346.0	33.0

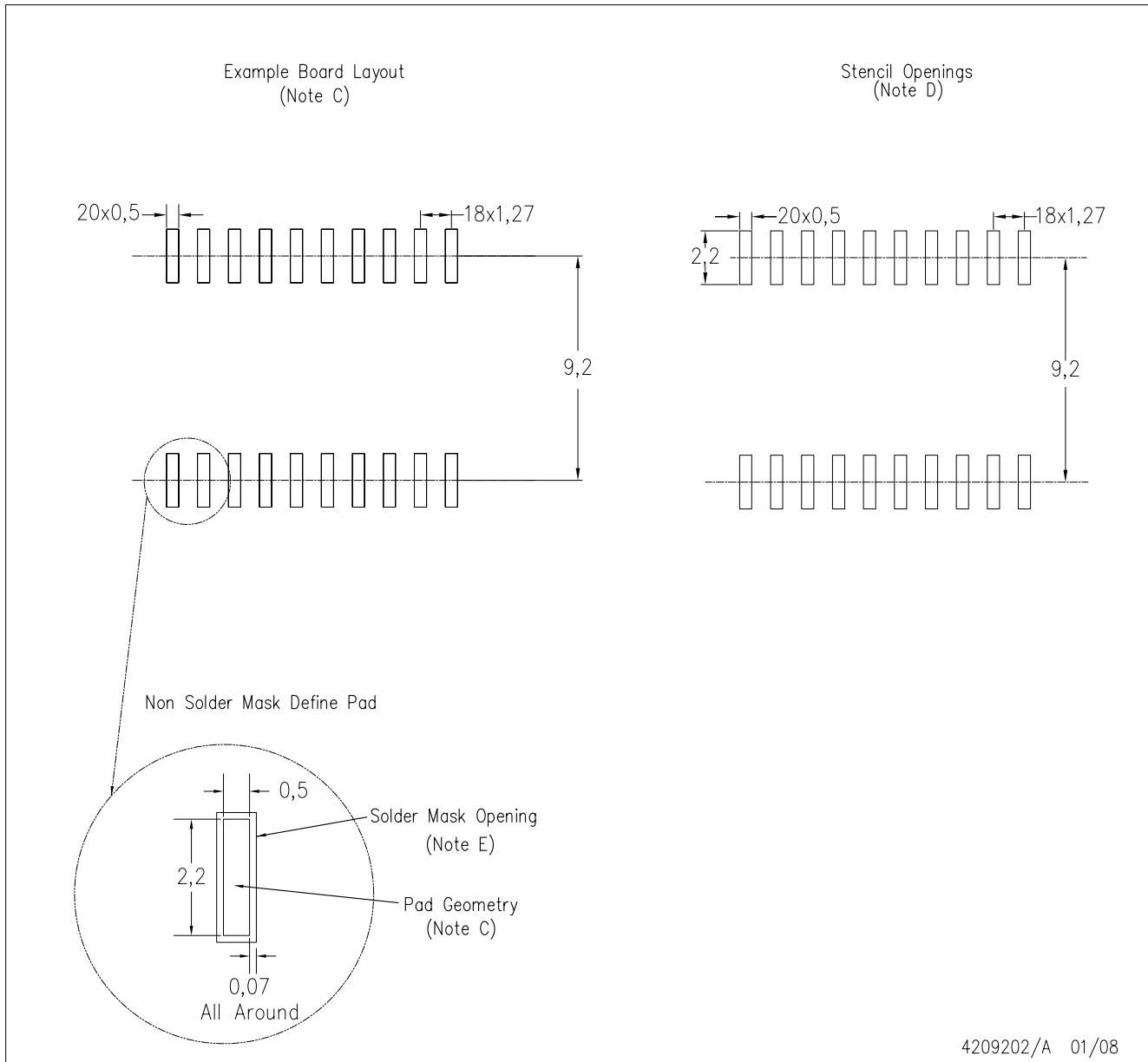
DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)

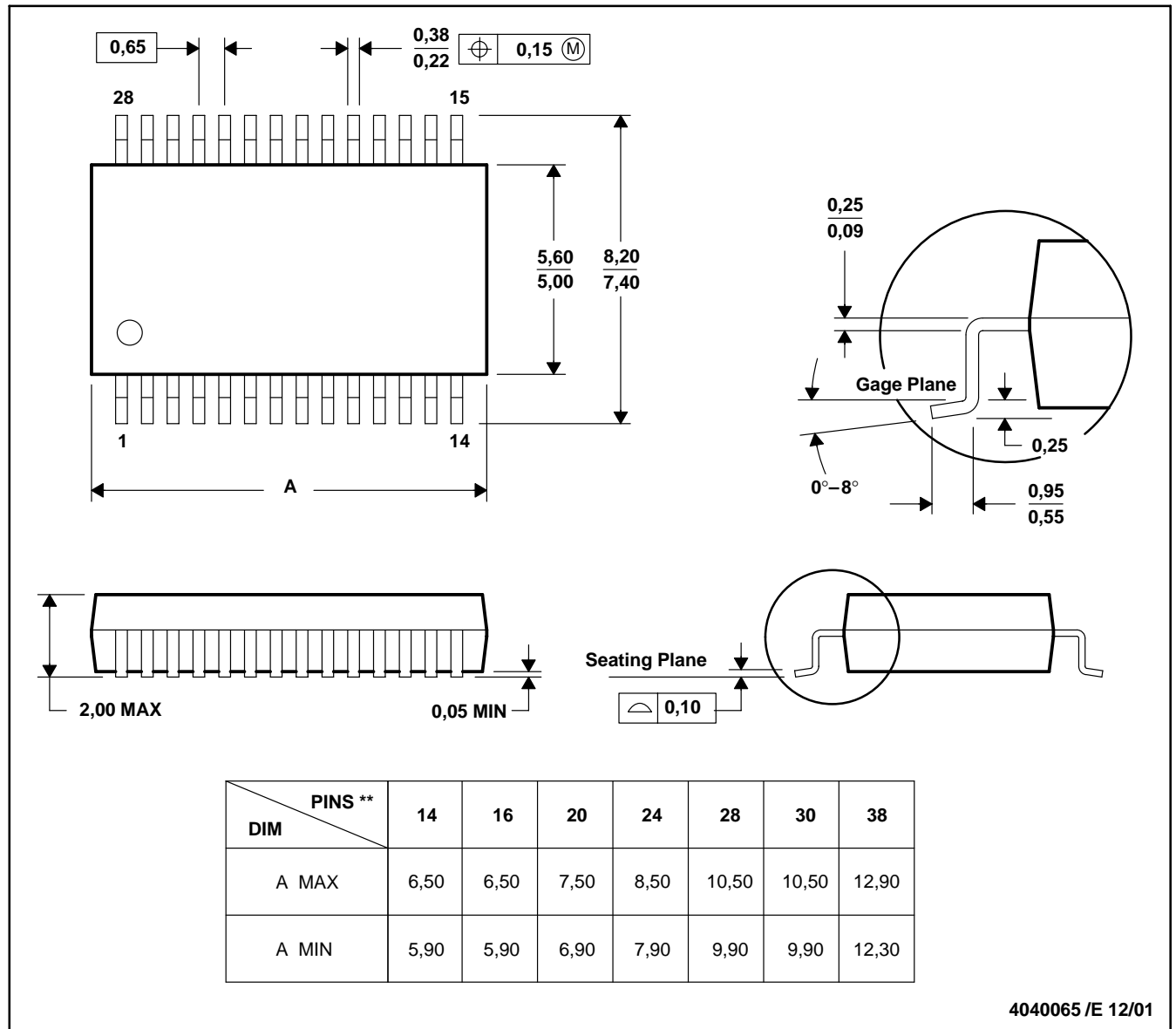


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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